Arizona State University: A Leader in Advanced Packaging R&D

Jason Conrad

Arizona State University

Contents

- My journey
- Introduction to ASU
- ASU strategy
- Recent wins
- Advanced packaging & SHIELD USA
- How to connect

Career overview: Jason Conrad

- **Roles** at ASU (Dec 2023):
    - COO, Southwest Advanced Prototyping Hub
    - Site Lead, MacroTechnology Works
    - Program Director, SHIELD USA

- **Industry Experience** (23 years):
    - Wafer Fab Eng & Ops
    - Silicon Machining R&D Eng
    - Wafering & Epi Eng & Ops

Disclosures

Listed for transparency and objectivity in my research

- Jason has a minor equity interest in **NXP Semiconductors**. NXP develops and manufactures semiconductor devices. NXP may potentially benefit financially from the research findings on advanced packaging presented here.
- Jason has a minor equity interest in **Advanced Micro Devices Inc (AMD)**. AMD designs AI and HPC semiconductors. AMD may potentially benefit financially from the research findings on advanced packaging presented here.
- Jason has a minor equity interest in **Analog Devices Inc (ADI)**. ADI designs and produces semiconductors to empower the Intelligent Edge. ADI may potentially benefit financially from the research findings on advanced packaging presented here.
- Jason has a minor equity interest in **International Business Machines Corp (IBM)**. IBM researches, designs, and manufactures semiconductors. IBM may potentially benefit financially from the research findings on advanced packaging presented here.

Why is ASU at IMAPS DPC?

Arizona State University

- ~190,000 degree-seeking students
- 430,000+ learners
- $1 billion in research annually
- Largest engineering school in U.S.
- #1 in the U.S. for innovation (10 years, 2016–25)
- Emerging leader in semiconductor and advanced packaging R&D

Arizona State University

#1 in the U.S. for innovation

BEST COLLEGES
U.S.News & WORLD REPORT
MOST INNOVATIVE
2025

ASU ahead of MIT and Stanford
— U.S. News & World Report,
10 years, 2016–25

ASU Charter

ASU is a comprehensive public research university, measured not by whom it excludes, but by whom it includes and how they succeed; advancing research and discovery of public value; and assuming fundamental responsibility for the economic, social, cultural and overall health of the communities it serves.

Fulton Schools of Engineering

Fall 2024

50+
graduate degree programs

27
undergraduate degree programs

#3 for licenses & options

#2 patents

#3 for startups

$281M
in awards

33,000+
students
estimated, in-person and online

7,300+
graduates
across all degree levels in AY2023-24

550+
faculty
across ranks

44
NSF CAREER
awards over the past four years

ASU's microelectronics strategy

ASU focus on Semiconductors

ASU is responsible for nation’s success in semiconductors

Reclaiming America’s position as the world’s leader in semiconductor manufacturing, research and development is a vitally important endeavor that requires collaboration and constant innovation. Make no mistake, this is an intense, long-term global competition and America’s universities are called upon to play an important role in this process by working with industry and producing the educated workforce that is needed to do this job.

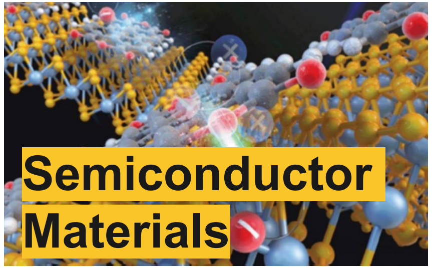
Arizona State University has a responsibility to commit its intellect, energy and resources to this effort – from research and discovery to providing the access and tools for learning. There is much more to do over the coming years and it if very exciting to partner with so many others who share our commitment to making things happen.”

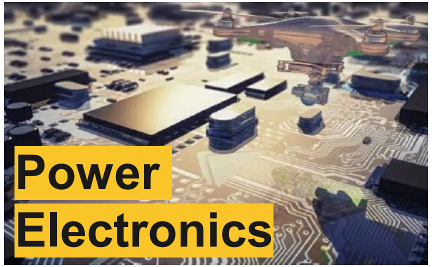
– Michael M. Crow

President of Arizona State University

ASU strategy

- Partner with industry
- Maximize CHIPS Act and other awards
- Bridge the “Valley of Death”
- Develop the workforce
- Focus on key capability areas:


Semiconductor Materials


Power Electronics


5G/6G Communications


Advanced Packaging

$52.7 billion CHIPS Act summary

ASU involved in all aspects of CHIPS Act

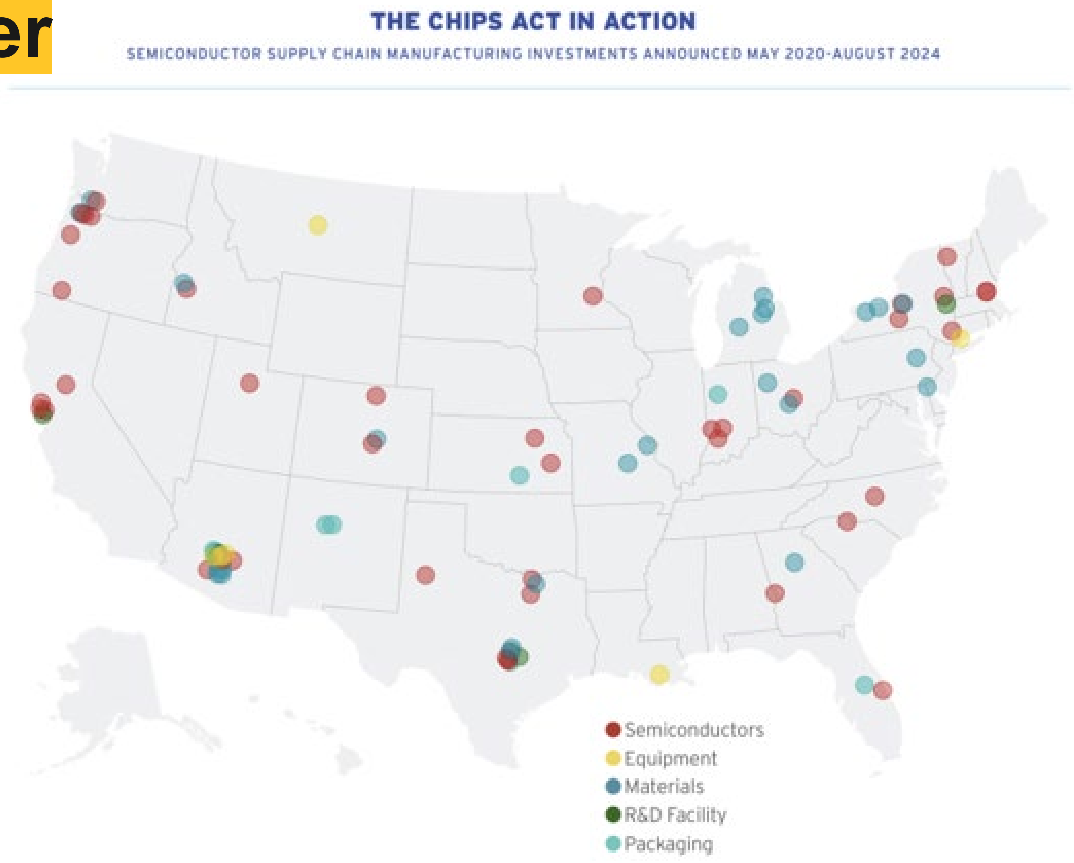
CHIPS for AMERICA

Department of Defense	**Department of Commerce**	**Department of State**	**National Science Foundation**
Microelectronics Commons **$2 billion**	**Manufacturing Incentives and R&D Programs** **$50 billion**	**International Technology Security and Innovation Fund** **$500 million**	**National Network for Microelectronics Education** **$200 million**
• Lab-to-fab capabilities • Defense prototyping projects • 8 regional hubs	• $39 billion for manufacturing incentives • $11 billion in R&D for NSTC, NAPMP, and up to 3 Manufacturing USA Institutes	• Develop allied country semiconductor workforce • Improve supply chain resilience • Enhance cybersecurity	• Curriculum • Training • Faculty hiring

Arizona is the fastest growing U.S. semiconductor cluster

$200

More than ~~$100~~ billion in private sector semiconductor investments in Arizona since 2021



Sources: Semiconductor Industry Association 2024 State of the Semiconductor Industry Report and invest.gov

Proximity to leading-edge manufacturers

MacroTechnology Works (MTW)

- At ASU Research Park in Tempe AZ
- 250,000 ft^2 site
- 49,000 ft^2 cleanroom
- 22,000 ft^2 wet/dry labs
- R&D, pilot, and production capable
- Flexible subdivision for proprietary programs

Student access; professionally staffed

R&D excellence at ASU

ASU is committed to semiconductor R&D leadership

At ASU's MacroTechnology Works (MTW), we're revolutionizing microelectronics R&D with cutting-edge faculty research, student engagement, core facilities, and strategic industry partnership and co-location. Our initiatives, like the SWAP Hub and SHIELD USA, demonstrate our commitment to the nation’s leadership in semiconductor technology and advanced packaging.”

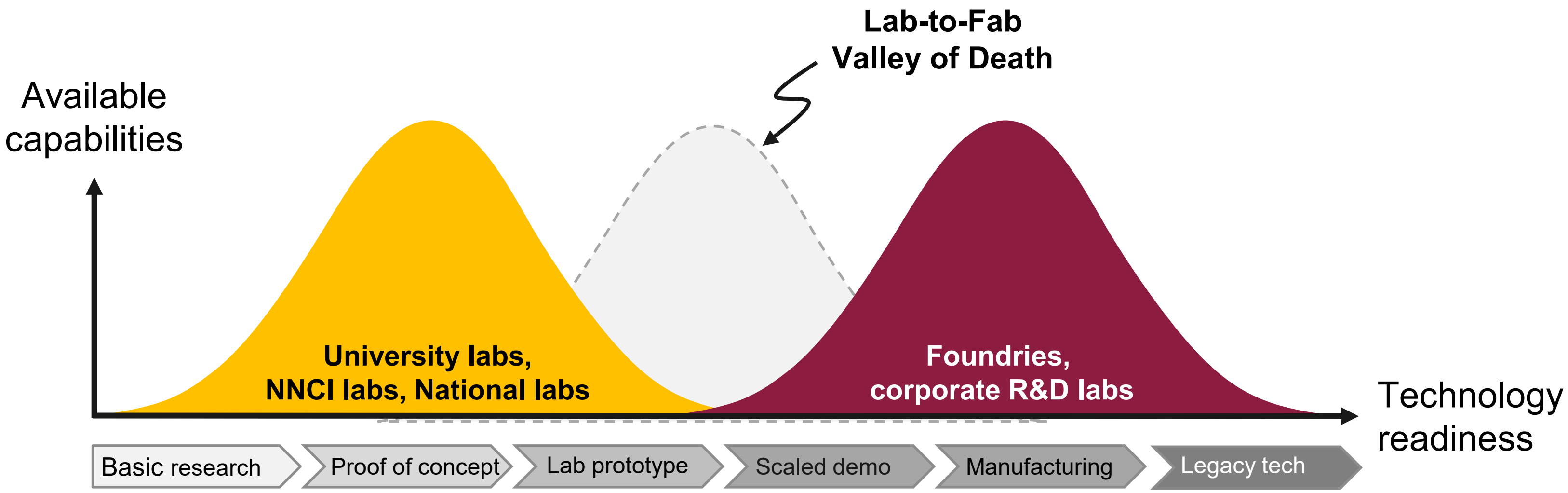
– Sally Morton

Executive Vice President of ASU Knowledge Enterprise

Bridging the "Valley of Death"

Exploiting industry-scale equipment

- Faculty labs → innovation
- Core Facilities → access to industry-scale tools
- Industry co-location → partnership

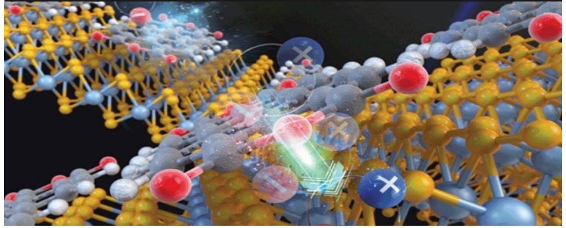


Is the strategy working?

R&D capability and industry partnerships

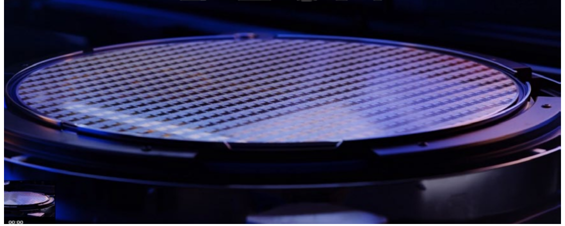
Semiconductor Materials

$270M partnership with Arizona Commerce Authority and Applied Materials to create cutting-edge Materials to Fabrication lab at MTW



Advanced Packaging & Heterogenous Integration

DoD Microelectronics Commons investment for Deca 300 mm Fan Out Wafer Level capability at ASU with license to run M-Series and Adaptive Patterning at MTW



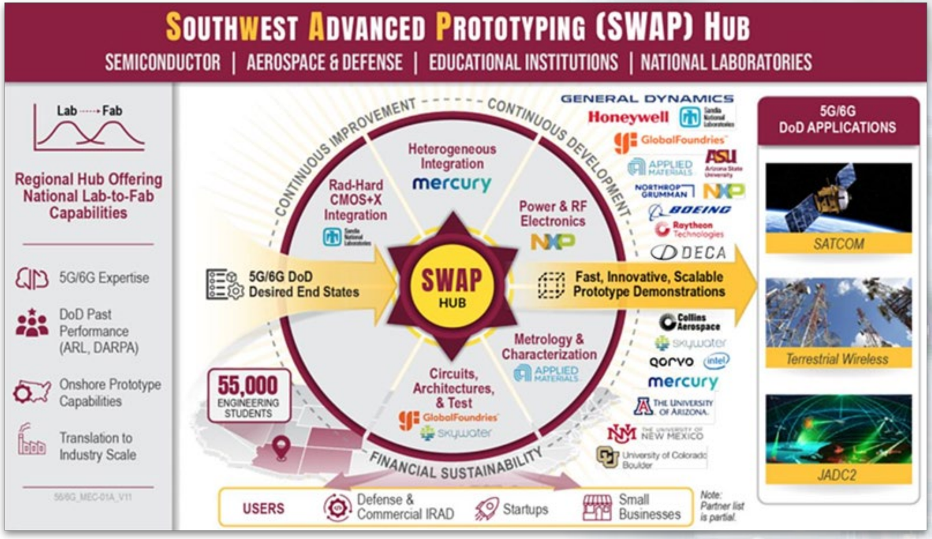
Power Electronics and 5G/6G

$17.5 million partnership with Arizona Commerce Authority and NXP to create high-frequency and high-power device test capabilities at MTW

SWAP Hub capabilities

Southwest Advanced Prototyping Hub
Arizona State University

- **Technical Areas**
  - Heterogeneous Integration: Deca M-Series Gen 2
  - Power and RF Electronics
  - Metrology and Characterization
  - Circuits, Architecture and Test
  - Rad-Hard CMOS+X Integration Sandia National Laboratories
- **Cross-cutting Themes**
  - Workforce Development
  - Trusted and Assured THE UNIVERSITY OF NEW MEXICO
  - Extreme Environments



SOUTHWEST ADVANCED PROTOTYPING (SWAP) HUB

SEMICONDUCTOR | AEROSPACE & DEFENSE | EDUCATIONAL INSTITUTIONS | NATIONAL LABORATORIES

Lab → Fab

Regional Hub Offering National Lab-to-Fab Capabilities

- 5G/6G Expertise
- DoD Past Performance (ARL, DARPA)
- Onshore Prototype Capabilities
- Translation to Industry Scale

5G6G_MEC-01A_V11

CONTINUOUS IMPROVEMENT — CONTINUOUS DEVELOPMENT — FINANCIAL SUSTAINABILITY

5G/6G DoD Desired End States → SWAP HUB → Fast, Innovative, Scalable Prototype Demonstrations

Heterogeneous Integration: mercury
Power & RF Electronics: NXP
Metrology & Characterization: APPLIED MATERIALS
Circuits, Architectures, & Test: GlobalFoundries, skywater
Rad-Hard CMOS+X Integration: Sandia National Laboratories

55,000 ENGINEERING STUDENTS

USERS: Defense & Commercial IRAD; Startups; Small Businesses

Note: Partner list is partial.

5G/6G DoD APPLICATIONS
- SATCOM
- Terrestrial Wireless
- JADC2

170+ members

MICROELECTRONICS COMMONS
BRIDGING THE GAP FROM LAB TO FAB

Strength in 5G/6G, AI hardware, and Commercial Leap Ahead

Awarded projects: $29.6M Year 1 funding

- Project 1 - 5G/6G - Integrated RF GaN Technology to Support NextG Wireless Systems
  $5.1M
  Team: **NXP**, Raytheon, National Instruments, ASU
- Project 2 - 5G/6G - SMART - Scalable Modular Architecture for RF Transceivers
  $5.7M
  Team: **Alphacore**, ASU, Rice, Lockheed Martin, Auburn
- Project 3 - AI Hardware - SLEAC - Spaceborne Low-Energy AI Computing
  $6.0M
  Team: **ASU**, Sandia, Raytheon, USC, UC Boulder, LTC Design, AFRL
- Project 4 - CLA - Multi-MHz, High Density, Ultra-fast RADAR Power Converter
  $5.0M
  Team: **ASU**, Sandia, Infineon, Lockheed Martin, Thermavant
- Project 5 - Secure Edge - ARC-V Secure Processor
  $7.8M
  Team: **Idaho Scientific**, Synopsys, Global Foundries, Mercury Computer, BAE Systems, ASU

SHIELDUSA

Substrate-based Heterogeneous Integration Enabling Leadership Demonstration for the USA

Arizona State University & DECA

NAPMP NOFO1 $100M Award

Materials & Substrates – Organic Materials

CHIPS for AMERICA

Natcast NSTC and NAPPF

SEMI INSIGHTS | INBUSINESSPHX.COM | JANUARY 6 2025

Arizona and ASU Selected for Flagship Prototyping and Advanced Packaging R&D Facility

inbusinessPHX.com

Natcast
National Center for the Advancement of Semiconductor Technology

The Arizona Commerce Authority announced that the U.S. Commerce Department and Natcast, the operator of the National Semiconductor Technology Center (NSTC), have selected Arizona as the site of the co-located NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility, the third of three CHIPS for America research and development (R&D) flagship facilities.

The facility will combine 300mm research and prototyping for front-end manufacturing and packaging capabilities, meeting a unique need for advanced packaging R&D within the U.S. semiconductor ecosystem. Key packaging capabilities are expected to include a baseline advanced packaging piloting line to enable the development and commercialization of new packaging processes. The facility will also support U.S. workforce development efforts by providing opportunities for collaborative, hands-on research utilizing industry-leading tools and equipment.

Investments in ASU microelectronics since 2023

$100M capabilities + $30M projects

ASU Southwest Advanced Prototyping Hub
Arizona State University

Center for Advanced Wafer-Level Packaging Applications and Development

DECA ASU

$100M award

SHIELDUSA
Substrate-based Heterogeneous Integration Enabling Leadership Demonstration for the USA
ASU Arizona State University & DECA

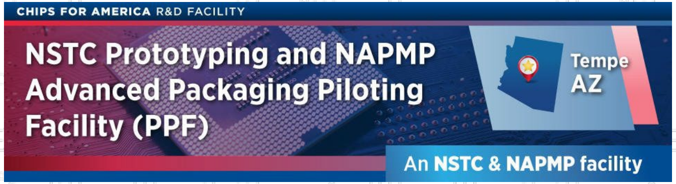
$270M investment materials-to-fab-center

APPLIED MATERIALS | ASU Arizona State University | ARIZONA COMMERCE AUTHORITY

$17.5M for 5G/6G ecosystem

NXP | ARIZONA COMMERCE AUTHORITY | ASU

$3.1B facility in ASU Research Park

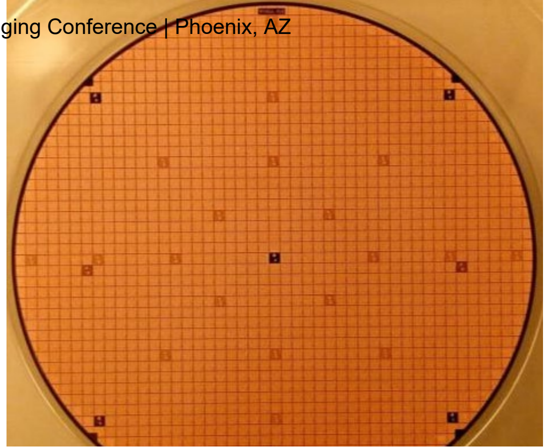

CHIPS FOR AMERICA R&D FACILITY
NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility (PPF)
Tempe AZ
An NSTC & NAPMP facility

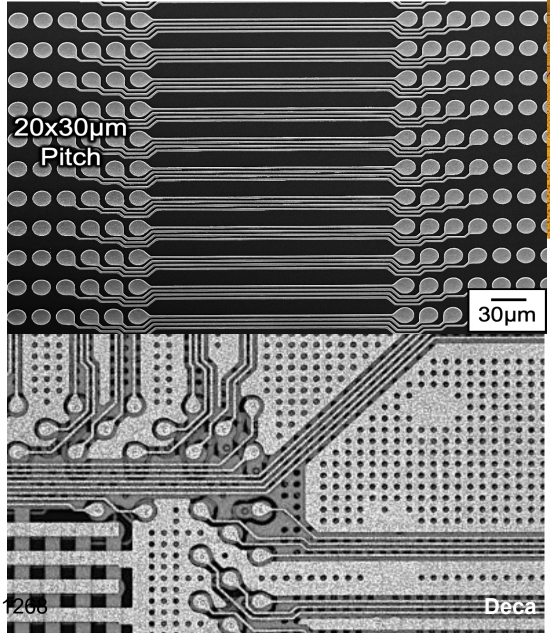
>$500M

ASU advanced packaging capabilities

300mm FOWLP line

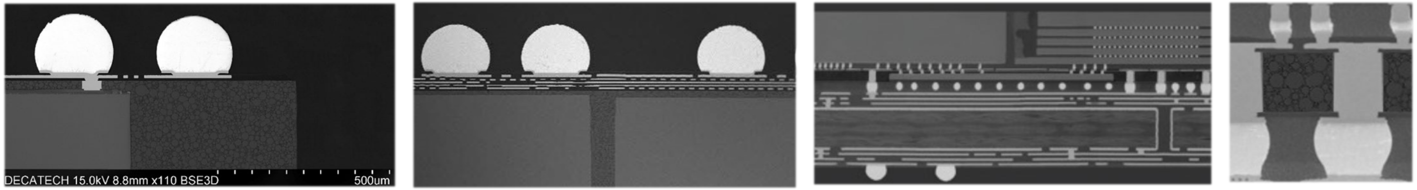
- **20+ tools** to run **Deca's FOWLP** process on **300 mm** round "panels"
- **Capability available to all**, summer 2025 through AEP Core at MTW
- **Foundation** for SHIELD USA and more

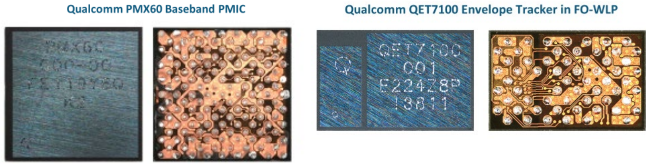




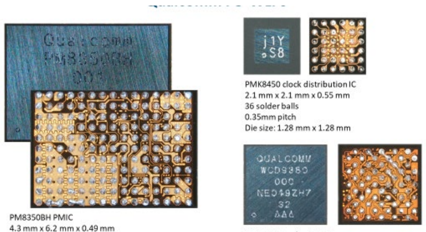
Deca Technologies

Industry Leading M-Series™ Fan-out & Adaptive Patterning®





iPhone 14 Pro Max Teardown by TechSearch International
(Five M-Series devices)



PM8350BH PMIC
4.3 mm x 6.2 mm x 0.49 mm
165 solder balls
0.4mm pitch
Die size: 4.20 mm x 5.94 mm

shown to scale

Source: TechSearch International, Inc. teardowns.

PMK8450 clock distribution IC
2.1 mm x 2.1 mm x 0.55 mm
36 solder balls
0.35mm pitch
Die size: 1.28 mm x 1.28 mm

WCD9380 audio CODEC
3.0 mm x 3.1 mm x 0.47 mm
60 solder balls
0.35mm (0.49x0.49) staggered pitch
Die size: 2.80 mm x 2.92 mm

Deca is the #1 independent provider of advanced packaging technology[1]

... over 6 billion M-Series devices in the field

ASE GROUP nepes skywater ASU

Fan-out WLP & PLP Technologies 2021- Markets & Technology Report, Yole Developement, June 2021

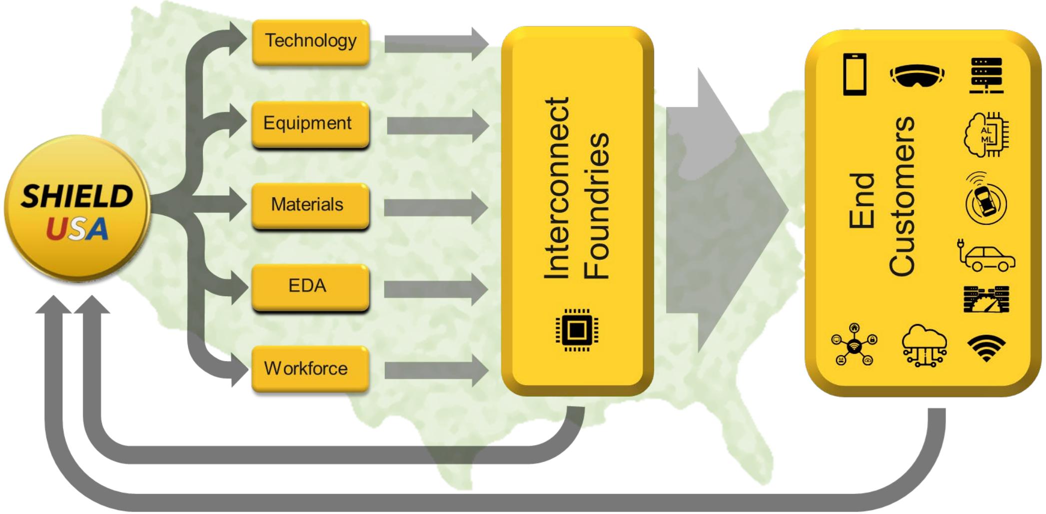
SHIELD USA

Substrate-based **H**eterogeneous **I**ntegration **E**nabling **L**eadership **D**emonstration for the **USA**

Supporting the Growing US Ecosystem

SHIELD USA will:

- Engage and develop ecosystem
- Enable R&D
- Deliver leap-ahead technology
- Train packaging workforce



Enable domestic **Interconnect Foundries** for leading-edge packaging

SHIELD partnerships

Driving innovation across the supply chain

- **Leadership:**

ASU

DECA

- **Core partners:**

AMD

ANALOG DEVICES

HEIDELBERG INSTRUMENTS

IBM

THE NATIONAL CENTER FOR AMERICAN INDIAN ENTERPRISE DEVELOPMENT

NXP

ROGERS CORPORATION

saras MICRO DEVICES

skywater

synopsys®

UNIVERSITY OF MARYLAND

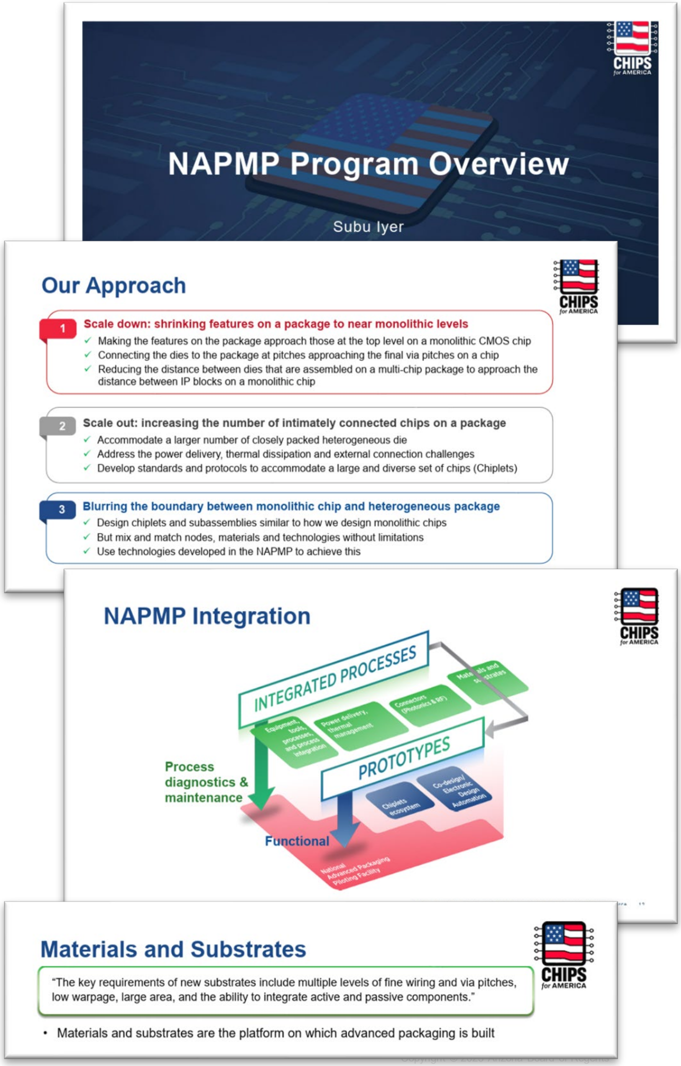
- **Faculty:** 8 faculty with 14 graduate students

NAPMP vision

Substrates are the foundation for advanced packaging

- Scale down: smaller features
- Scale out: more connected chips
- Packages designed like chips

Subu Iyer
Senior Technical Advisor



NAPMP Program Overview

Subu Iyer

Our Approach

1 Scale down: shrinking features on a package to near monolithic levels
- ✓ Making the features on the package approach those at the top level on a monolithic CMOS chip
- ✓ Connecting the dies to the package at pitches approaching the final via pitches on a chip
- ✓ Reducing the distance between dies that are assembled on a multi-chip package to approach the distance between IP blocks on a monolithic chip

2 Scale out: increasing the number of intimately connected chips on a package
- ✓ Accommodate a larger number of closely packed heterogeneous die
- ✓ Address the power delivery, thermal dissipation and external connection challenges
- ✓ Develop standards and protocols to accommodate a large and diverse set of chips (Chiplets)

3 Blurring the boundary between monolithic chip and heterogeneous package
- ✓ Design chiplets and subassemblies similar to how we design monolithic chips
- ✓ But mix and match nodes, materials and technologies without limitations
- ✓ Use technologies developed in the NAPMP to achieve this

NAPMP Integration

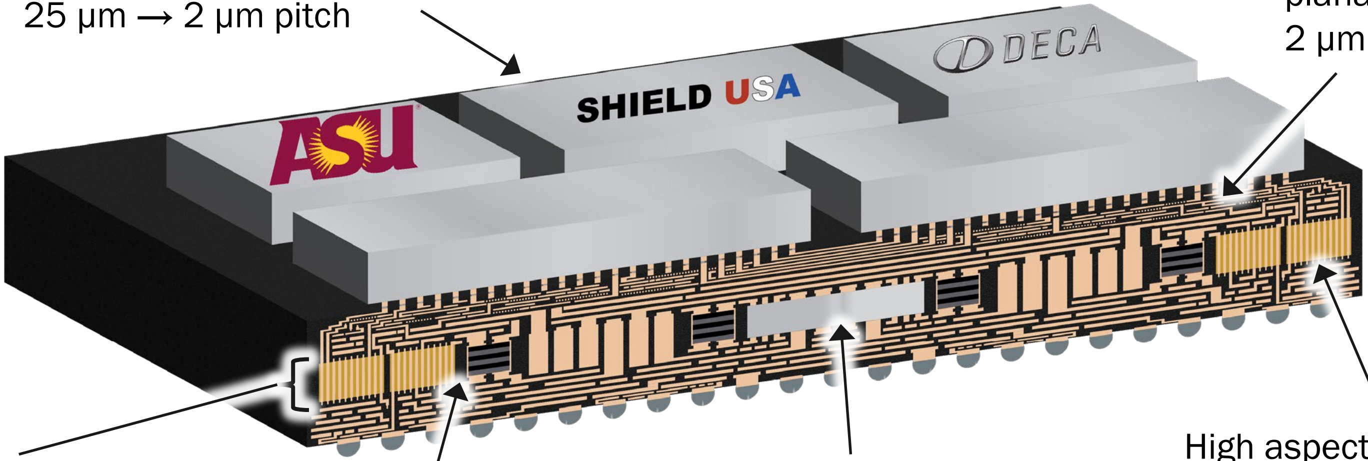
Materials and Substrates

"The key requirements of new substrates include multiple levels of fine wiring and via pitches, low warpage, large area, and the ability to integrate active and passive components."

- Materials and substrates are the platform on which advanced packaging is built

SHIELD USA leap-ahead technology

Transforming proven fan-out technology into advanced molded core substrates



Ultra-fine pitch chiplets & dielets
25 μm → 2 μm pitch

Ultra-high density
planarized MDx RDLs
2 μm → 0.5 μm L&S

Molded fan-out core

High aspect-ratio vertical
interconnect blocks (VIBs)
→ 20 μm pitch through-core

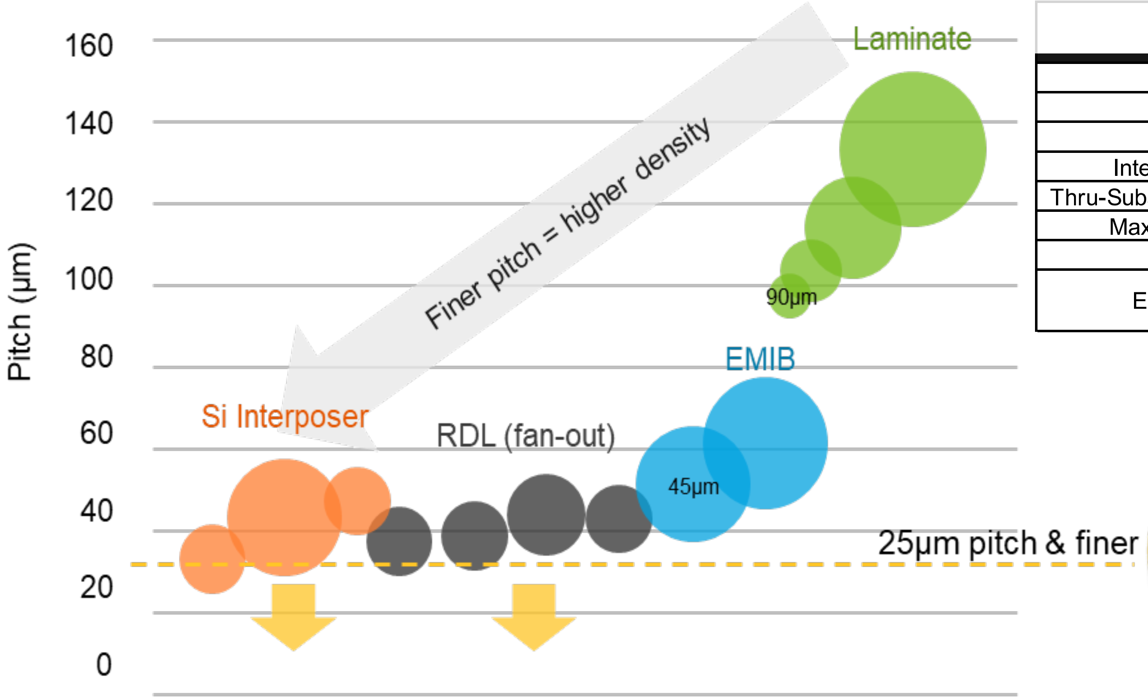
Embedded active devices
→ Power management
→ RF & III-V devices
→ Memory, IO controllers, etc.

Embedded passives
→ High density capacitors
→ Novel inductors for power delivery

SHIELD USA process targets

Driving silicon-like capabilities on organic materials

Chiplet Packages in Production



Demonstrator	1	4
Min. Line Width	2 µm	0.5 µm
Min. Line Space	2 µm	0.5 µm
Min Bump Pitch	25 µm	2 µm
Interlevel Via Diameter	5 µm	1 µm
Thru-Substrate Via Diameter	35 µm	12 µm
Max # Layers Per Side	3	10
Max Thickness	0.85 mm	1.5 mm
Embedded Passives		Capacitors + Inductors

SHIELD Capabilities

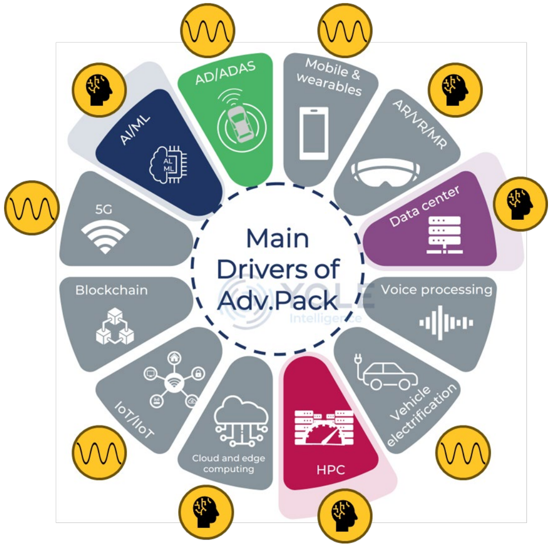
Source: *TechSearch International (2024) & customer input*

SHIELD USA exemplars

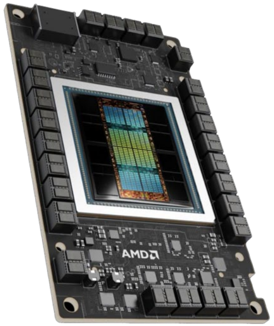
Proving the technology where the market demands it

- **The Advanced Packaging Market**
  - **$38B** today
  - **$69B** by 2029 (11% CAGR)

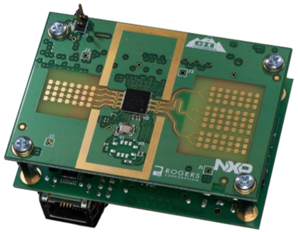
- **SHIELD USA exemplars:**
  - #1: High performance AI
  - # 2: mmWave & High-Frequency RF



AI & HPC



RF, mmWave & ADAS

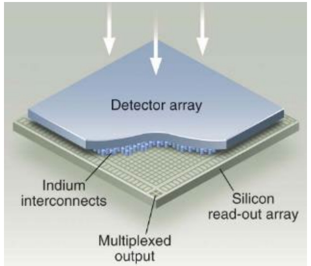


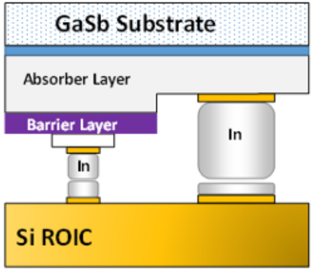
Source: *Yole Intelligence (2024). Status of the Advanced Packaging Industry 2024.*

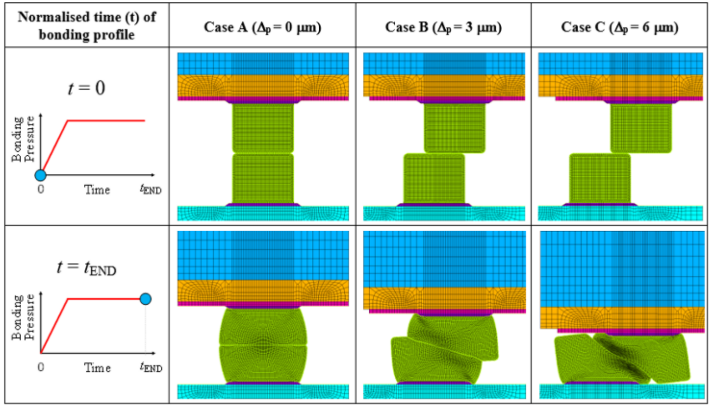
Supported by simulation and metrology

Faculty leadership key to our success

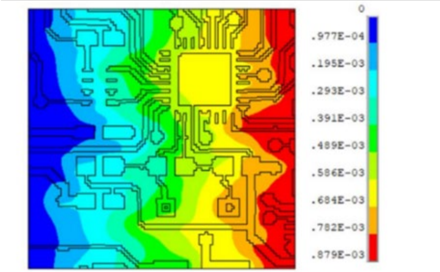
S. Stoyanov and C. Bailey, "Modeling Insights Into the Assembly Challenges of Focal Plane Arrays," in IEEE Access (2023)



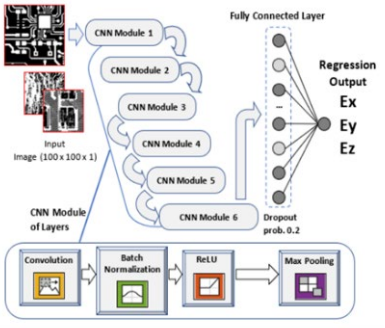


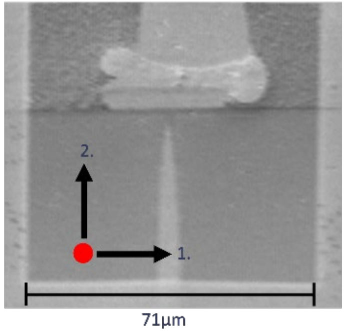


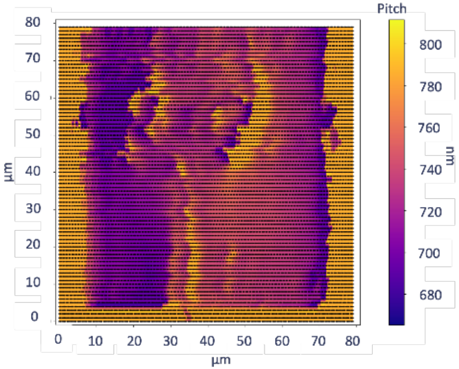
S. Stoyanov and C. Bailey, "Deep Learning Modelling for Composite Properties of PCB Conductive Layers," EuroSimE (2022)



igure 3: Example of FEA prediction for *X*-displacement
mm) field of a copper pattern under

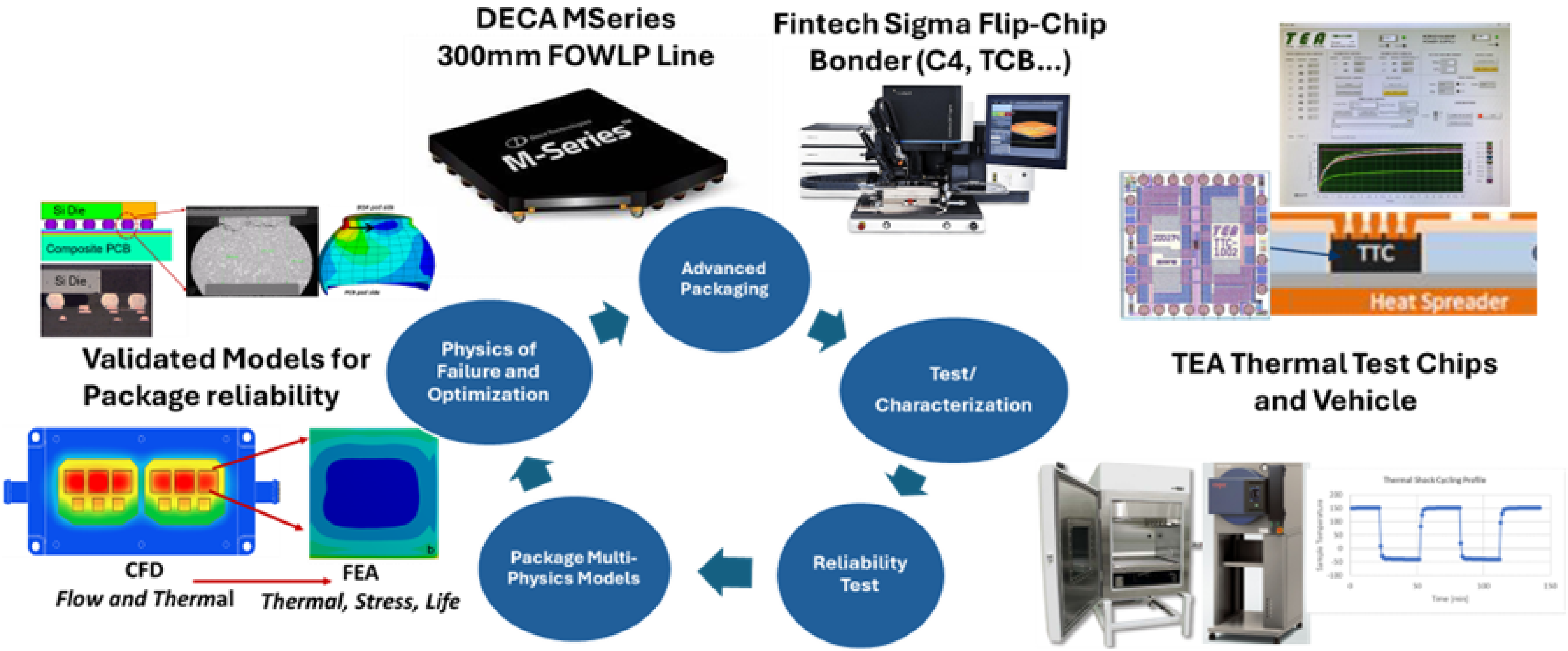






Supported by reliability predictions

Faculty leadership key to our success



DECA MSeries 300mm FOWLP Line

Fintech Sigma Flip-Chip Bonder (C4, TCB…)

TEA Thermal Test Chips and Vehicle

ESPEC HALT/HASS, HAST and TC Chambers

Validated Models for Package reliability

CFD *Flow and Thermal*

FEA *Thermal, Stress, Life*

Advanced Packaging

Test/ Characterization

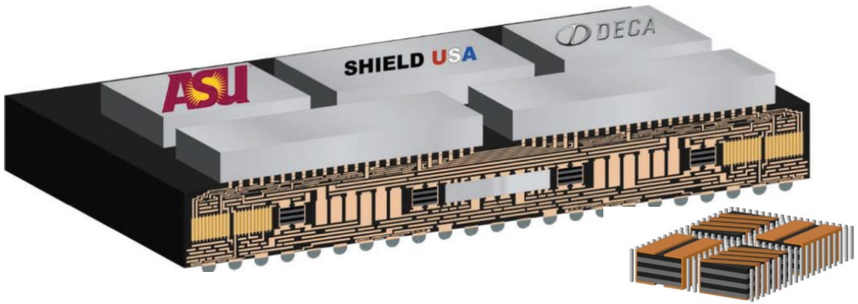
Reliability Test

Package Multi-Physics Models

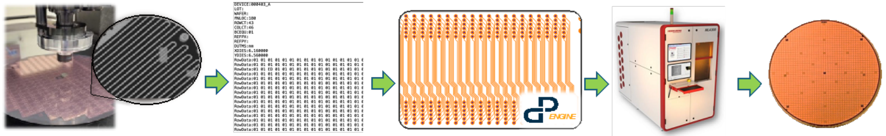
Physics of Failure and Optimization

SHIELD USA vision

- **Cost-effective organic substrates**
  - ○ Wafer-like processing enabling 600mm panels
  - ○ Digital lithography & Adaptive Patterning
  - ○ Ultra-High Density RDL (Silicon like L/S)
  - ○ 5% wiring for signals; rest for power
- **Chip-like design flow**
- **Materials optimization**
  - ○ Non-Polyimide Dielectric
  - ○ Df, Dk, CTE…
- **Design for Reliability**
  - ○ Changing CTE through substrate



Embedded Components and VIB's



Optical inspection

Defect map

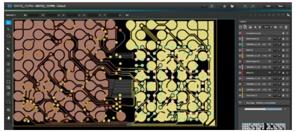
Dynamically generate lithography pattern to reroute around defects

LDI Exposure

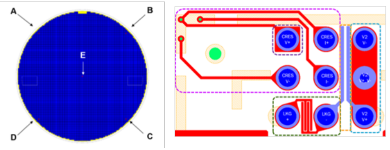
Unique lithography pattern per layer

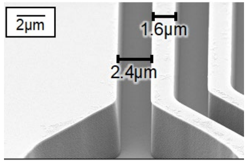
Adaptive Defect Mitigation

Automated Optical Inspection (AOI)



In-Process Electrical Test





Defect Metrics & Measurements

Goals for workforce development

Harnessing the power of ASU

- **Build for scale to reach many**
  - Digital and physical infrastructure
  - New courses and degrees
- **Design flexible (and stackable) pathways**
  - Stackable modular learning units
  - Learner pathways for any STEM student
  - Programs for working professionals
- **Expand access to more students**
  - K-12
  - Community colleges
  - Industry
  - Government
  - Non-profits
  - Community organizations

Ways to Connect

Key Links

ASU

https://www.asu.edu/

Microelectronics

https://microelectronics.asu.edu/

Deca

https://thinkdeca.com/

Workforce Development

https://microelectronics.asu.edu/workforce-development/

Core Facilities

https://cores.research.asu.edu/

SWAP Hub

SHIELD USA

Conclusion

Conclusion

ASU has the

- Responsibility
- Strategy
- Scale
- Facilities
- Team
- Partnerships

To win!

Any questions?