Thermal Performance of High Thermal Conductivity TIM for Large Advanced Package through TTV Measurement and FEM Analysis Approach

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Abstract

With the development of artificial intelligence (AI) and high-performance computing (HPC) technology, advanced packages such as CoWoS (Chip on Wafer on Substrate) have become more popular in recent years due to its outstanding signal transmission speed and space management efficiency. Nevertheless, such high-power applications and the large size of heterogeneous integrated package may lead to thermal and high package warpage problems. In that case, the high stiffness heat spreader is usually used to solve the problem of large warpage. However, structural damage caused by stress and additional thermal resistance from the interface between heat spreader and die top surface have occurred. In terms of stress and thermal issues, optimizing packaging material selection and high thermal conductivity thermal interface material (TIM) are widely used to reduce the stress risk and enhance thermal performance. Therefore, it is important to accurately predict mechanical stress performance and thermal behavior.

In this study, the thermal conductivity that considers real application of TIM needs to be extracted to ensure the FO-EB-T (Fan-Out Embedded Bridge with TSV) package thermal performance. In order to achieve this purpose, junction-to-case thermal resistance (Θ_{JC}) measurement of large lidded FCBGA thermal test vehicle (TTV) is firstly measured to ensure the silicon based/graphite/alloy based TIMs thermal performance with liquid-cooling test fixture. Scanning acoustic tomography (SAT) and destructive physical analysis (DPA) are measured to check the TIM coverage and bond line thickness (BLT). Then, thermal conductivity which considers the interface effect is calculated by heat transfer equation using Θ_{JC}, TIM coverage and BLT results. After extracting the thermal conductivity from the TTV measurement, a thermal simulation is constructed to ensure thermal behavior of the large lidded FO-EB-T test vehicle with the liquid cooling system using FloTHERM.

Finally, the mechanical performance of the FO-EB-T is simulated by ANSYS to check the warpage and stress behavior. The structural material optimization is proposed to ensure the package warpage performance while reducing the chip module epoxy molding compounds (EMC) stress risk.

Overall, the paper proposes a method that can extract the thermal conductivity of TIMs in real application. And further ensure not only the thermal performance but also mechanical behavior of large lidded FO-EB-T by thermal and mechanical simulation. Above that, the FO-EB-T package development that can save the design of experiments (DOE) and the thermal behavior consider real application are being proposed.

Key words

Heterogeneous, TIM, FO-EB-T, TTV, Warpage, Thermal, Reliability

I. Introduction

The homogeneous and heterogeneous Chip-on-Wafer-on-Substrate (CoWoS) packages are widely used to achieve high-end products such as artificial intelligence (AI) and high-performance computing (HPC), as well as Co-Packaged Optics (CPO), due to CoWoS-S outstanding high

transmission rate. However, large package and chip module sizes may lead to low yield problems and mechanical issues for silicon interposers.

The Fan-Out Embedded Bridge with TSV (FO-B-T) package is used to replace the CoWoS-S package because its organic interposer offers a high degree of process flexibility and lower cost [1]. For example, to achieve better workability during the chip module fabrication process, we can minimize the coefficient of thermal expansion (CTE) mismatch effect through a DOE matrix using organic compound materials to optimize wafer warpage results [2].

Although FO-EB-T has higher process controllability, package warpage, reliability, and thermal performance remain issues that must be addressed for large-size packages. Typically, high package warpage can be mitigated by using high-stiffness heat spreaders, such as forged or stamped types. However, reliability and thermal problems may arise after adopting high-stiffness heat spreaders. In publication [3], the risk of compound cracking is highlighted as a reliability concern, necessitating the use of low CTE substrate core materials to reduce stress. Regarding thermal issues, publication [4] pointed out that additional heat spreader structures can lead to higher junction temperatures compared to exposed die structures. To resolve this problem, high thermal conductivity thermal interface materials (TIMs) must be utilized. Publication [5] compared the thermal performance between lidded and exposed structures of FO-EB-T, showing that the thermal performance of the lidded structure without high thermal conductivity TIM is inferior to that of the exposed die structure. Therefore, the thermal conductivity of high-performance TIM, considering real application effects, needs to be carefully extracted to address the thermal problem.

In this research, alloy-based TIM is used to achieve optimal thermal performance. Additionally, two standard TIMs (silicon-based and graphite) are adopted to ensure the performance of the alloy-based TIM. Thermal conductivity is first extracted through Θ_{JC} measurement using the large FCBGA-based TTV [6]. Then, the SAT and DPA results are used to calculate real thermal performance, considering real applications through the heat transfer equation. Finally, thermal and mechanical simulations are constructed to predict the behavior of the FO-EB-T structure.

II. TTV and Measurement

A. Thermal Test Vehicle

In this case, the package size of the 77.5 mm x 77.5 mm FCBGA-based TTV contains a 24.9 mm x 24.9 mm thermal die with a 10x10 array of thermal cells. The structure is shown in Fig. 1. A 2 mm thick heat spreader is assembled onto the thermal die. Each thermal cell is equipped with a sensor and a heater, resulting in a total of 100 sensors and 100 heaters in this TTV, as shown in Fig. 2. A uniform power of 100 W is applied in this case. A thermal test board is also mounted beneath the TTV.

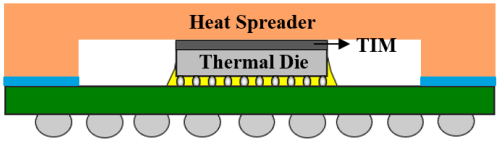


Fig 1. TTV structure

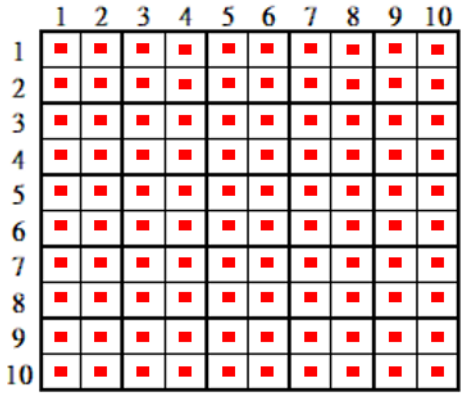


Fig 2. Thermal die (100 sensers)

B. Measurement Fixture

The TTV, along with the thermal test board, is upside down and plugged into a liquid-cooling fixture, as shown in Fig. 3. It is secured in place with a 45-psi pneumatic rod to hold the measuring object. The top surface of the TTV is attached to the cooling plate, which uses 20°C water through TIM2. A 1.5-mm hole is drilled to accommodate a K-type thermocouple for measuring the case temperature at the center of the package.

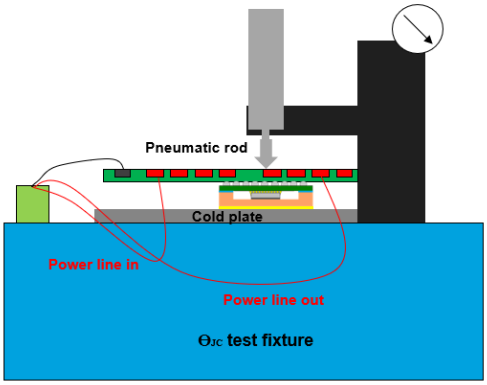


Fig 3. Liquid-cooling test fixture

C. *Thermal Resistance*

ΘJC represents the thermal resistance from the die to the package top surface. The equation is shown in (1). Tj represents the maximum junction temperature (°C) of the die, Tc represents the temperature (°C) at the center of the package top, and P represents the input power (W). In this case, P is set to 100 W.

$$\theta_{JC} = \frac{T_j - T_c}{P} \quad (1)$$

III. Results Analysis

As previously mentioned, three types of TIMs are used in this study: silicon-based, graphite, and alloy-based. The first two are used as control groups to ensure the thermal performance of the alloy-based TIM. The thermal conductivity ratios provided by the vendor are shown in Table I.

Table I. TIM thermal conductivity

TIM type	Silicon based	Graphite	Alloy based
Thermal Conductivity Ratio	1.0X	5.1X	19.5X

For bulk material thermal performance, the alloy-based TIM performs 19.5 times better than the silicon-based TIM and 3.8 times better than the graphite TIM. However, real applications must consider interface effects, such as contact resistance. If we directly use this data to simulate the thermal performance of the package, it will lead to an overestimation of the high thermal conductivity TIM. Therefore, the thermal conductivity that accounts for real application effects must be extracted carefully.

In the FCBGA type TTV, the ΘJC includes the thermal resistance of the die, TIM, and heat spreader, as shown in Fig. 4. To obtain the thermal resistance of the TIM, which includes interface effects, ΘJC must be deducted from the sum of the thermal resistances of the die and heat spreader. The results are shown in Table II. Note that there are three samples for each TIM, and the average ΘJC was taken.

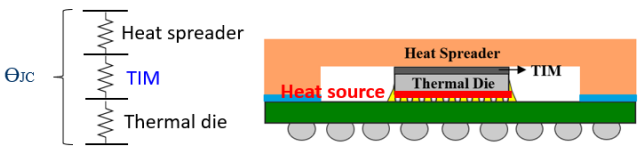


Fig 4. Thermal resistance of TTV

Table II. Measurement results and calculations

TIM type	Sample No.	ΘJC (°C/W)	Avg. ΘJC (°C/W)
Silicon based	1	0.101	0.107
	2	0.104	
	3	0.121	
Graphite	1	0.026	0.039
	2	0.041	
	3	0.050	
Alloy based	1	0.010	0.009
	2	0.010	
	3	0.008	

After ΘJC extraction, the thermal resistance of thermal die and heat spreader are measured through thermal resistance tester separately. The results are shown in Table III.

Table III. Thermal resistance of die and heat spreader

Item	Thermal die	Heat spreader
Thermal resistance (°C/W)	0.0005	0.002

Then, the thermal conductivity of the TIM, which includes interface effects, is calculated using the heat transfer equation with results from SAT and DPA as shown in equation (2). R represents the thermal resistance (°C/W), L represents the TIM bond line thickness (BLT) in micrometers (μm), K represents the TIM thermal conductivity (W/m·K), and A represents the TIM coverage area (m²). The SAT and DPA results are presented in Table IV. The silicon-based TIM coverage from SAT is approximately 70%, with a BLT of around 80 μm. The graphite TIM coverage is about 65%, with a BLT of approximately 90 μm. The alloy-based TIM coverage is around 95%, with a BLT of about 300 μm.

Finally, the thermal conductivity, including the interface effect, is summarized in Table V. Compared to the bulk thermal conductivity, the silicon-based and graphite TIMs are reduced by around 40%, while the alloy-based TIM shows an insignificant difference from the bulk thermal conductivity due to the formation of intermetallic compounds at the interfaces.

$$R = \frac{L}{K \times A} \quad (2)$$

Table IV. SAT and DPA results

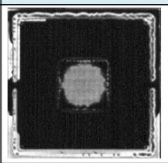
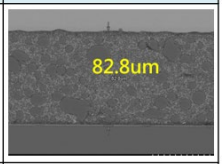
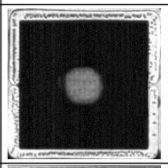
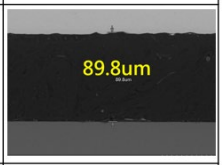
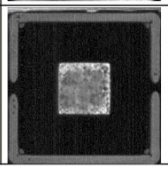
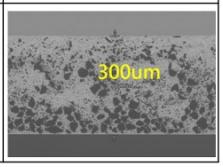
TIM type	SAT	DPA
Silicon based		
Graphite		
Alloy based		

Table V. Thermal conductivity comparison

Type	Silicon based	Graphite	Alloy based
Bulk	1.0X	5.1X	19.5X
Calculation	0.6X	3.1X	19.1X

IV. Thermal Simulation

After extracting the thermal conductivity, a thermal simulation that considers real applications was constructed using FloTHERM to evaluate the thermal performance of FO-EB-T. The structure is shown in Fig. 6. It contains three top dies connected to three embedded dies in series. The chip module consists of a 2-layer RDL between the top die and the embedded die. The package size is set at approximately 5000 mm² [5].

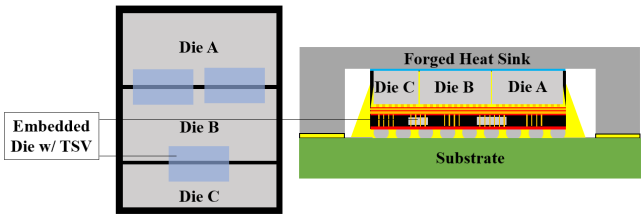


Fig 6. FO-EB-T structure

In this case, the ΘJC criteria should be lower than 0.05 °C/W. The simulation results are compared in Table VI, which shows that the graphite TIM can meet the ΘJC criteria when using the bulk thermal conductivity. However, after using the thermal conductivity data obtained from measurements, the ΘJC exceeds the criteria, necessitating the adoption of the alloy-based TIM to meet the requirements.

Table VI. Thermal simulation results

ΘJC (°C/W)	Type	Silicon based	Graphite	Alloy based
	Bulk	0.171	0.035	0.001
	Calculation	0.285	0.058	0.001

V. Warpage and Reliability Simulation

The warpage and reliability simulations are conducted using ANSYS Mechanical after the alloy-based TIM is selected from the thermal simulation. According to research [3], EMC cracking is the most common failure mode in the FO-BE-T package. The cracks are caused by stress concentration at the corners of the top die, as shown in Fig. 7.

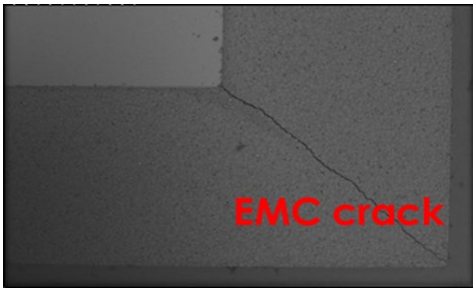


Fig 7. EMC Crack [3]

The simulation results are shown in Table VII, where a '+' indicates convex warpage and a '-' indicates concave warpage. From the simulation results, the EMC stress is larger than the stress baseline, which indicates that the device has already passed a reliability test. The warpage performance, however, is within the warpage criteria. In this situation, when we change the substrate core material from high CTE to low CTE, the stress is lower than the stress baseline, and the warpage performance is even better.

Table VII. Warpage and reliability simulation results

Core CTE	Package warpage RT/HT(um)	EMC stress ratio
High	+115/-56	1.13X
Low	+94/-43	0.94X

VI. Conclusion

In this research, a method for extracting the appropriate thermal conductivity, which includes real applications, has been proposed using TTV ΘJC measurements. The results indicate approximately a 40% reduction in thermal conductivity compared to the data provided by the vendor. If

the vendor's data is used directly, the thermal simulation results will be overestimated, potentially leading to thermal issues.

Package warpage and reliability simulations were conducted after the thermal simulation. The results show the necessity of using low CTE substrate core material to address the significant stress problem.

Through simulation, this study offers a solution for a high thermal performance FO-EB-T package. Based on these findings, DOE can be utilized to reduce costs and also aid in the future development of FO-EB-T packages.

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