Novel Thin Dry Film Photoresist and Process Optimization for Ultra-Fine Patterning

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Abstract

We have developed a novel dry film photoresist capable of forming ultra-fine wiring for advanced semiconductor packages. Using laser direct imaging exposure, we successfully formed post-development patterns with line and space, L/S = 1.2 µm/1.2 µm (1:1) and L/S = 1.0 µm/3.0 µm (4 µm pitch). Furthermore, we also succeeded in forming copper wiring patterns after electrolytic plating with L/S = 1.5 µm/1.5 µm. As far as we know, these results are the most outstanding for ultra-fine pitch and they can contribute to the future production of 2.xD panel-level packages.

Key words

Advanced semiconductor package, Dry film photoresist, Laser direct imaging exposure, Panel-level package

I. Introduction

In the past, semiconductor performance improvements have been driven by the miniaturization of transistors in the front-end process. On the other hand, in recent years, with the adoption of advanced semiconductor packaging that enables high-speed connections between logic and memory dies, the back-end process technologies for enhancing semiconductor performance are gaining attention. With the recent expansion of the generative AI market, the number of advanced semiconductor packages for high-performance AI-related products tends to be increased. In particular, the 2.xD packages, in which dies are connected through an interposer, are expected to be a future trend [1], [2], and silicon wafers typically used for interposers. However, silicon wafers are restricted in terms of the large substrate production, and RDL interposers with organic insulating resin layer are attracting attention [3], [4]. Examples of package structures using RDL interposers include CoWoS-R [5] and i-THOP [6]. RDL interposers with fine wiring with less than L/S= 2/2 µm have the potential to be produced in large size by the panel process, and a shift from conventional liquid photoresists (LPR) to dry film photoresists (DFR) is expected for wiring formation materials (Fig. 1) [7]. Compared to LPR, DFR offers advantages such as being free from edge bead formation, the ability of inorganic alkaline development, and the capability of double-sided processing, which means it is difficult to process the front and back sides of substrate at the same time.

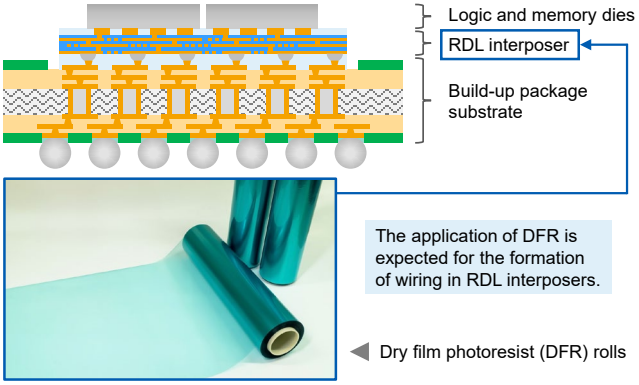

Fig. 1 The schematic image of 2.xD package and the appearance of dry film photoresist roll

The size of the interposer needs to be expanded due to the increase in both logic and memory dies [5]. There are currently two main types of exposure methods. One is called the stepper method, which uses a reticle to repeatedly expose patterns through projection exposure. Since the same reticle is exposed by utilizing stitching, this method is superior in pattern reproducibility and is widely used in the semiconductor field. The other is called direct imaging (DI), which uses a laser to expose patterns without a reticle. This method is characterized by the absence of a reticle and the ease of alignment. DI exposure machines are applied to mass production lines of substrate manufacturers.

In this paper, we evaluated the formation of fine DFR patterns with less than L/S=2/2 µm, mainly targeting the h-line DI exposure process.

II. Materials and Methods

To meet the requirements for DI exposure and high resolution, we developed a novel DFR, TA-1. The resist, formed from a negative-type photosensitive resin composition, was coated onto a PET film as a carrier film, under optimized coating conditions. After drying, an oriented polypropylene film was laminated as a cover film, and we successfully produced TA-1 in roll form. The resist thickness was measured as 7 µm. The TA-1 roll was slit to a width of 500 mm and used in the following evaluations.

A. Evaluation of Resolution after Development

After removing the cover film, TA-1 was laminated onto a 170 mm x 130 mm build-up film panel with a 0.5 µm thick electroless copper layer. The test panel was designed as a practical FC-BGA substrate, and the panel surface roughness Sa after electroless plating was approximately 0.1 µm. The lamination was performed using a hot roll laminator under the following conditions: preheat temperature of 50 deg.C, roll temperature of 105 deg.C, pressure of 0.34 MPa and speed of 1.5 m/min. Subsequently, the laminated panel was exposed under optimal focus conditions with various exposure doses using a DI exposure machine (SDi, manufactured by ORC Manufacturing Co.,Ltd.). Here, two types of evaluation patterns were prepared: one with a L/S ratio of 1:1, and another with a total pitch of 4 µm, with dimensions prepared in 0.1 µm increments. After exposure, post-exposure baking (PEB) was performed on a hot plate at 50 deg.C for 60 seconds. Then the carrier film was peeled off, and development and water rinsing were carried out under the following conditions: developer of 1 wt% Na_2CO_3 aqueous solution, temperature of 30 deg.C, spray pressure of 0.15 MPa and actual processing time was set to twice the minimum development time. The resolution and the line width of the resulting TA-1 pattern were measured using an optical microscope and SEM (S-3400N, manufactured by Hitachi High-Tech Corporation). Similar evaluations were conducted in the case of using an i-line stepper.

B. Fabrication of electrolytic copper plating patterns

Electrolytic copper plating using a semi-additive process was applied to the patterned panel of TA-1 obtained by the same procedure as described above. First, as a pretreatment, O_2 plasma treatment was performed for 60 seconds using an ashing instrument (NA-8000, manufactured by ULVAC, Inc.), followed by 60 seconds dip treatment in dilute sulfuric acid. Subsequently, electrolytic copper plating was conducted using a copper sulfate plating solution, followed by rinsing and drying. The plating conditions were temperature of 25 deg.C, current density of 3 ASD, and a duration of 8-9 minutes. After plating, the panel was applied to a stripping process using a stripper containing amine compounds at 50 deg.C for 1 minute, followed by rinsing and drying to obtain the electrolytic plated copper wiring pattern. The resolution and line width of the resulting wiring pattern were evaluated using an optical microscope and SEM.

III. Results and Discussion

A. Evaluation of Resolution after Development

To achieve high resolution, we optimized the process. We evaluated exposure doses of 140, 160, 180, and 200 mJ/cm² using an h-line DI exposure machine. As a result, the best resolution of the TA-1 (7 µm thick) pattern was obtained at 180 mJ/cm² (Table 1). For the pattern design with a L/S ratio of 1:1, we achieved L/S = 1.3 µm/1.3 µm (aspect ratio of 5.4), and for the design with a 4 µm pitch, we achieved L/S = 1.1 µm/2.9 µm (aspect ratio of 6.4). Furthermore, we examined line width compensation. In DI exposure, it is possible to pre-adjust the line width of the drawing design. After investigating the range from -0.2 µm to -0.8 µm, we found that the optimal compensation value of -0.6 µm gave the best resolution (Fig. 2). As shown in Fig.3, SEM observations of the TA-1 pattern shape revealed excellent line edge roughness and short resist foot. In contrast, exposure at 140-160 mJ/cm² showed pattern deformation due to insufficient curing, while exposure at 200 mJ/cm² led to increased line width and poor resolution, causing residue between patterns.

Table 1 Evaluation results of resolution after development

		TA-1	TA-2
DFR thickness	[µm]	7	7
Breaking point (B.P.)*	[sec]	16	23
Exposure dose	[mJ/cm^2]	180	80
Resolution (L/S ratio of 1:1)	[µm]	1.3 / 1.3	1.2 / 1.2
Resolution (4 µm pitch)	[µm]	1.1 / 2.9	1.0 / 3.0

*The minimum time when the unexposed DFR is completely developed.

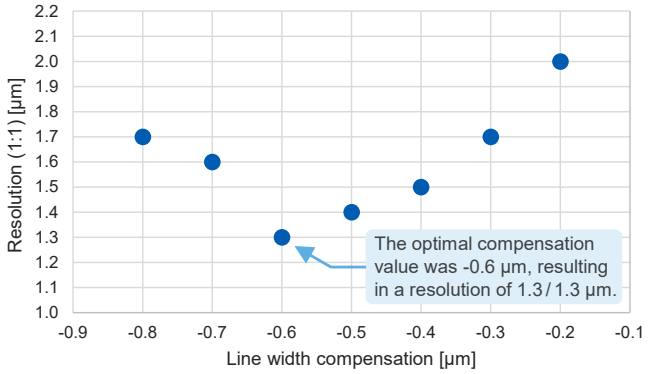

Fig. 2 The optimized results of line width compensation

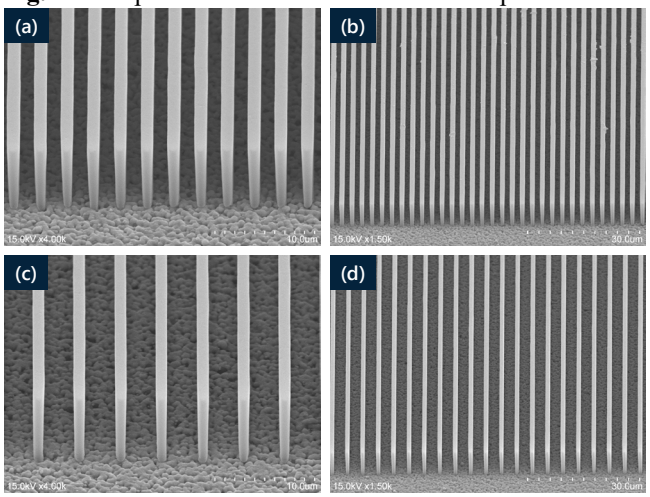

Fig. 3 SEM images of the DFR pattern of TA-1 after development by h-line DI exposure machine: (a) L/S = 1.3 µm/1.3 µm, magnification x4,000, (b) L/S = 1.3 µm/1.3 µm, x1,500, (c) L/S = 1.1 µm/2.9 µm, x4,000, (d) L/S = 1.1 µm/2.9 µm, x1,500.

Furthermore, to achieve a higher resolution of the developed DFR pattern, we prepared sheet samples of a new DFR, TA-2 (7 µm thick) with an improved resist composition and evaluated them under the same conditions as those used for TA-1. As a result, we obtained a highly sensitive DFR pattern at 80 mJ/cm². For the pattern design with a L/S ratio of 1:1, we achieved L/S = 1.2 µm/1.2 µm (aspect ratio of 5.8), and for the design with a 4 µm pitch, we achieved L/S = 1.0 µm/3.0 µm (aspect ratio of 7.0). As shown in Fig. 4, SEM observations of the TA-2 pattern shape confirmed excellent line linearity.

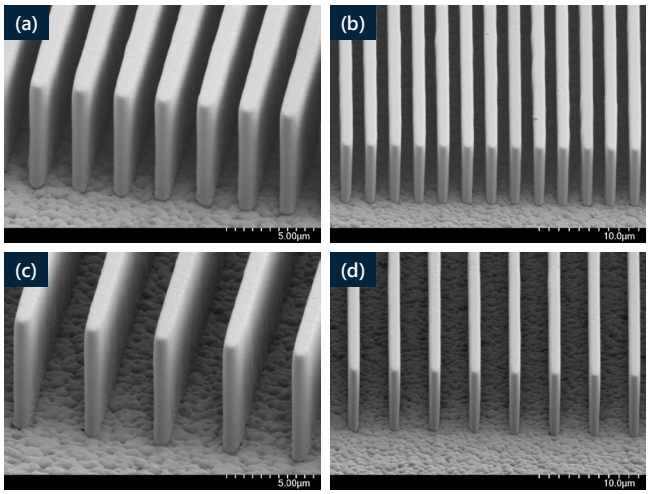

Fig. 4 SEM images of the DFR pattern of TA-2 after development by h-line DI exposure machine: (a) L/S = 1.2 µm/1.2 µm, diagonal view, (b) L/S = 1.2 µm/1.2 µm, front view, (c) L/S = 1.0 µm/3.0 µm, diagonal view, (d) L/S = 1.0 µm/3.0 µm, front view.

Additionally, we evaluated the resolution of the TA-1 patterns obtained by exposure using an i-line stepper. As shown in Fig. 5, we achieved L/S = 1.6 µm/1.6 µm for the 1:1 pattern and L/S = 1.4 µm/2.6 µm for the 4 µm pitch pattern with an exposure dose of 130 mJ/cm². We confirmed that TA-1 is capable of forming fine patterns at both h-line and i-line wavelengths. Furthermore, we were able to form L/S = 1.6 µm/1.6 µm and L/S = 1.4 µm/2.6 µm patterns on wafers with a copper sputter layer on the surface. This result suggests that DFR can be applied even on substrates with lower surface roughness.

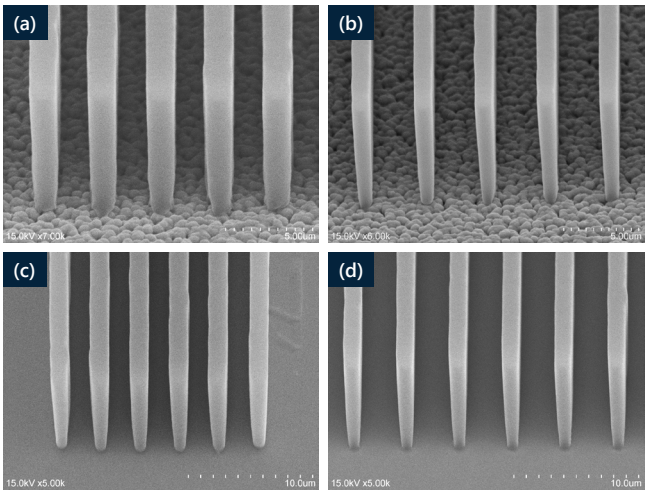

Fig. 5 SEM images of the DFR pattern of TA-1 after development by i-line stepper: (a) L/S = 1.6 µm/1.6 µm with build-up film panel, (b) L/S = 1.4 µm/2.6 µm with build-up film panel, (c) L/S = 1.6 µm/1.6 µm with copper sputtered wafer, (d) L/S = 1.4 µm/2.6 µm with copper sputtered wafer.

B. Fabrication of electrolytic copper plating patterns

To confirm the wiring formation capability, we evaluated the electrolytic copper plating and DFR stripping using TA-1 patterns obtained by h-line DI exposure. As shown in Fig. 6, we successfully formed copper wiring with L/S = 1.5 µm/1.5 µm and the thickness was approximately 4 µm. For fine patterning, the stripping of DFR tends to be difficult, but no DFR residue was observed between the wiring patterns. We also observed the cross-sectional SEM images of the wiring patterns and confirmed that there was no TA-1 residue at the interface between the seed layer and the electrolytic copper. In addition, we successfully formed copper wiring with L/S = 3.0 µm/1.0 µm, considering the side etching due to the flash etching process for seed layer removal. Although the spaces between the copper patterns were narrower, a well-defined shape was still obtained. Additionally, the flash etching process successfully enabled the formation of wiring with L/S = 2/2 µm.

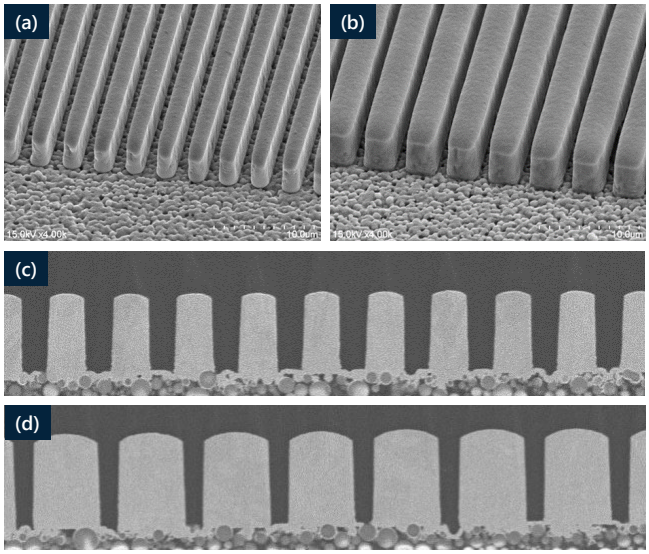

Fig. 6 SEM images of the electrolytic copper wiring pattern using TA-1: (a) L/S = 1.5 µm/1.5 µm, overhead view, (b) L/S = 3.0 µm/1.0 µm, overhead view, (c) L/S = 1.5 µm/1.5 µm, cross-sectional view, (d) L/S = 3.0 µm/1.0 µm, cross-sectional view.

IV. Conclusions

As a result, we successfully formed ultra-fine DFR patterns with L/S = 1.2 µm/1.2 µm and L/S = 1.0 µm/3.0 µm using a novel DFR and DI exposure method. As far as we know, these are the best results under the conditions of DFR and DI exposure. The ability to form high-resolution fine patterns on the panels using build-up film brings us significantly closer to practical application. We believe these results can contribute to the increase in Cu wiring density and large substrate production of advanced packages.

Acknowledgment

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