Wafer Level Substrates with Si-Core and Hybrid Organic/Inorganic Interconnect

Steven Verhaverbeke, Han-Wen Chen, Suresh Ramalingam
Applied Materials
33225 Oakmead Village Dr MS1240
Santa Clara, CA 95054 USA
Ph: 408-398-2587
Email: steven_verhaverbeke@amat.com

Vineeth Harish, Subramanian Iyer
UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS
Los Angeles, CA, USA

Abstract

The relentless drive toward higher bandwidth, lower latency, lower power has driven interconnect technologies on substrates that yield small linewidth for signal die-to-die coupled with larger linewidth and thicker Cu lines for power delivery and small pitch assembly. Traditionally this was achieved by using a silicon interposer with small linewidth mounted on a laminate substrate with thick Cu lines for power in a 2.5D integration approach. However, this method introduces additional interconnect layers, parasitics and cost constraints while limiting interposer size. Our results show that a single silicon core substrate can effectively replace both the laminate and the Si interposer by combining a hybrid organic/inorganic interconnect. Moreover dies can now be assembled at <10um pitch using a solderless Cu-Cu thermocompression bonding scheme.

Key words

Substrates, Wafer Level, Si-core, 2.5D, Hetergeneous Integration

I. Introduction

The rise of chiplet and 2.5D packaging has been driven by the increasing demands for higher performance, scalability, and power efficiency in modern semiconductor design. As Moore's Law slows, traditional monolithic scaling becomes less viable due to cost and yield challenges. Chiplet-based architectures address these limitations by enabling modular integration of heterogeneous dies, allowing manufacturers to mix and match different process nodes and functionalities within a single package. 2.5D packaging, which utilizes an interposer to connect multiple chiplets, has emerged as a key enabler by providing high-bandwidth, low-latency interconnects while mitigating signal integrity and power delivery challenges [1], [2], [3], [4]. This approach is widely adopted in AI accelerators, high-performance computing (HPC), and networking applications, offering a path to scaling performance without the complexity of full 3D stacking.

2.5D silicon interposer packaging, while enabling high-bandwidth chiplet integration, comes with several limitations and challenges. A primary constraint is reticle size, which restricts the maximum interposer dimensions, limiting scalability for large and complex designs. Testing is another major hurdle, as the added interposer layer complicates both wafer-level and package-level testing, making fault isolation and yield optimization more difficult. Reliability concerns arise due to the mechanical stress and thermal expansion mismatches between the interposer, chiplets, and substrate, which can lead to warpage, delamination, and increased failure rates. Signal integrity issues also emerge as longer interconnects, increased parasitic effects and multiple transition layers introduce latency and degrade high-speed signal performance. Additionally, the high cost of silicon interposers—stemming from their complex fabrication, fine-pitch micro bumps, and advanced assembly processes—makes 2.5D packaging an expensive solution. These challenges drive the search for alternative approaches, such

as silicon core substrates, which aim to simplify integration while improving performance, yield, and cost efficiency.

A single multilayer silicon core substrate offers several advantages over traditional 2.5D interposer packaging by streamlining integration, improving performance, and reducing costs. Unlike silicon interposers, which are limited by reticle size and introduce additional interconnect layers, a multilayer silicon core substrate allows direct high-density routing of chiplet connections without the need for a separate interposer. This reduces signal integrity issues by minimizing interconnect length, lowering parasitics, and improving power delivery. Reliability is also enhanced, as eliminating the interposer reduces mechanical stress, thermal expansion mismatches, and potential failure points. Additionally, testing and manufacturability are simplified, as the silicon core substrate supports direct integration of chiplets, improving yield and fault isolation. Cost efficiency is another key benefit, as removing the silicon interposer reduces fabrication complexity and assembly steps, leading to lower overall packaging expenses. This approach enables scalable, high-performance chiplet architectures while overcoming the limitations of traditional 2.5D integration.
The traditional 2.5D package is illustrated in Figures 1, 1-4, 1-5, and 1-6 of the UCIe specification [5].
The combination of an organic substrate and a silicon or RDL interposer with silicon inserts (bridges) provides the following capabilities:

1. High-density, short-reach local interconnect within the silicon interposer or silicon bridges.
2. Thick copper lines in the organic substrate for high-current power delivery.
3. Thick dielectric in the organic substrate enables long-reach differential pair communication at high frequencies with low insertion loss.

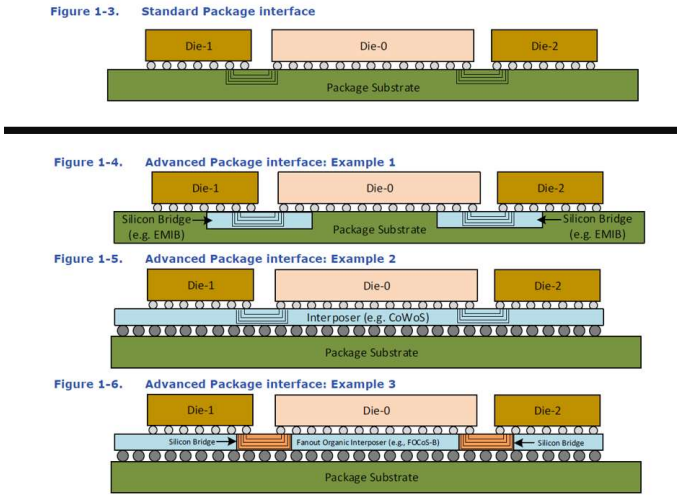

Fig. 1. Packaging Options as outlined in the UCIe spec [5].

However, the current generation of organic substrates and their combination with silicon interposers face several limitations in meeting the evolving demands of high-growth market applications. First, this approach introduces significant parasitic effects due to the multiple interconnect levels (PCB–organic substrate–silicon interposer) and the presence of through-silicon vias (TSVs) in the silicon interposer. These parasitics degrade power supply quality and cause voltage ripple. Second, the method is highly expensive, requiring numerous unit process steps and complex assembly procedures, including the use of carriers and their bonding/debonding steps.

II. Wafer Level Substrates

In this paper, we propose a novel substrate made with Si wafers as the core. This new approach enables a dual-sided build-up on both sides of the Si core, enhancing integration and performance. These new substrates are targeting emerging technologies like artificial intelligence, advanced telecommunications and autonomous vehicles.
This approach was recognized by the National Advanced Packaging Manufacturing Program (NAPMP), which selected the Si-Core substrate, as outlined in this paper, as one of three technologies awarded funding [6]. The NAPMP is supporting semiconductor packaging research and development as part of the U.S. CHIPS Act.

Si as the core material is replacing the conventional core which is made up of glass fiber epoxy. The manufacturing process starts with a Si 300mm wafer. The thickness can be anywhere between 100um and 775um thick. A standard 300mm wafer is 775um thick and can be ground and/or polished to the desired thickness or can be used at full thickness as is. We have demonstrated through full thickness Si drilling. All processing is done with a free-standing wafer, i.e. without any carrier, and both sides are being processed. The base Si wafer can be bare or can have additional features for embedding, such as trench capacitors, or a GaN device layer with HEMT devices for voltage regulation, or embedded cooling channels.

In the first process module, the through vias are made by a process of (i) laser through drilling, (ii) epoxy based organic dielectric filling, (iii) via-in-via epoxy laser drilling, (iv) electroless Cu seed plating on the epoxy sidewalls and (v) lithography and Cu plating. This process enables vias through the Si for the targeted range of thicknesses.

Figure 2 shows an example of this through via on a 300um thick Si wafer plus 60um epoxy dielectric (30um on top and 30um on bottom). The wafer with total thickness of 360um can be handled without any carrier wafer. This process is a substantial improvement over traditional Si interposers which are typically limited to 100um thickness because of

the blind TSVs and PVD seeded metallization and are only processed single sided.

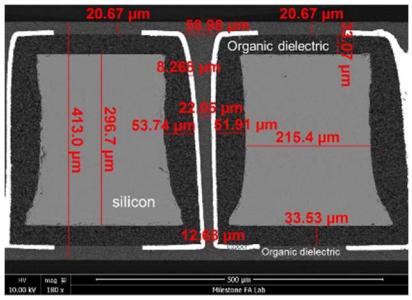

Fig. 2. Through Si-Core vias in 300um thick Si+ 60um epoxy = 360um via total length.

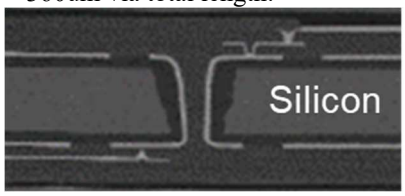

Fig. 3. Dual sided Si-Core substrate with 3 interconnect layers on top and 3 interconnect layers on bottom.

.

Following the through via formation, the organic interconnect layers are build-up simultaneously on both sides and balanced to avoid any warpage. An example of a dual sided Si-Core substrate is shown in Figure 3. The organic layers provide connections for power delivery, for long-range cross-substrate communcaiton and through the Si Core.

Many features can be added as shown in Figure 4. This includes the Si-Core, the laser through vias, the embedded passive and/or active devices, the embedded cooling, the organic build-up, even inorganic build-up and the chiplet attachment. Note that, in the Si core, embedded featrues can be built-in includding Si-trench capacitors, GaN epitaxial device layer with HEMT power switches, embedded capacitors, GaN HEMT dies, embedded inductors, embedded waveguides, and embedded cooling channels.

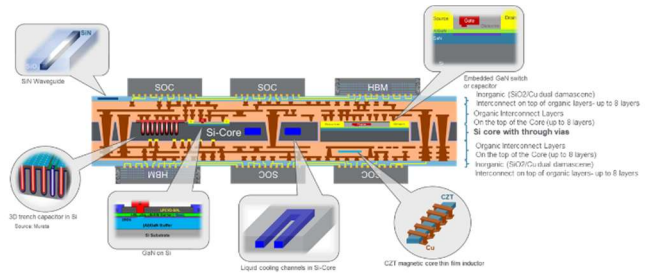

Fig. 4. Graphical Reprensation of Si-Core substrate with all the features added.

III. Inorganic Interconnect on top of organic

The Si-If platform developed by UCLA applies damascene BEOL techniques in SiO2 for fine-pitch routing [7]. This allows heterogeneous dies to be assembled at sub-10 µm pitch with solderless thermocompression bonding (TCB) through Cu-Cu [8], circumventing many of the challenges inherent in solder-based interconnects and organic packages [9]. Since organic polymer wiring layers remain pivotal for supporting thicker Cu traces, our strategy has been to deposit the inorganic dielectric layers on top of the organic wiring layers and terminating them with copper pillars in SiO2 for direct solderless Cu-Cu TCB without the inclusion of an interposer. The inorganic layers were deposited on the organic layers with a low temperature inorganic CVD deposition process.

An important focus of the hybrid substrate is the enablement of fine pitch assembly (≤ 10µm). In prior work [10], the feasibility of Cu-Cu TCB on a hybrid layer was explored as seen in Fig. 5. Based on the results in [10] it was observed that a tack and gang anneal approach could be used to improve throughput and achieve higher bond quality. With the organic layers below, it is important to lower the temperature for anneal to be suitable for the hybrid substrate (thermal budget of 250-300°C) while ensuring a similar level of bonding reliability.

A tacking time of 15s was used with an interface temperature of 250°C along with an in-situ Formic Acid clean to reduce copper oxides and maintain a pristine bonding interface. Next each sample was placed in a wafer to wafer bonder where no pressure was applied and it was annealed under high vacuum at a fixed time.

The results for the anneal temperature variation experiments revealed that a temperature of 240°C and 4 hr is sufficient.

Figure 6 shows a FIB cross section of the final assembly after a 4 hour 240°C anneal.

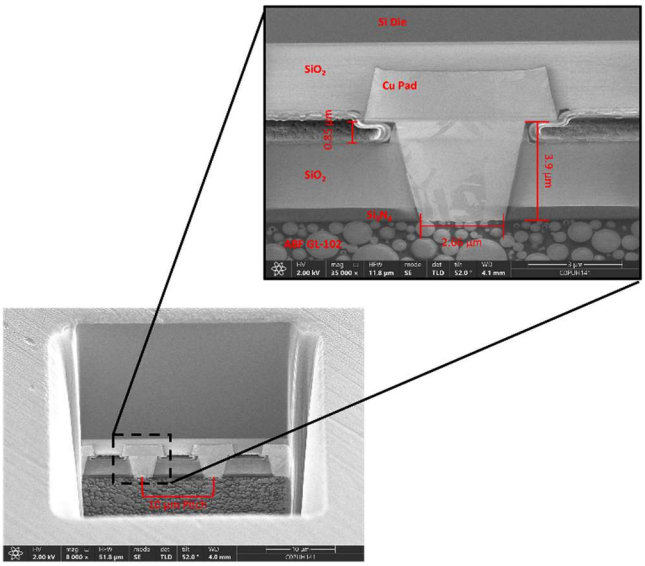

Fig. 5. Cross Section of the bonded die at 10um pitch with direct Cu-Cu TCB assembly.

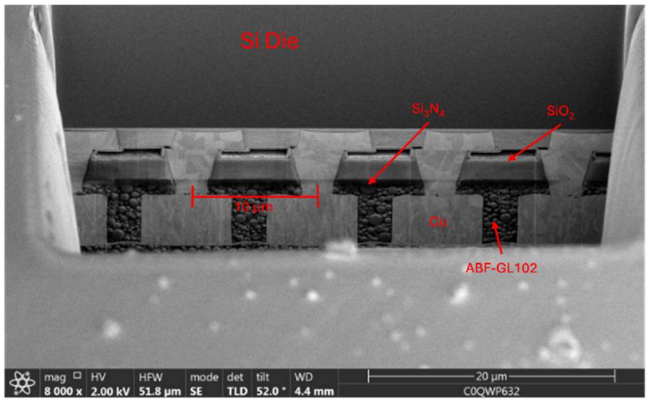

Fig. 6. Cross Section of final assembly after a 4 hr 240C anneal (with some slight misalignment).

IV. Conclusion

Wafer Level Substrates are a new class of substrates, called out by the NAPMP as the highest density substrates. Wafer Level Substrates can offer densities normally only available on Si Interposers and Si inserts/bridges in RDL Interposers. In this work we show how these substrates are using both organic and inorganic interconnect by depositing the inorganic interconnect on top of the organic interconnect, resulting in a hybrid wiring layered substrate. The organic interconnect is made with semi-additive copper traces and embedded in organic polymer dielectrics. The inorganic layers are deposited with low temperature CVD and the Cu traces in the inorganic layers are formed with a damascene process. In addition such a substrate can be employed for direct Cu-Cu TCB bonding of dies which was demonstrated at a 10um pitch. We believe that these findings provide critical insights and offer a significant step towards the adoption of hybrid structures in next-generation high-density electronic packaging applications.

References

[1] Farhang Yazdani, John Park, "Pathfinding and Design Optimization of 2.5D/3D devices in the context of multiple PCBs," *IMAPS 10th International Conference on Device Packaging*, March 10-13, 2014, Fountain Hills, AZ, USA, pp. 294-297.

[2] Farhang Yazdani, John Park, "Pathfinding Methodology for Optimal Design and Integration of 2.5D/3D Interconnects," *Proceedings of the 64th IEEE Electronic Components and Technology Conference*, Orlando, Florida, May 26-30, 2014.

[3] Farhang Yazdani, "A novel low-cost high performance and reliable silicon interposer", 2015 IEEE Custom Integrated Circuits Conference (CICC), pp. 1-6, 2015.

[4] John Park, "Pathfinding for Multiple Platforms," *IMAPS 10th International Conference on Device Packaging*, March 10-13, 2014, Fountain Hills, AZ, USA, pp. 298-300. .

[5] Universal Chiplet Interconnect Express (UCIe) Specification, July 10, 2024, Revision 1.1., Version 1.0

[6] https://www.commerce.gov/news/press-releases/2024/11/chips-america-announces-300-million-funding-boost-us-semiconductor.

[7] S. Jangam and S. S. Iyer, "Silicon-Interconnect Fabric for Fine-Pitch (≤10 μm) Heterogeneous Integration," IEEE Trans. Compon., Packag. Manufact. Technol., vol. 11, no. 5, pp. 727–738, May 2021, doi: 10.1109/TCPMT.2021.3075219.

[8] S. Jangam et al., "Fine-Pitch (≤10 μm) Direct Cu-Cu Interconnects Using In-Situ Formic Acid Vapor Treatment," in 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA: IEEE, May 2019, pp. 620–627. doi: 10.1109/ECTC.2019.00099.

[9] K. Sahoo, V. Harish, H. Ren, and S. S. Iyer, "A Review of Die-to-Die, Die-to-Substrate and Die-to-Wafer Heterogeneous Integration," IEEE Electron Devices Rev., vol. 2, pp. 6–31, 2025, doi: 10.1109/EDR.2024.3501214.

[10] V. Harish et al., "Fine Pitch (≤ 10 μm) Die to Wafer Cu-Cu TCB on Organic Polymer Build Up Films," 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), Denver, CO, USA, 2024, pp. 2178-2183, doi: 10.1109/ECTC51529.2024.00392.

[11]