Panel RDL Interposer or Substrate (PRIS) for a Vertical-Cavity Surface-Emitting Laser (VCSEL)

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Abstract
In this study, the transformation of high-speed electrical signals into optical signals using a glass panel RDL interposer or substrate (PRIS) integrated with a vertical-cavity surface-emitting laser (VCSEL) chip is investigated for co-packaged optics (CPO) applications. Emphasis is placed on the design, fabrication, and electrical and optical characterization of the package. S-parameters simulations are performed and compared with experimental results. In addition, a 56 Gbps PAM-4 optical eye diagram is measured and characterized.

Key words
Panel-level, RDL-first, chip-last, co-packaged optics (CPO), high-speed, heterogeneous integration

I. Introduction
Panel RDL interposer and substrate (PRIS) is a glass-based fan-out chip-last panel-level technology. For PRIS' capability, the minimum line/spacing (L/S), trace thickness, and dielectric thickness are 2/2 µm, 2-5 µm, and 4-6 µm, respectively, which are much finer and thinner than the conventional substrates [1]–[4]. PRIS is suitable for applications such as products driven by artificial intelligence (AI), co-packaged optics (CPO), and others.

In CPO applications, as shown in Fig. 1, an application-specific integrated circuit (ASIC) switch, electronic integrated circuits (EICs), including a transimpedance amplifier (TIA) and a driver, and photonic integrated circuits (PICs), including a photodetector (PD) and a vertical-cavity surface-emitting laser (VCSEL), are interconnected on a substrate [5]–[7]

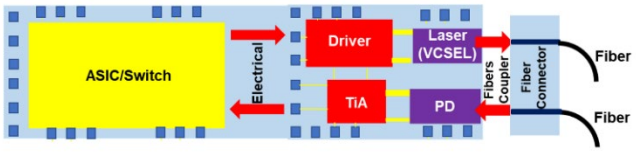

Fig. 1. Heterogeneous integration of key components in CPO.

The objective of this study is to demonstrate the feasibility of the high-density and high-speed glass PRIS with finer trace with a VCSEL, which is a key part of a CPO system. The VCSEL chip is assembled on top of the PRIS to form an optical module package, which can convert electrical signals into optical signals, as shown in Fig. 2.

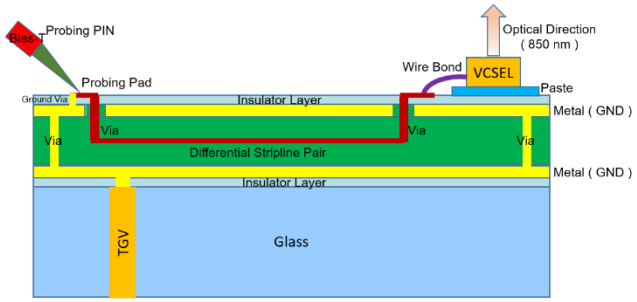

Fig. 2. VCSEL chip assembled on top of the glass PRIS to form an optical module.

Characterizations such as S-parameter measurement using a vector network analyzer (VNA) are conducted to verify the signal integrity of high-speed transmission through the PRIS and gold wire. Electro-optical characteristics, including threshold current, slope efficiency, and forward voltage, are evaluated to compare the performance of the optical package and VCSEL chip itself. In addition, a 56 Gbps PAM-4 optical eye diagram is measured to assess the quality of the optical

signals transmitted through the package. The simulation is performed for S-parameter and impedance matching using the ANSYS HFSS and Q2D software.

II. PRIS

A. Design and Structure

Fig. 3 shows the structure of stripline and microstrip on a glass panel with a thickness of 1.1 mm. The stripline structure, as shown in Fig. 3(a) and 3(b), includes 4-µm-thick ground layers at the first and third metal layers (ML1 and ML3), and a single-lane differential pair at the second metal layer (ML2). For the differential pair, the L/S, trace thickness, and dielectric thickness (above and below the traces) are 6 µm/10 µm, 2 µm, and 6 µm, respectively. As shown in Fig. 3(c) and 3(d), the microstrip includes a ground layer at ML1, and a single-lane differential pair at ML2. For the differential pair, the L/S, trace thickness, and dielectric thickness (below the traces) are 12.4 µm/10 µm, 2 µm, and 6 µm, respectively. Since the focus of this study is on the electrical and optical characteristics of the glass substrate or interposer and the VCSEL, the TGV is not presented in this study.

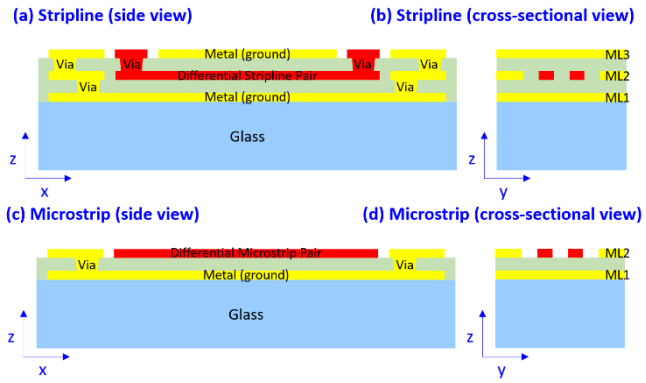

Fig. 3. Structure of stripline and microstrip.

The designs and structures mentioned above result in an impedance of 100 Ω based on the ANSYS Q2D simulation results. The differential pair is designed and fabricated with the length of 5 mm and 10 mm. For the electrical characteristics of the dielectric material in this study, the dielectric constant (Dk) and dissipation factor (Df) are 3.1 and 0.02, respectively.

B. RDL Process

The PRIS is fabricated with dimensions of 510 mm x 515 mm x 1.1 mm, as shown in Fig. 4. Fig. 5 illustrates the process flow of PRIS fabrication using the stripline structure as an example. The fabrication process starts by coating an adhesion promoter and depositing a metal seed layer on a glass panel via physical vapor deposition (PVD). It is followed by photoresist (PR) coating, exposure, development, and Cu plating, then by stripping the PR and etching the seed layer to form ML1. Subsequently, PID coating, exposure, development, and curing are performed to form the dielectric layer between ML1 and ML2 (denoted as D12). The above steps are repeated to form ML2, D23, and ML3. Finally, electroless palladium immersion gold (EPIG) is applied as a surface treatment to protect the metal from oxidation and enhance the bonding of contact pads to bond with gold wires.

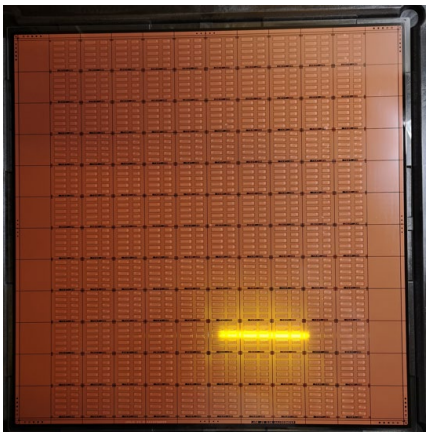

Fig. 4. PRIS fabricated with dimensions of 510 mm x 515 mm x 1.1 mm.

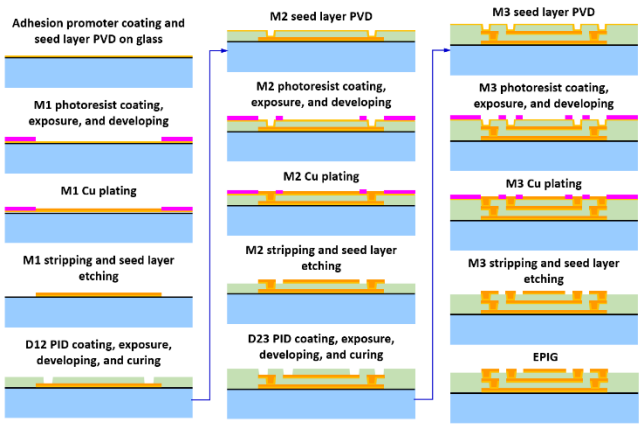

Fig. 5. Process flow of PRIS fabrication.

Fig. 6 shows optical microscope (OM) images of the PRIS from both top and cross-sectional views. For the stripline structure shown in Fig. 6(b), the differential pair L/S and thickness in ML2 are 5.7 µm/10 µm and 2.2 µm, respectively, which are close to the target value (6 µm/10 µm and 2 µm). The thickness of D12 and D23 are measured as 5.1 µm and 4.2 µm, which slightly deviate from the target (6 µm). For the microstrip structure shown in Fig. 6(c), the differential pair L/S and thickness in ML2 are 11.7 µm/10.4 µm and 2.1 µm, respectively, which are close to the target values (12.4 µm/10 µm and 2 µm) The thickness of D12 is 4.7 µm, which also slightly deviates from the target (6 µm).

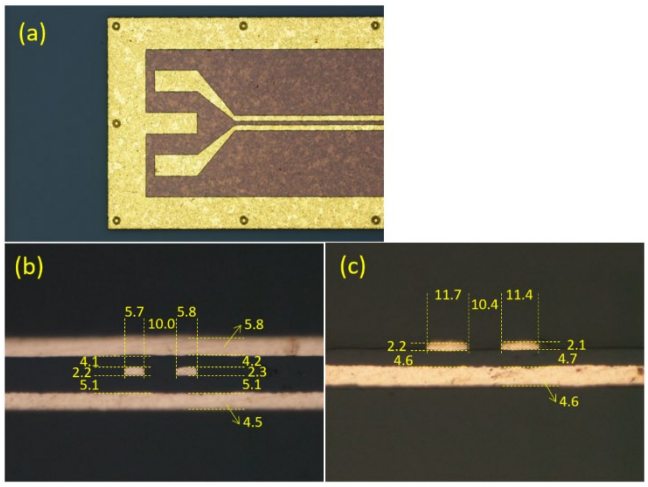

Fig. 6. OM images of the PRIS: (a) Top view; (b) cross-sectional view of the stripline and its dimensions (μm); (c) cross-sectional view of the microstrip and its dimensions (μm).

C. S-parameter Measurement and Simulation

The measured S-parameters using a VNA is compared with the simulated results from ANSYS HFSS, as shown in Fig. 7. For both stripline and microstrip structures, the measured Sdd11 values are below -15 dB, and the Sdd21 values are greater than -4.5 dB up to 26 GHz of frequency (limited by the bandwidth due to the 100 μm pitch of the GSGSG probes). These results suggest that the PRIS not only achieves finer L/S and thinner dielectric compared to conventional substrates but also demonstrates good performance in the high-speed transmission. The deviation in frequency and S-parameter magnitude between measurement and simulation is within 2GHz and 3dB, indicating consistent results.

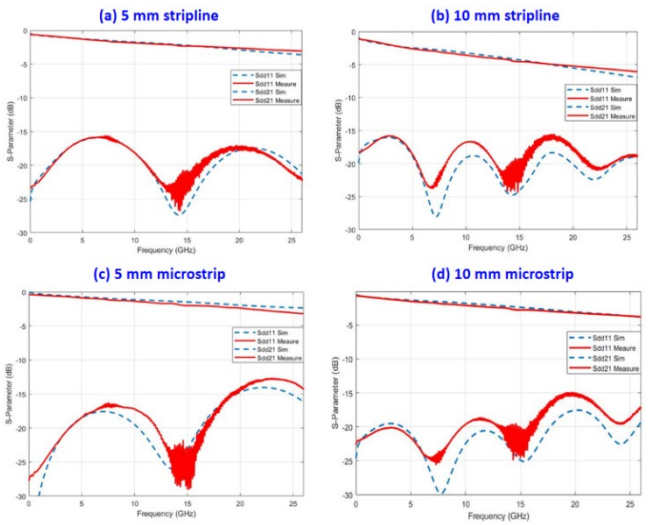

Fig. 7. Measured and simulated S-parameters of PRIS.

III. VCSEL Chip

The laser source used in this study is a high-speed GaAs-based oxide 850-nm VCSEL chip, intended for the development and evaluation of optical communication applications [8]. The VCSEL is wire-bonded on its top surface, and light is emitted from the top of the device. The bandwidth supports data rates of up to 28 Gbps using NRZ or up to 56 Gbps using PAM-4 modulation per channel. This chip is suitable for short-reach (50G/100G/200G) Ethernet, transceivers, and active optical cables (AOC). Fig. 8 shows the VCSEL chip and its dimensions. The chip size and thickness are 190 μm x 205 μm and 150 μm, respectively. The P and N contact area for wire-bonding is 70 μm x 70 μm.

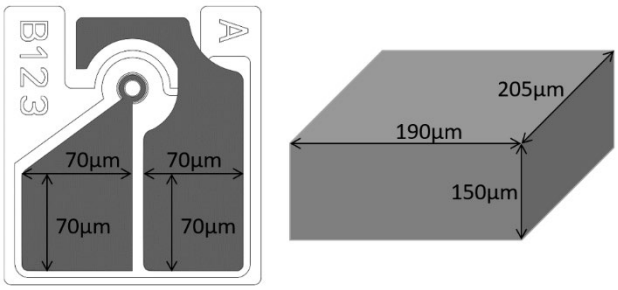

Fig. 8. The VCSEL chip and its dimensions.

IV. Chip Assembly

The chip assembly process includes die bonding with die-attach adhesive, adhesive curing, plasma pre-treatment, and wire bonding. Fig. 9 shows the PRIS with VCSEL chip after assembly. The PRIS and VCSEL chip are connected using two 0.8-mil gold wires (20.3 μm in diameter).

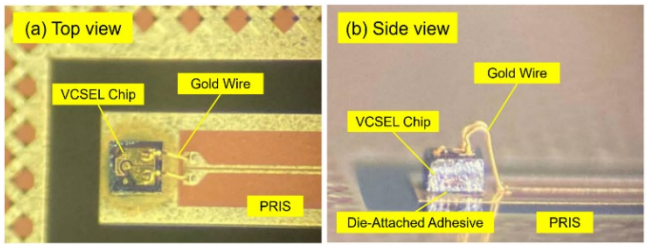

Fig. 9. OM image of the PRIS with VCSEL chip after assembly.

To evaluate the residue effect of the bond wires on S-parameters, the S-parameters are also measured and simulated for PRIS including a pair of gold wires (Fig. 10). As shown in Fig. 11, all measured Sdd11 and Sdd21 values are below -15 dB and greater than -4.5 dB, respectively, at 14GHz (the Nyquist frequency at 56 Gbps PAM4), except for the 5 mm microstrip.

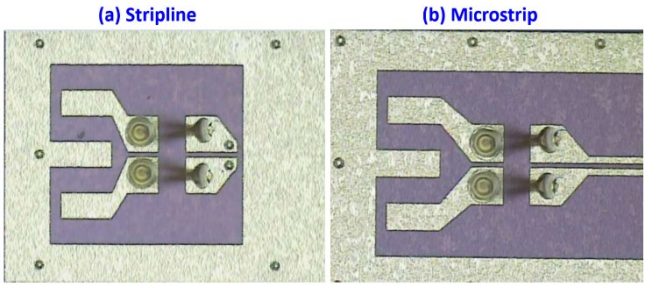

Fig. 10. OM images of the PRIS with a pair of gold wires.

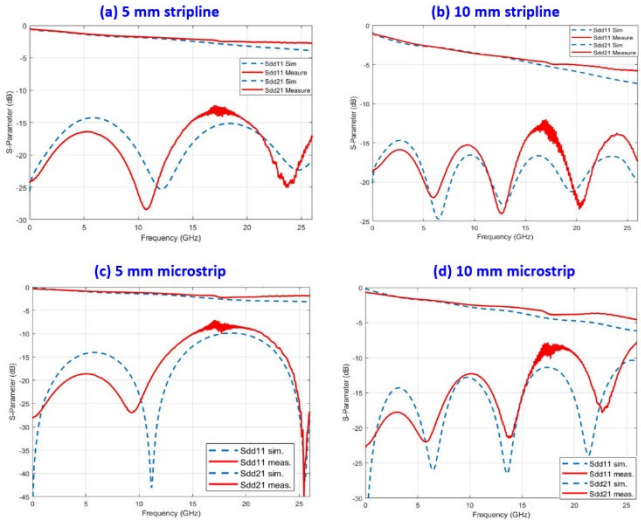

Fig. 11. Measured and simulated S-parameters of PRIS with gold wires.

V. Package Optical Measurement

The experimental measurement setup is shown in Fig. 12. It consists of an Anritsu MP1900A 64 Gbps pattern generator, a Keysight E3630A DC power supply, a 100 μm-pitch GSGSG high-bandwidth probe pin, an Agilent 8163B optical power meter, a Keysight 86100D digital communication analyzer (DCA) with an 86116A module, and a 1 m-long lensed fiber.

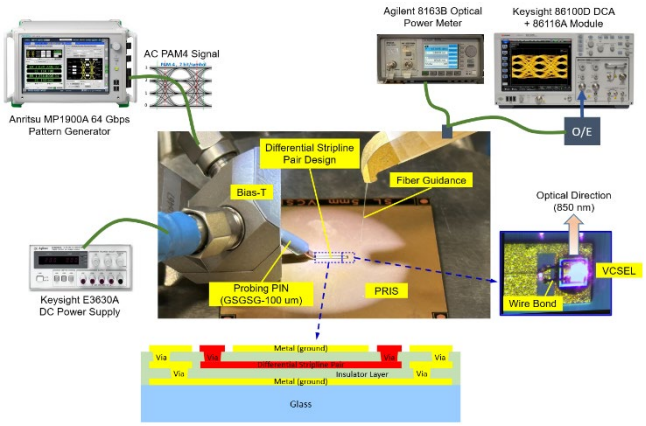

Fig. 12. Experimental measurement setup.

Fig. 13 shows the process flow of the optical measurement. The measurement begins by placing the GSGSG probe pin on the corresponding pads of the sample. The electrical PAM4 signal is then fed from the pattern generator to the transmission line in the PRIS, stimulating the VCSEL to output an optical PAM4 signal. The signal is checked by the optical power meter while adjusting the current and aligning fiber to couple the output signal. When the optical power reaches a sufficient level, the eye diagram is measured and characterized using the DCA.

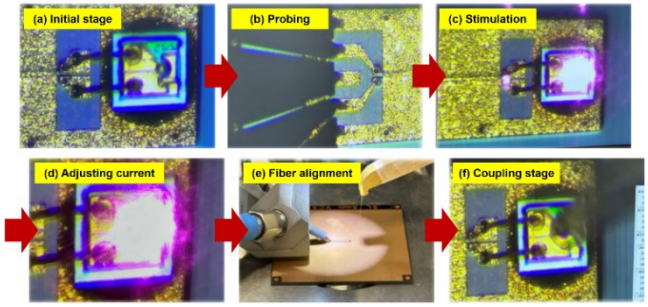

Fig. 13. Process flow of the optical measurement.

Fig. 14 shows the electro-optical characteristics of the VCSEL chip and package. The minimum and maximum values reported in Fig. 14 represent results from multiple measurements across 20 different devices. Compared to the VCSEL alone, the threshold current (Ith) of the package decreases from 8.2 mA to 0.36 mA due to the additional resistance contributed by the copper transmission line. This is also the reason for the increase in forward voltage (Vf), from 2.3V to 2.4 V.

Parameter	Symbol	VCSEL		Package		Unit	Note
		Min.	Max.	Min.	Max.		
Threshold Current	Ith	0.81	0.822	0.36	0.36	mA	-
Slope Efficiency	SE	0.81	0.85	0.8	0.84	mW/mA	@7.5 mA
Forward Voltage	V_f	2.2	2.3	2.32	2.4	V	@7.5 mA

Fig. 14. Electro-optical characteristics of the VCSEL chip and package.

The measured 56 Gbps PAM-4 optical eye diagram is shown in Fig. 15. The transmitter and dispersion eye closure for PAM4 (TDECQ) are 2.87 dB, 1.52 dB, 2.62 dB, and 1.52 dB for the stripline original eye, stripline after feed-forward equalization (FFE), microstrip original eye, and microstrip after FFE, respectively. All TDECQ values are below 3.4 dB, in accordance with the IEEE 802.3 specification, which indicates that the optical module using PRIS can provide high-quality signal transmission.

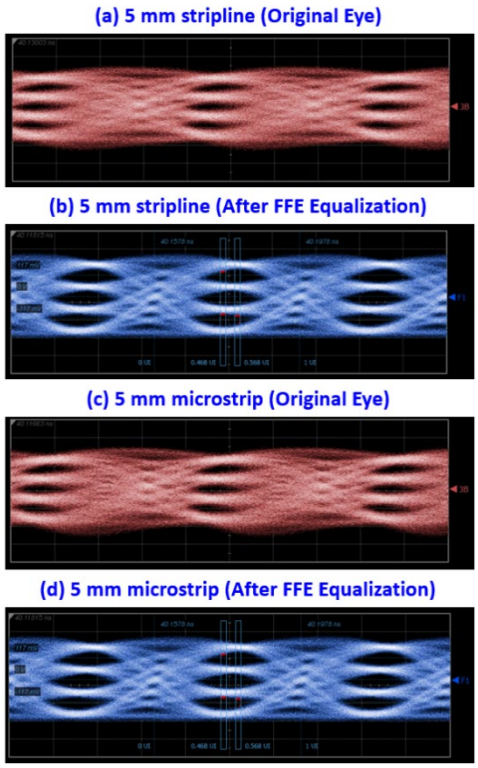

Fig. 15. Measured 56 Gbps PAM-4 optical eye diagram.

VI. Conclusion

The feasibility of a glass PRIS with a VCSEL chip assembly has been demonstrated in this study. The glass PRIS has been fabricated on a 510 mm x 515 mm panel. The OM image has verified the high-density RDL in PRIS and the successful assembly of PRIS with the VCSEL chips. The measured and simulated S-parameters for PRIS alone and PRIS with a pair of gold wires have shown good signal integrity at a high bandwidth. The high-quality, high-speed optical eye diagram and low TDECQ indicate that the package is an excellent optical module and suggest that it is feasible and effective for the PRIS-based heterogenous integration in CPO applications. The next phases of this study will be on the glass PRIS with ASIC switch, laser driver, TIA, PD, etc. The potential challenge related to VCSEL temperature sensitivity is also an important topic for future work.

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