FOWLP for Next-Generation Optical Switches: Scalable Packaging Solutions for Photonic-Electronic Integration

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Abstract

The continuous growth of data-driven applications such as 5G fronthaul, memory disaggregation, and autonomous systems demands increasingly efficient and scalable network technologies. Optical switching is emerging as a key solution due to its potential for low-latency operation, high bandwidth, and energy efficiency. However, the integration of photonic and electronic components into compact and manufacturable packages imposes significant challenges, especially at high interconnect densities.

This paper presents the development and validation of a fan-out wafer-level packaging (FOWLP) approach as part of the Horizon Europe project PUNCH. The work focuses on demonstrating a scalable and precise process flow capable of integrating multiple dies, including a photonic integrated circuit (PIC) placeholder and several electronic ICs (EICs), into a common package

A critical aspect of the PUNCH approach is the development of a scalable, high-performance electrical and optical packaging solution based on a 200 mm FOWLP process. The concept includes a two-layer ERDL with line/spacing of 10/10 µm, allowing short interconnects between PIC and EICs, thereby improving overall performance and reducing power consumption. The package can be connected to a high-density substrate via soldering or substrate embedding. Both approaches are evaluated within PUNCH. For the optical interface, the implementation of an optical redistribution layer (ORDL) is investigated to facilitate scalable fiber coupling, further enhancing the practicality of FOWLP for optoelectronic integration.

In this work, we present the first experimental results of a FOWLP demonstrator, where multiple EICs have been integrated with a large central die, resembling the PIC, to assess manufacturability, die placement accuracy, warpage control, and electrical performance.

Key words

Embedding, FOWLP, Optical Redistribution Layer, Optical Switches, Photonics, System-in-Package

I. Introduction

The increasing demand for low-latency, high-bandwidth, and time-sensitive applications such as 5G fronthaul, industrial automation, data center memory disaggregation, and autonomous systems is pushing the limits of current networking technologies. Optical switching has emerged as a key enabler due to its potential for low latency, high power efficiency, and cost-effectiveness. However, large-scale photonic switch fabrics face significant challenges in electrical and optical packaging, particularly in achieving high-density interconnections, minimizing signal losses, and ensuring scalability for high-volume manufacturing.

In addition to advancing novel approaches for photonic switches and transceivers — and their integration into 5G radio access networks and data center subsystems — the Horizon Europe project PUNCH (Packaging of novel Ultra-

dyNamiC pHotonic switches and transceivers) focused on leveraging Fan-Out Wafer-Level Packaging (FOWLP) technology to address the challenges in facilitating scalable packaging solutions for photonics.

FOWLP provides several advantages over conventional integration techniques, where photonic integrated circuits (PICs) and electronic ICs (EICs) are often mounted separately on a printed circuit board (PCB). By enabling high-density interconnects, reduced parasitic effects, and improved thermal management, FOWLP supports more compact and efficient integration.

The process involves embedding multiple known-good dies into an epoxy mold compound (EMC), followed by the application of a high-resolution electrical redistribution layer (ERDL) to ensure compact and reliable electrical connectivity. This allows for seamless co-integration of PICs and EICs within a single package.

The 2D FOWLP approach adopted in PUNCH offers specific advantages over 3D integration techniques — where PICs and EICs are stacked vertically — such as lower thermal crosstalk, improved heat dissipation, and a simplified package architecture that avoids the complexity of Through-Silicon Vias (TSVs). However, this approach also introduces challenges, including the need for dense signal routing and managing warpage in large-scale packages.

II. Packaging for Photonic-Electronic Integration

Optical switches are critical components in modern high-speed communication networks, enabling efficient data routing with minimal latency [1], [2]. The integration of photonic and electronic components is essential for enhancing the performance of these switches and is facilitated by advanced packaging technologies.

Recent advancements in 3D heterogeneous integration highlight the benefits of co-packaging optical and electronic ICs, which optimize system efficiency by reducing interconnection distances and improving thermal management [3], [4]. FOWLP has emerged as a good method for packaging PICs, allowing for higher interconnect density and efficient thermal management by embedding multiple dies within a single package [5], [6].

Fiber attachment is a crucial aspect of optical packaging, directly influencing the efficiency of optical switches. Different coupling techniques can be used, such as edge couplers, grating couplers, and adiabatic tapers.

Edge couplers provide a direct optical path by aligning the fiber with the waveguide's edge, resulting in low coupling losses and high efficiency, though this method requires precise alignment, which can complicate manufacturing [7], [8]. Grating couplers utilize periodic structures to diffract light, allowing for vertical coupling but is very limited in bandwidth and is polarization-sensitive [9].

A further strategy is based on adiabatic tapers. In combination with the inclusion of Optical Redistribution Layers (ORDLs), this approach enhances optical coupling by enabling efficient and flexible routing on either package level (FOWLP) or on a substrate [10]. While edge couplers, once embedded, are not or only difficult to access, adiabatic taper structures allow accessing the PIC from the top side. ORDLs allow for the interconnection of different PICs as well as the coupling of PICs to optical connectors. When combined with substrate embedding, where dies or FOWLPs are embedded into a PCB, this architecture enables highly parallel, low-loss optical interconnects. Substrate embedding further simplifies system assembly, improving thermal and electrical performance, and supporting scalable manufacturing [11].

III. FOWLP Design and Process Development

A. Package Layout

The design of the package is strategically developed to optimize the integration of a large central die, resembling the PIC, surrounded by multiple smaller driver EICs. Specific characteristics of this test vehicle design are the relatively large area of the package (15x15 mm^2), a high number of dies (1 PIC, 8 EICs) and small gap down to 100 µm between the dies to achieve short interconnection paths. and accommodate high speed operation. Four identical EICs are placed on both north and south side of the PIC in this demonstrator as shown schematically in Fig. 1.

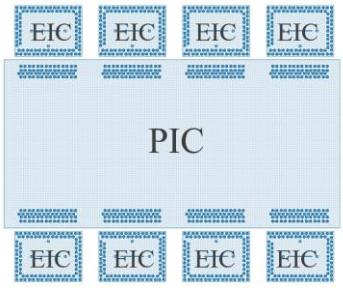

Fig. 1: Schematic representation of the multiple EICs around a single PIC.

A two-layer polymer-based ERDL is designed incorporating daisy chain and Kelvin structures to comprehensively evaluate the electrical performance of the demonstrator. Alongside the back-end-of-line metallization on the dies, the electrical test structures cover a total of three metal layers. The interconnection paths within the ERDL are consistently maintained at 125 µm and the dielectric via opening size is 30 µm.

The daisy chain resistance test structures between the metallization on the chip and the first metal layer are designed to demonstrate the successful implementation of the FOWLP process, facilitating connections between all EICs and the PIC. Additionally, daisy chain structures between the first and second ERDL metal layers allow for a detailed evaluation of the two-layer ERDL performance.

B. Assembly and Molding

The FOWLP is manufactured in a mold-first face-down approach as depicted in Fig. 2, allowing for the integration of multiple dies with the shortest interconnections paths without the need of bumping the chips.

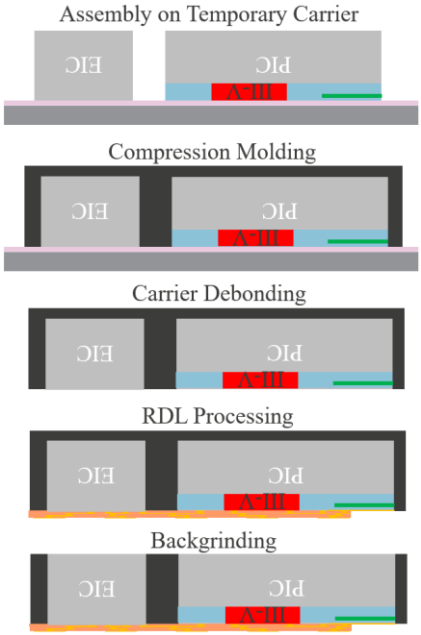

Fig. 2: Simplified process flow of a mold-first face-down FOWLP approach.

In this process, the components are assembled on a temporary carrier, followed by compression molding to create a reconfigured wafer (Fig. 3). A Datacon 2200 Evo Advanced is used for the assembly of the dies and a TOWA Y-120 compression molding machine with a 200 mm diameter cavity for molding. For test purposes, the wafer is not fully populated. The die positions are accurately measured with a Mahr OMS 600 coordinate measurement system before and after compression molding to determine placement accuracy and die shift due to different CTEs of carrier end molding material.

The comparison of die position measurements before and after molding is used to derive a die shift factor, which is then utilized to compensate for the die shift in following wafers by adjusting the assembly position [10].

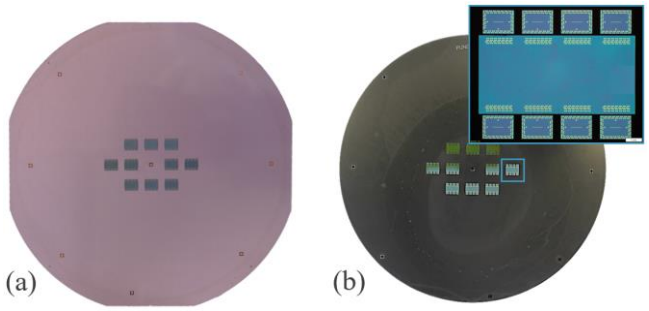

Fig. 3: Test chips assembled on a temporary carrier before molding (a) and reconfigured wafer after compression molding and debonding of the temporary carrier (b).

Although only the central part of the wafer is populated in this run for test purposes, this compensation factor can be used to eliminate the effect of die shift for larger or fully populated wafers. A deviation of less than 10 µm from the target position after molding is achieved, which is sufficient for further processing. No significant difference between the die shift of larger and smaller dies is observed, especially important for ensuring a good connection through the ERDL between the various dies in the package.

C. RDL Processing

After debonding of the reconfigured molded wafer, wafer-level lithography processes are used to create an ERDL.

The main challenge in ERDL processing is the optical interface for the ORDL. Although it is not present in the test vehicle, it is used to set up the necessary processes. The ORDL interface must remain free of ERDL layer deposition, while ensuring that neither the ERDL processes nor auxiliary steps such as plasma cleaning cause damage to the interface. To achieve this, a thin metallic layer is patterned over the ORDL interface prior to the actual ERDL processing. In order to realize this, a thin metallic layer is structured over the ORDL interface prior to the actual ERDL processing. The type of metallization is chosen in accordance with the compatibility of the RDL processes and the capability of selective wet etching towards the ERDL materials after ERDL processing. This area can be seen in the upper left side of Fig. *4*. The actual ERDL processing can be performed as usual starting with the first dielectric layer realized by a photo imageable polyimide. The recess for the optical interface is already considered in all mask layers, for the polyimide as well as the Cu layers (no routing over this area). The following copper layers are realized by semi-additive processing. The second Cu layer on the FO package is realized thicker compared to layer one to enable the embedding as well as the solder ball integration version as a higher amount of Cu is needed for the soldering process of SnAg.

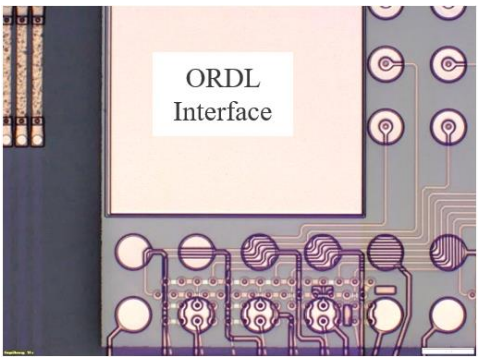

Fig. 4: FOWLP after last (passivation) polymer layer with an area covered only with a thin metal layer as interface to ORDL.

The third and last polyimide layer acts as a passivation and solder stop layer. The wafers are grinded to final thickness after the finalization of the ERDL layers. This is done last for better handling during ERDL processing.
For samples dedicated for soldering on a substrate, solder balls are applied in wafer-level stencil process as a last process step before dicing. This process step is left out for samples dedicated for substrate embedding.
Fig. 5 shows an exemplary package with solder balls after singulation as well as after assembly on a test substrate. Details on the further integration of the packages in or on a substrate, respectively, are given in section V.

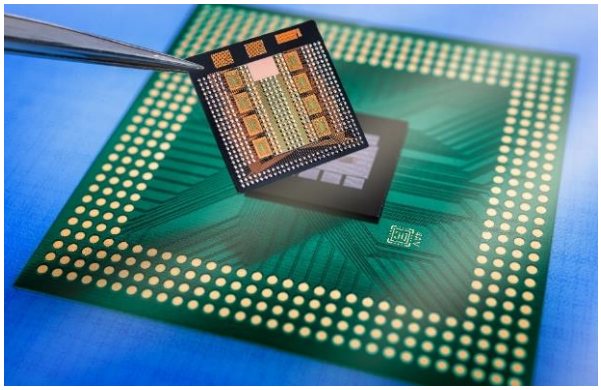

Fig. 5: Exemplary packages before and after assembly on a test substrate.

IV. Evaluation and Testing

To evaluate the process results, optical inspection and cross-sectioning as well as warpage measurements and electrical testing are performed.
Cross-sections as depicted in Fig. 6 show good pad connections and continuity of traces. The warpage on package level is measured and below 10 µm along one package side, which is considered low enough for the fiber array attachment, for which only a smaller part of the package side is critical.

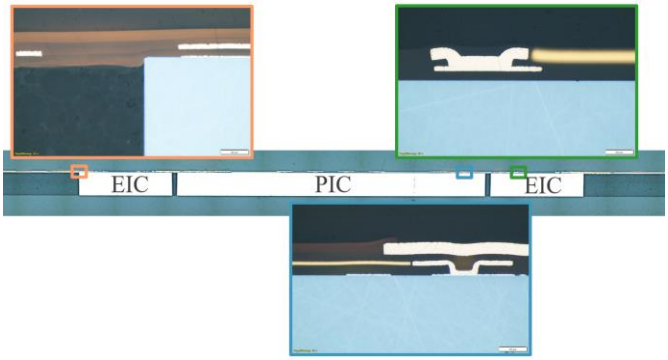

Fig. 6: Cross-section of the FOWLP with details of redistribution layers and vias, showing good connections between vias and landing pads.

To characterize the successful electrical connectivity and verify the electrical performance of the interconnecting ERDL, the daisy chain resistance is characterized using a standard probe station (Alessi REL-2500). The characterization results for 4 exemplary packages are presented in Fig. 7. These daisy chains connect the chip metallization and the first ERDL metal layer.
No open circuits, representing a yield of 100 %, are observed. As expected, the electrical resistance follows a linear trend with an increasing number of vias. The average electrical resistance of an individual ERDL and a connecting via is measured to be 67.5 ± 7 mΩ. An offset from the origin is observed, which can be attributed to the interconnection length between the signal path and the first via.

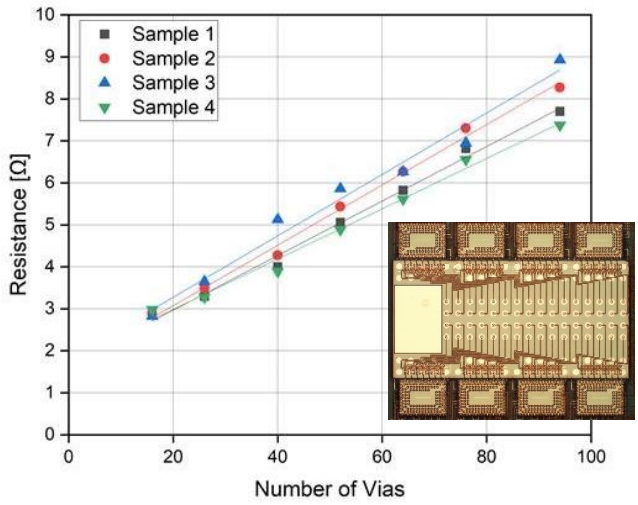

Fig. 7: Preliminary characterization results of the daisy chain resistance for four different packages. The insert shows an exemplary FOWLP demonstrator with daisy chain structures.

V. Further Integration and Optical Connection

A. Substrate Integration and thermal management

To connect the developed FOWLP to the next level of the electrical and optical network, two routes of substrate integration are investigated: FOWLP on substrate and embedding of the entire FOWLP structure into a high-density substrate.

Fig. 8 illustrates the approach in which a FOWLP with solder balls is connected to the substrate by means of a conventional soldering process. To also accommodate the optical connection from the PIC integrated in the FOWLP to the ICS, a method is developed to realize adiabatic coupling between a taper structure on the PIC and an ORDL layer previously defined on the IC. Details on this approach are given in [13]. The ORDL is directly connected to the fiber array by optical alignment.

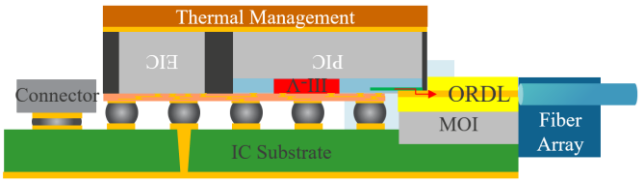

Fig. 8: High level of schematic of the integration approach with a FOWLP soldered on an IC substrate.

Fig. 9 illustrates the approach in which the FOWLP is embedded into the IC substrate and located in the cavity. A thin layer with less than 50 µm of polymer layer is laminated and covers the FOWLP. The optical connection is similarly foreseen using an adiabatic coupler, but in this case implemented by fabricating the ORDL on top of the face-up oriented PIC with taper structures.

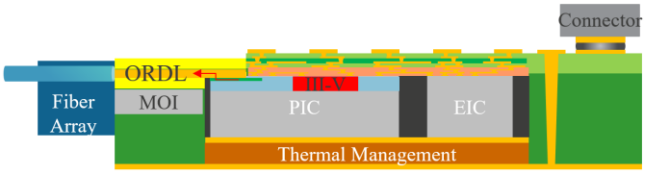

Fig. 9: High level of schematic of the integration approach with a FOWLP embedded in an IC substrate.

This approach combines the advantages of mature wafer-level processes for the fine-line connection of PIC and EICs and layer thicknesses of less than 10 µm from FOWLP with the advantages of substrate embedding, such as short electrical interconnection paths compared to flip-chip soldering, mechanical stability and the possibility to use an ORDL on the substrate for in-plane connections between the optical components and the next packaging level. Although the embedding approach requires more technical maturity compared to a conventional on-substrate integration, it promises up to 50% reduction of e-signal attenuation compared to flip-chipping [14].

Additionally, both methods enable effective thermal management, as the two-dimensional configuration results in less thermal cross-talk compared to three-dimensional approaches. Furthermore, heat sinks and metallic connections facilitate efficient and extensive heat dissipation through the backside of the package.

B. Optical Redistribution Layer

To serve as ORDL, a polymer-based material is proposed due to its low propagation loss and the compatibility of single-mode (SM) polymer waveguides with wafer- and package-level integration. To achieve efficient adiabatic coupling between PIC and ORDL, the on-chip waveguide - typically SiN or Si - must be tapered in a manner that minimizes excitation of higher-order or radiation modes. The taper design follows the “Mono” method, which ensures efficient coupling by maintaining phase-matching conditions between the two waveguides [15].

PICs incorporating these “Mono” adiabatic tapers are fabricated using a process flow that includes lithographic patterning and/or flip-chip bonding for the deposition of polymer waveguides [13]. The resulting adiabatic coupling loss is illustrated in Fig. 10. For SiN taper lengths of 1 mm, coupling losses below 1 dB are achieved across most wavelengths within the O-band. Additionally, the polarization-dependent loss for the depicted PIC-to-ORDL configuration (see inset) remains below 1 dB.

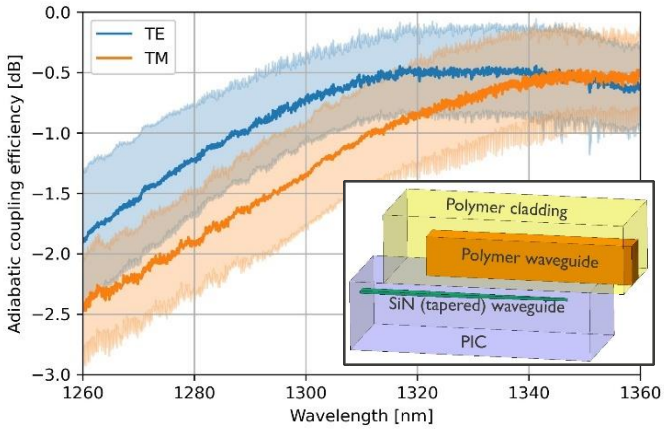

Fig. 10: Average adiabatic coupling efficiency for a 1-mm long taper in the O-band wavelength region, for both transverse electric (TE) and magnetic (TM) polarization. The inset graphically shows the SiN-to-polymer optical coupling setup.

Building on these findings, polymer-based ORDL fan-out circuitry presents a scalable solution for optical interconnects by integrating optical routing layers, thereby mitigating the complexity and limitations associated with directly interfacing many optical fibers with the PIC. This approach

is particularly well-suited for heterogeneous integration, offering high bandwidth density and improved energy efficiency. This approach allows making optical connections from the PIC top surface, so is compatible with PICs integrated in FOWLPs.

Optical FOWLP offers a path to significantly higher optical I/O density on photonic chips, enabling more compact designs and greater waveguide integration. With spacing limited primarily by crosstalk between adjacent polymer waveguides, interconnect pitches below 50 µm are achievable - allowing denser and more efficient coupling to external fiber arrays.

C. Fiber array attachment

The ORDL waveguides are designed in such a way that their mode field diameter (MFD) matches those of standard single mode fibers, thereby elegantly allowing direct butt-coupling between both. As the mechanical stability of this attachment is crucial, a mechanical optical interface (MOI) in the form of a stiff substrate (silicon or glass) is foreseen underneath the ORDL. The dimensions of the chosen fiber array (FA) in terms of width and thickness are be based on the optimization of the contact area between the FA and the ORDL+MOI components.

PUNCH also investigates direct FA attachment to standard edge couplers on PIC in case an intermediate ORDL is not required. To systematically optimize the FA integration process and mitigate the associated risks of optical misalignment and coupling inefficiencies, a comprehensive series of experiments was conducted. These investigations focused on evaluating two distinct mode field diameter (MFD) matching strategies: the use of spot-size converters (SSCs) and ultra-high numerical aperture (UHNA) fiber arrays. Both approaches demonstrated potential for improving coupling efficiency between the FA and the small MFD of the edge couplers on the PIC. Currently 3.3 dB coupling loss is achieved for the connection between an UHNA fiber array and edge couplers in O-band.

VI. Conclusion and Outlook

The results validate the feasibility of using FOWLP for large-scale optoelectronic packaging, paving the way for future implementations with functional PICs and semiconductor optical amplifiers (SOAs).

High placement accuracy and full electrical functionality were achieved in the initial demonstrator. Various optical coupling strategies were explored, laying the foundation for future full integration of active PICs. The results underline the potential of FOWLP as a key enabler for next-generation optoelectronic systems.

While processing will remain on 200 mm wafer scale during the PUNCH project, the overall process flow is compatible with larger wafer formats and potential high-volume production.

The next phase of the project will include the integration of functional PICs with SOAs and transceiver elements as well as the detailed analysis of the two different substrate integration methods presented in this paper. Especially the variant that combines FOWLP and substrate embedding promises excellent electrical performance and scalable processes for making an optical connection. Both FOWLP and substrate embedding are enablers of making scalable, cost-efficient and flexible optical interconnections by means of optical redistribution layers and adiabatic coupling.

Furthermore, while this work focused on the low-speed aspects of the electrical interconnections, the analysis of high-frequency signal integrity is planned for future demonstrators with functional dies.

By transitioning from conventional sequential packaging methods to a more parallel and scalable approach, the PUNCH FOWLP concept demonstrates a promising pathway toward high-volume manufacturing of advanced optical switches. The development of robust packaging solutions that incorporate multiple technologies is essential for advancing the capabilities of optical networking systems.

Acknowledgment

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