Innovative Digital Patterning by LITHOSCALE® XT for UHD FO WLP and HD PLP Required in 3D Integration

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Abstract
Fan-out panel level packaging (FO PLP) represents a growing segment of the overall FO packaging technologies, with designers motivated to transition from wafer to panels to achieve enhanced utilization of multi-die packages and optimized CoO. In the present investigation, LITHOSCALE® XT system, which has been proven for UHD FO WLP, was utilized for lithographic patterning of redistribution layer (RDL) and VIA structures for application in FO PLP for substrate 300×300 mm². This innovative equipment overcomes the limitations of legacy exposure technology, especially for large die sizes interposer patterning. The advanced software has been optimized to meet the demands of challenging 3D integration, representing a significant technological innovation that addresses the requirements for the future HPC and AI devices driving innovation and efficiency in the semiconductor industry.

Key words
FO PLP, digital lithography, RDL/via patterning, high resolution dielectric PI.

I. Introduction
The Fan–out (FO) packaging is a versatile technology providing low pitch, high I/O density packages with lower thermal resistance, better signal integrity and smaller footprint then other mainstream packages. One of the major trends driving the FO packaging development is large die partitioning into chiplets and heterogenous integration (HI). The industry is trying to reduce single–unit die sized by integrating several partitioned smaller dies to improve the gross yield because the smaller the die, the higher the yield. These dies – "chiplets" are emerging in HPC related applications, including data centers, AI networking and edge computing segments. Ultra–high density (UHD) Fan–out Wafer level packaging (FO WLP) technologies are being adopted in HPC, networking and computer applications to enable integration of chiplets and HI [1].

Fan–out Panel–level packaging (FO PLP) is a growing segment of the packaging industry. The reason for designers to consider a change from WLP to panel–level is cost optimization. Most activities for FO packaging are batch activities performed on the entire wafer or panel at one time. The more die processed during batch activities, the greater opportunity for cost optimization. For FO PLP, handling substrate warpage and die shift can be a challenge even at the wafer level; these must be considered at the panel level as well. There are a few panel sizes available, and using the largest panel size for economic advantage may involve a trade–off with yield. New equipment and materials may be required [2]. The PLP enables the industry to increase the substrate area for building chiplets. The square area allows more chips to be assembled at the same time, increasing capacity, and reducing supply constraints. The FO PLP allows for simplified integration of various die technologies (logic, memory, and RF) into a single package that is smaller and thinner [3].

Both approaches, WLP and PLP come in the RDL-last and RDL-first flavors, have reached maturity and are currently being introduced in high volume manufacturing.

Clear application trends follow the technology roadmap that describes integration of low-density core technology for e.g. RF (radio frequency) or PMIC (power management IC) packaging over high density application processor packaging to ultra–high density applications for networking services etc. [4].

The organic interposer technology in one of the most promising new integration interposer platforms, providing low RC interconnect with good signal isolation and design scalability. The devest development offer 5.5× reticle size,

line/space 2 µm/2 µm RDL, "via CD/cap" 8 µm/11 µm, 4 SoC with 12 HBM. The interposer RDL layer count is up to 9 layers (9L) and 248 IPDs. The SoC die–to–die (D2D) gap is 150 µm and minimum SoC micro bump pitch is 35 µm. Chip on Wafer size is 66×68mm^2 [5].

In the previous research, the capacity of the Maskless Exposure Technology (MLE) was effectively employed for lithographic patterning of high–resolution, low temperature cure polyimides (PI) dielectrics for UHD FO WLP [4]. By digital patterning with LITHOSCALE® equipment, the steep VIA profiles were attained required for subsequent 3D integration processes. The accomplished resolution exceeded 2 µm L/S at 5 µm FT achieving the min. VIA diameters 4 µm [6].

In the present investigation, the efforts were made to further expand an application to FO PLP. The newly developed high throughput LITHOSCALE® XT was employed in this research, by using high resolution PI dielectric materials.

II. Experimental

A. Digital Lithography Technology

The LITHOSCALE® XT is example of a digital high-volume lithography system for advanced 3D heterogenous integration. Its real-time auto focus, high depth of focus, dynamic distortion compensation, and broad process–matrix capabilities prove the benefits of the technology vs. traditional exposure systems for next-generation devices.

Operating at single or, simultaneously, at two wavelength bands (λ=375 and 405 nm), thin & thick resists, dielectric materials, transparent, black, RGB or IR resists as well as many other established and novel materials are optimally exposed. An individual 'exposure-matrix' permits to select arbitrary pairs of test parameters, such as exposure dose, spectral composition focal position, and exposure speed, to quickly determine the optimum process recipe and multi-dimensional process windows during the production ramp–up phase, thereby minimizing set-up times and simplifying material changes. This equipment allows for excellent process control, including sidewall profile, complex topography structure and high aspect ratio patterning. Exposure is performed on the full wafer surface, demonstrating zero stitch performance [6]. The LITHOSCALE® XT processing pipeline digitally transforms vectorized pattern data and compensates for distortions during exposure based on pre-measured and real-time acquired alignment information. An illustration of the capabilities is shown in Fig. 1.

Figure 1: Glass wafer, tilted view, patterned by black resist illustrating the features of the system: six exposure heads, having fulfilled layout, wafer edge zone exposure control feature.

B. Processing Conditions of High-Resolution PI Dielectric

In this paper, MLE was employed on a multi–exposure head LITHOSCALE® XT to prove the technology's suitability for production-grade FO PLP on novel thin film PI dielectric on wafer and panel substrates.

Targeting the application's requirements, the newly developed, high-resolution PI LTC 9320–E76B next-gen., negative tone, PFAS–free dielectric was evaluated. To achieve a post-cure dielectric film thickness of 5 µm, the process conditions were optimized ascertaining the most effective focus/dose/energy matrix for the high-resolution PI. The objective of the work was to reduce the feature sizes and to achieve optimal VIA profiles. The processing conditions are summarized in Table 1 while the LITHOSCALE® XT design layout is shown in Figure 2.

Table 1: Lithography Processing Conditions of PI Dielectric

Process	Equipment	LTC 9320–E76B next gen
Spin Coating/Wafers Spray Coating/Panels	EVG120	4220 rpm/30s OmniSpray®
Lithography/ Maskless Exposure	LITHOSCALE® XT	Wavelengths 375nm, 405nm Dose range 350–850 mJ/cm^2 Focus range –14 to +6 µm
Soft Bake Final Cure	EVG105	100 °C for 5 min 230 °C for 180 min
Spray Development	EVG120	HTR–D2 (CPO) for 40 s
Descum		O_2 plasma for 30 s

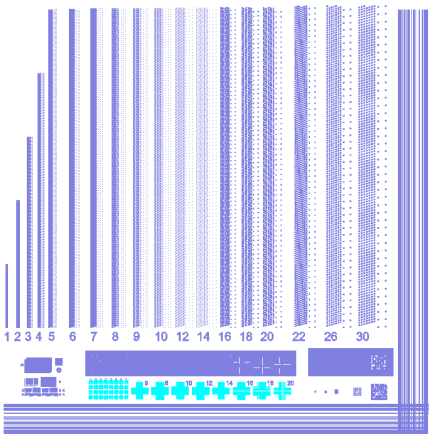


Figure 2: Design layout is repeated in a period of 11mm in all four directions: dense VIA, isolated VIA, L/S patterns.

The rectangular glass substrates, measuring 300×300 mm² square, were subjected to a spray coating process that employed OmniSpray® technology. The utilization of ultrasonic spray nozzles ensured the attainment of maximal homogeneity of the PI coating.

III. Results and Discussion

The metrology and data analysis work included CD uniformity scans, optical macro- and microscopical inspection, SEM cross–section inspection and spectral reflectance measurement of the coated wafers.

A. Spray Coating Uniformity Plot on Glass Panel

Analyzing the FT uniformity plots (Figure 3) of the spray coated panels, we also proved good uniformity value of ±8.3 %. The spectral reflectance measurements were taken with total 81 points resulting in an edge exclusion zone 10 mm.

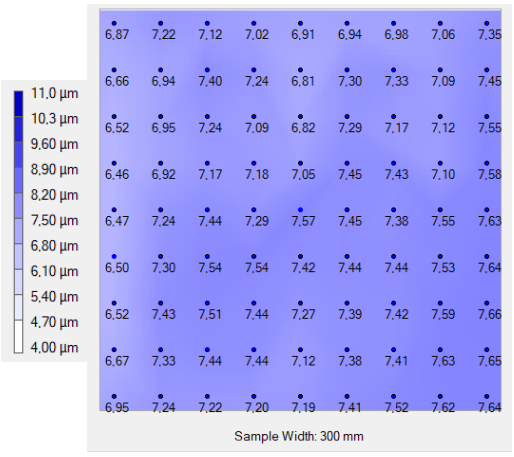
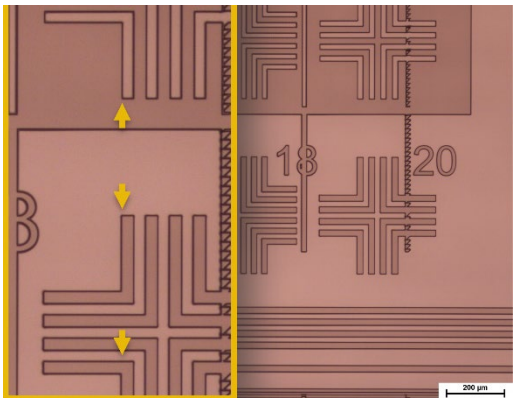


Figure 3: FT Uniformity plot for PI dielectric after spray coating on square substrate 300×300mm².

B. "ZERO STRICH" Software Optimization on Si and Glass

In this work, high dynamic grey–level overlap between the fields at different gradients is investigated and the influence of the negative–tone PI and the exposure dynamics is reviewed. The new equipment feature is implemented in a manner where neighboring exposure field overlap in a finely formed gradient-field, forming a resolution-wise crisp, but amplitude–wise smoothly diminishing border region that is exactly matched to its opposite counterpart. The individual resist behavior can be accommodated, which otherwise can lead to artefacts due to the interference between different curing states. It was proven, that also for PI dielectric, the new functionality together with well-controlled material dynamics is a critical feature that overcomes challenges of reticle limitations as found in steppers and enable stitch-less "infinite"–field exposures in digital exposure like the EVG's LITHOSCALE® XT system for advanced packaging applications.

To investigate the exposure-overlap regions in detail, stitching markers (vertical and triangular rasterized lines) are automatically overlayed onto the layout at equal distances on the left and right of the stitching region, respectively. Note that the stitch is chosen to be exactly at one of the vertical lines to trigger possible edge defects. Despite this challenge the exposure does not indicate any visible alterations from the intended profile.



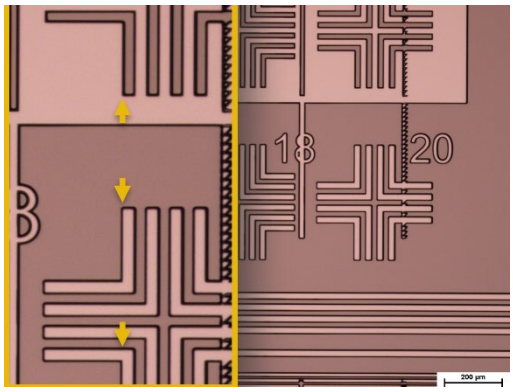


Figure 4: TOP - PI dielectric patterned on Si wafer with active "ZERO STITCH" software feature. Stitching markers are activated on the left and right of the stitching line (superimposed line and row of triangles) The stitching region is magnified on the left and the stitching line is demarked by yellow arrows. BOTTOM - Image of the "ZERO STITCH" software feature applied on PI dielectric patterned on a glass wafer. No stitching artifacts can be found in either case.

C. SEM Resolution Test Structures

For investigating the image and resist performance a range of test patterns were implemented ranging from dot arrays, straight & diagonal free-standing and parallel lines to circles and wedges as they are used in a wide range of applications. The "Siemens Stars" are structures that are commonly avoided during real-application processing, since they challenge the exposure process literally in all directions. These structures always unveil the resolution breakdown and the resist resolution/moulding at the resist resolution, whichever comes first. In Figure 5 positive tone patterning structures from the same field are displayed next to each other. Over and under-exposure can easily be monitored and set with these paired patterns. Only at the optimum exposure point both tones appear as similar structures.

The central resolution breakdown circle at the <2 µm-L/S level shows that the L/S-ratio becomes biased towards the intrinsic resist behavior. The slight bridging between the sub-resolution beams at the center is caused by digital sampling of the exposure system.

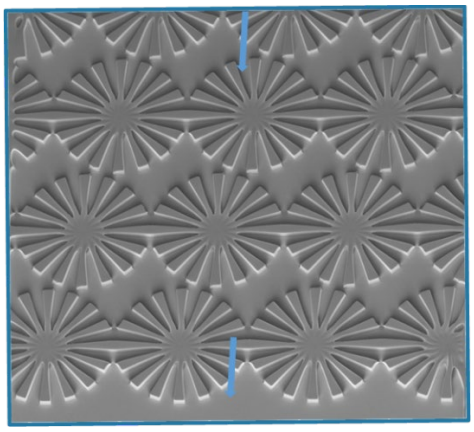


Figure 5: The 'Siemens Stars' show smooth edge contour of star pattern in all lateral directions. The "zero stitch" is not visible over the multiple patterns.

D. Critical Dimension Uniformity Plots

After investigating the optimized exposure and directional resolution limits the homogeneity of the imaging quality the test-matrix across the whole substrate was evaluated on a grid of resolution-evaluation cells.

The particular measurement utilized the vertical 11 µm L/S CD-targets in the L-shaped target line (Fig. 6) featuring equal line an space width of the line structures, generated a list of representative entries covering the whole substrate and interpolated the data to visualize the critical dimension uniformity (CDU) across the whole substrate in a continuous fashion. The relative CDU evaluated as Michelson contrast yielded ±1.83 % and stayed below 150 nm in all but two locations on the wafer-edge.

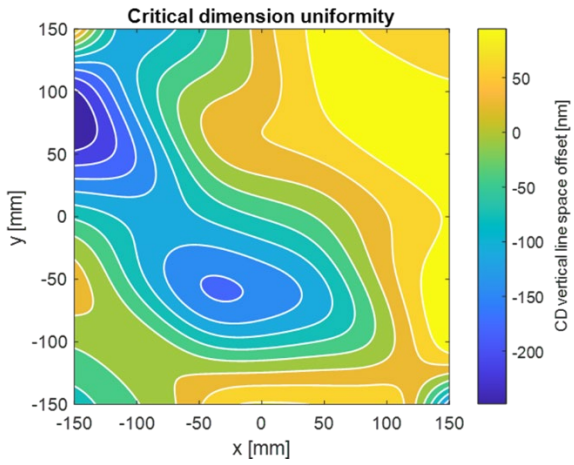


Figure 6: CDU – contour plot of the critical dimension distribution evaluated as vertical line distance in writing orientation. Sampling was performed in a l→r, t→b raster scan fashion. No

vertical striping is visible in the scan direction.

IV. Conclusions

To support the growing advanced packaging application, EVG conducted research on digital patterning of high-resolution PI by LITHOSCALE® XT equipment on 300×300mm^2 glass and silicon substrates, respectively.

By this newly developed, high throughput equipment, in synergy with advanced software, unique values of the technology vs. PoR in FO PLP were proven. The EVG's digital patterning technology achieved 4 µm bottom VIA opening at high resolution <2 µm L/S on PI dielectric.

Besides the fan–out packaging, the system is ideally suited for applications involving multi die patterning, MEMS, advanced imaging, and die traceability for security and automotive applications.

The spray coating by propriety Omnispray® technology resulted in only ±8.3% uniformity on panels, emphasizing the EVG's full technologies solutions for panel processing.

The LITHOSCALE® XT fully digital platform ensures large die size patterning capabilities having no design restrictions in 3D integration. Advanced software is a key for Zero Stitch feature and dynamic "on–the–fly" compensation needed in heterogenous integration processes. This development establishes a new industry standard in the field of the digital patterning system for both, UHD FO WLP and HD PLP.

It was demonstrated that LITHOSCALE® XT equipment is essential for meeting future requirements of HPC and AI devices 3D integration driving innovation and efficiency in the semiconductor industry.

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