Multiphysics Approach to Reliability Prediction of Integrated Circuits Due to Radiation Induced Failures

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Abstract
The continuous advancement in semiconductor technology has led to a reduction in device operating and threshold voltages, rendering integrated circuits increasingly vulnerable to particle radiation effects. Concurrently, the shrinking process sizes have exacerbated charge sharing effects, elevating soft errors induced by single event effects to a primary cause of circuit failures. To address this challenge, we present a multiphysics workflow that enables robust sensitivity evaluation of integrated circuits under radiation-induced stress.

This paper presents a comprehensive approach to evaluating the radiation-induced vulnerability of semiconductor components in aerospace and defense applications. As the miniaturization of integrated circuits continues, traditional netlist-based analyses have become insufficient for accurately assessing the impact of single event effects (SEEs). We introduce a novel reduced order modeling (ROM) framework that couples TCAD-level device simulations with system-level reliability estimation and using CRÈME96 environment model. The ROM is trained using datasets generated from Design of Experiments (DOE) runs conducted through TCAD simulations, spanning the full LET domain and validated against published cross-section data.

Key words
Radiation, SEE, Susceptibility, Semiconductor, Reliability

I. Introduction
The current approach for designing chips that are radiation hardened typically involves a legacy-based methodology, deriving most of the baseline design aspects from existing product types. This approach stifles innovation and limits the ability to adopt a wide range of component types for space applications. Also, given the extended design and qualification cycles, the types of rad-hard components are restricted to a narrow set of product categories and vendors. With all these challenges present and the tremendous growth of space applications requiring components with high reliability to radiation effects, the need to have a simulation driven approach not only becomes more important but also a requirement.
The multiphysics approach outlined in this paper aims to improve current chip design workflows while broadening opportunities for innovative commercial products and design categories, particularly those requiring radiation-hardened capabilities for high-demand applications.
In this paper, we evaluate the behavior of semiconductors at the component level under single event effect (SEE). A comprehensive approach using a reduced order modeling (ROM) framework is presented to characterize the behavior of discrete elements. The developed model predicts SEE-induced response across varying strike conditions, bias levels, device geometries, and layout parameters such as incident angle and sensitive area.

II. Device and Stress Procedure Description
When high-energy particles, such as protons, heavy ions, or neutrons, penetrate semiconductor devices, they deposit energy along their trajectory through a process called ionization. This energy deposition generates electron-hole pairs within the semiconductor substrate. The free charges created can be collected by sensitive regions of the device, particularly the drain regions of transistors, resulting in

transient current pulses. These pulses, also known as single-event transients (SETs), can propagate through the circuit and lead to logic errors or functional disruptions.

The trend towards device miniaturization and increasing integration density in modern semiconductor technology has intensified the vulnerability of integrated circuits (ICs) to such particle-induced effects. As transistors shrink in size and more components are packed into a single chip, the spatial energy deposition range of a single particle becomes capable of influencing multiple adjacent transistors simultaneously. This increased spatial susceptibility leads to the charge sharing effect, wherein the generated charge from a single particle is distributed across several nodes. Consequently, this results in single-particle-induced multiple transient events (SMTEs), which are particularly challenging to detect and mitigate.

Moreover, the reduction in critical charge—the minimum amount of charge needed to change a logic state—and lower switching thresholds in scaled technologies further exacerbate the situation. Even particles that do not directly strike sensitive regions can induce enough charge through indirect paths to flip states or cause timing violations, significantly increasing the probability of soft errors in logic and memory circuits.

As SEE have emerged as a primary failure mechanism in space and high-radiation environments [1], the need for robust evaluation of IC susceptibility has become critical. This evaluation is not only necessary to ensure mission-critical reliability but also to guide the development of fault-tolerant and radiation-hardened design strategies. Traditional evaluation methods that rely solely on circuit netlists are no longer sufficient due to the intricate physical interactions that occur at nanometer-scale feature sizes. Therefore, there is a growing emphasis on incorporating physical layout information and three-dimensional device modeling into SEE vulnerability assessments [2]. This shift reflects the need for multiphysics modeling that couples charge generation, transport, and collection with layout-aware simulation techniques. By integrating TCAD-based transient analysis with reduced order modeling, the proposed framework enables accurate prediction of SEE-induced behavior in adverse environments.

III. Rad Hard Design Workflow

The workflow for evaluating and enhancing the radiation tolerance of integrated circuits, as proposed in this paper, is illustrated in Fig. 1 and consists of a systematic, multi-step methodology aimed at streamlining the radiation-hardening process.

The first step involves identifying the fundamental building blocks of an Intellectual Property (IP) core—these can be logic gates, flip-flops, or custom-designed functional units. Understanding how these elemental structures respond to high-energy particle interactions is crucial for extrapolating the behavior of the entire IP block under radiation exposure. To characterize these responses, Technology Computer-Aided Design (TCAD) simulations are conducted on representative discrete devices. TCAD offers a detailed physics-based modeling environment capable of simulating charge generation, transport, and transient responses at the device level. Simulations yield transient current waveforms, voltage perturbations, and charge deposition profiles across a range of Linear Energy Transfer (LET) values and strike geometries.

Given the sheer volume and complexity of the simulation data, a process known as Reduced Order Modeling (ROM) is employed to distill the information into compact, analytical models. The ROM is constructed using a response surface methodology in optiSLang™, trained on a Design of Experiments (DOE) spanning the LET domain. The surrogate model retains key features of the device's transient response while enabling rapid evaluation across parameter space.

Next, the vulnerability of each device is quantified through a metric known as the cross-section curve, which plots the

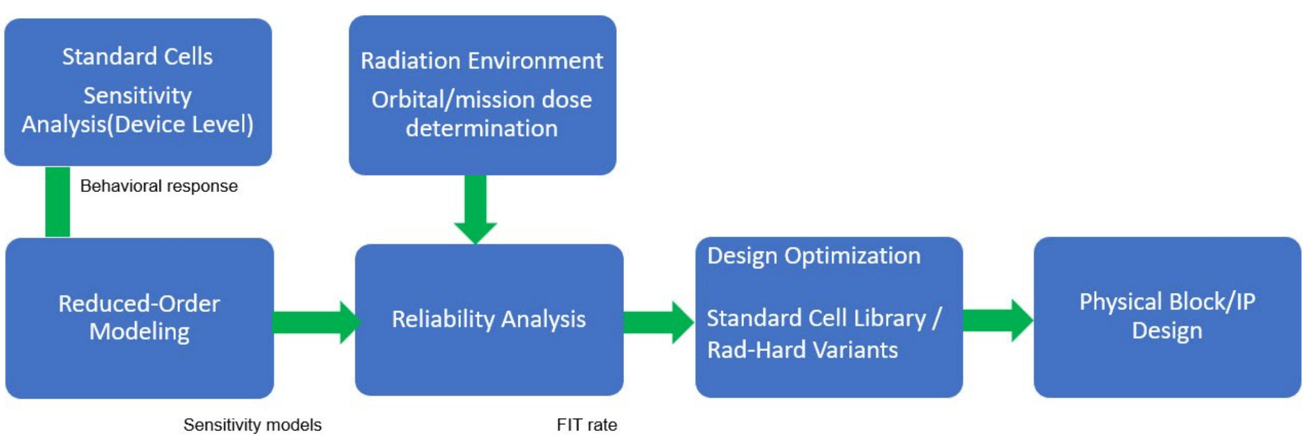

Fig. 1 Rad Hard-Design for Reliability (R-DfR) Workflow

likelihood of an event against the energy of the incident particle. This curve is a key indicator of device sensitivity. To translate this sensitivity into a system-relevant reliability metric, reliability analysis is performed to estimate the Failure in Time (FIT) rate, which measures the expected number of failures per billion hours of operation.

The cross-section data is fitted to a Weibull distribution, and the resulting parameters are used in CRÈME96 to simulate FIT rate under specified orbital and shielding conditions.

The calculated FIT rates and associated sensitivity profiles are then fed back into the design process, allowing engineers to make informed decisions on physical layout strategies, redundancy techniques, and IP selection. This feedback loop is critical in developing radiation-hardened-by-design (RHBD) components that are robust against a wide spectrum of high-energy particle effects, thereby improving the overall reliability and safety of ICs used in space, avionics, and other mission-critical applications.

IV. Data/Results and Discussion

In modern semiconductor analysis, functional decomposition of complex integrated circuits into smaller building blocks and their constituent sensitive devices allows for a more tractable evaluation of radiation effects. For this study, we adopted a hierarchical analysis strategy, beginning at the transistor level and progressing up to the component level. Specifically, semiconductor components were discretized into functional blocks, and each functional block was further broken down into the sensitive devices that comprise its structure.

To investigate the electrical characteristics and radiation susceptibility of these components, we employed TCAD tools. TCAD enabled us to simulate both the intrinsic device behavior, as well as the transient response to high-energy particle strikes across a range of LET values and bias conditions. The simulations included SEE analysis at the transistor level, using a broad spectrum of Linear Energy Transfer (LET) values to account for various particle energies and types encountered in radiation environments.

Following the completion of device-level SEE simulations, a ROM methodology was implemented to upscale the data to the component level. This approach facilitates efficient prediction of radiation responses at higher levels of integration without requiring exhaustive simulation of every particle interaction at the device level.

As a case study, the proposed simulation and modeling workflow was applied to a 6-transistor static random-access memory (6T-SRAM) cell. The layout of the SRAM cell is illustrated in Fig. 2, alongside the ROM output depicting voltage fluctuations that correspond to bit upsets induced by particle strikes. These voltage signatures are critical indicators of soft errors, such as single event upsets (SEUs), and provide insight into which device nodes are most vulnerable to state flips.

The ROM development process involved an automated pipeline that converts raw output files generated from TCAD simulations—typically large text files containing time-domain data—into usable input for Ansys optiSLang™. This platform is employed to build a response surface model that captures the functional relationship between input parameters (e.g., LET, strike location) and output metrics (e.g., node voltage, transient current). The response surface enables fast evaluation of device behavior over a wide range of scenarios, bypassing the need for computationally expensive full simulations.

One of the key outcomes of this ROM-based methodology is the generation of a cross-section curve for the SRAM cell, as shown in Fig. 3. This curve quantifies the probability of a soft error occurring as a function of LET and serves as a well-established metric for radiation sensitivity. Comparison of our simulation-based cross-section predictions with existing experimental data demonstrates strong correlation, validating the accuracy and reliability of the ROM framework.

However, while the cross-section curve is instrumental in characterizing device sensitivity, it has limited utility in guiding design optimization directly. To translate this data into a mission-specific reliability measure, it is essential to perform reliability analysis that accounts for the operating environment of the device. This includes particle flux

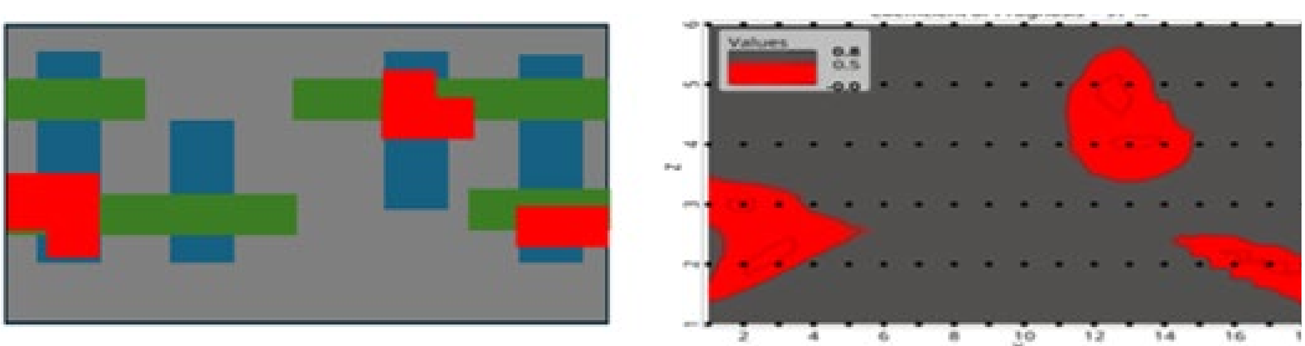

Fig. 2 SRAM layout showing SEE impact on TCAD (left) compared to ROM prediction of bit flip (right)

profiles, mission duration, shielding conditions, and expected error rates under nominal and worst-case scenarios. By integrating cross-section data into a reliability model, designers can estimate FIT rates and use these insights to implement targeted hardening strategies, optimize layout, or select appropriate redundancy techniques.

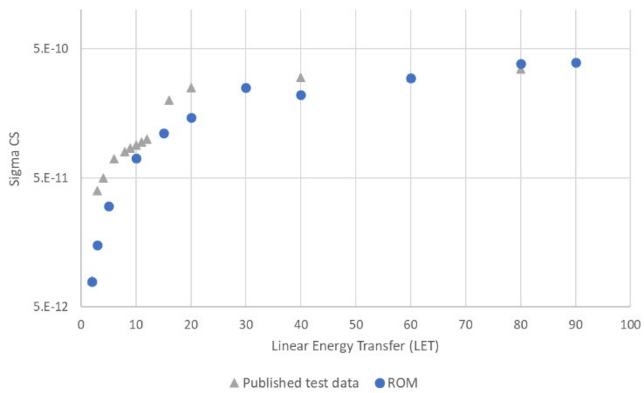

Fig. 3 Comparison of ROM to published cross-section data

V. Reliability Analysis

Reliability analysis was conducted under a defined environmental condition—specifically, the space radiation environment. This study considered a broad range of orbital regimes, spanning from low Earth orbit (LEO) to geosynchronous Earth orbit (GEO). To model the radiation environment, CRÈME96 was employed to generate particle flux distributions based on user-defined orbital parameters, including altitude, inclination, and shielding thickness.First, the sensitivity cross-sectional area determined from the sensitivity analysis (cross section curve) is curve fit using a Weibull distribution function (1).

$$\sigma(x) = A.\left[1 - e^{(-[(x-x_0)/W]^s)}\right] \quad (1)$$

where, x is LET_{eff}, $\sigma(x)$ is the cross-section, x_0 is onset or LET threshold, W is the width parameter, and s is dimensionless exponent.

Then the event rate is obtained by integrating over the cross section and the differential flux as shown in (2).

$$Event\ Rate = \int_0^\infty F(x)\,.\,\sigma(x)dx \quad (2)$$

If we express LET as x, $F(x)$ is the particle differential flux distribution and $\sigma(x)$ is the cross-section.

Sensitivity analysis was performed on a 22 nm FD UTBB FD-SOI by running SEE experiment on a 6-T SRAM [3] and the soft error rate was predicted to be 2.32×10^{-12} /(bit.day). For comparison, the SEE cross section curve measured in [3] was used to estimate the error rate from the reliability analysis. The calculated error rate at GEO condition and with 118 mils shielding was 4×10^{-11} /(bit.day). The reliability prediction is conservative due to difference in environment models relative to those used in [3].

VI. Conclusion

This study presents a novel approach to evaluating radiation-induced vulnerabilities in integrated circuits. The workflow begins with TCAD-based analysis of charge sharing effects and multi-node charge collection in densely packed layouts. Using TCAD simulations, we constructed 3D models of discrete devices and analyze their behavior across a range of LET values. This device-level analysis forms the foundation for a predictive model that accounts for various bias conditions, device sizes, and areas. The core of our methodology lies in discretizing semiconductor components into functional blocks and determining their sensitivity and reliability.

Our research demonstrates the importance of incorporating physical layout information and charge sharing effects in radiation vulnerability assessments. By integrating TCAD simulations, reduced order modeling, and CRÈME96 environment model, the proposed method enables scalable and cost-effective evaluation of semiconductor reliability in harsh environments. The resulting FIT predictions support layout optimization, redundancy planning, and hardening strategies for aerospace and defense-grade ICs.

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