UCIe Full Signal Integrity Analysis Flow with Compliance Check for Heterogenous Integration

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Abstract — Universal Chiplet Interconnect Express (UCIe) standard is important for the future of advanced packaging and semiconductor system design. This paper explores the trends in the industry and Cadence Design Systems complete analysis solutions with UCIe standard compliance checking and verification. This paper details the analysis solution and design architecture with various testcases from Cadence Design Systems and their customers who continually push the industry standards and challenges the existing analysis capabilities currently available.

Keywords — Signal Integrity, 3D Heterogenous Integration (3DHI), Universal Chiplet Interconnect Express (UCIe), UCIe Compliance Checking, Cadence Design Systems, Advanced Interface Bus (AIB), Rapid Assured Microelectronics Prototypes (RAMP), Semiconductors, Silicon Interposer, Systems in Package (SIP), Microsystems, Microelectronics, Clarity, 3D FEM, SystemSI, 2.5D Heterogeneous Design & Simulation, 3D Packaging.

I. Introduction

The increasing complexity and computational demands of 3DHI systems design is challenging to even the best-equipped organizations throughout the industry. On-package chiplets demand significant simulation and increasing design turns, as more designs are packaging multiple components which only a few years ago were discretely packaged. The disparate and deep skillsets of these technologies and the exponentially increasing computational demands of newer process nodes threaten to lengthen design times and increase time-to-market ramps.

This paper and its presentation are organized as follows: First, detail about the UCIe standard and its importance. Second, heterogeneous integration of the interposer is summarized. Finally, the fine-grained simulations and analysis required to close the design are discussed.

II. UCIe Standard Importance

"The Universal Chiplet Interconnect Express (UCIe) is an open, multi-protocol capable, on-package interconnect standard for connecting multiple dies on the same package" [4]. UCIe was defined to provide a standard compliance mechanism to ensure operability and support a wide range of devices with different performance characteristics. UCIe specification covers the die-to-die interconnect and protocols from an interoperable, multi-vendor ecosystem.

Chiplets give designers much greater flexibility by opening new frontiers for reuse and thereby enabling better pricing, performance, and power consumption across the industry. Chiplets are the key to extending Moore's Law through the next decade and beyond [5]. Membership to the UCIe Consortium is open and encouraged to all companies in the industry that want to help enhance the UCIe specification.

III. Heterogenous Integration

The second topic of this paper details heterogenous integration; specifically, the interposer used in this paper, and related to microelectronics Systems In Package (SIP). Gordon Moore believed that a "Day of Reckoning" would come whereas "it may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected" [2]. This is a trend many industry leaders like Intrinsix are pioneering. Fig. 1 shows standard and advanced

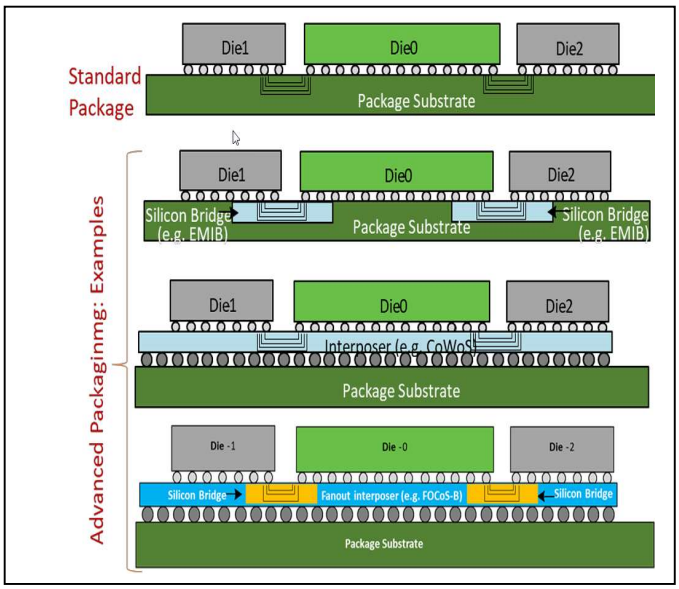


Fig. 1. Multi-Die Advanced Package Module

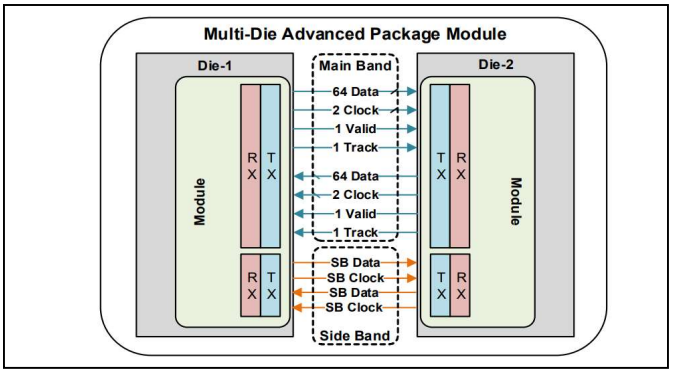


Fig. 2. Multi-Die Advanced Package Module

packaging 2D and 2.5D scenarios. Fig 2. Shows the multi-die advance packaging module interconnect standards.

There are many drivers of on-package chiplets: growing performance demands, lower overall portfolio cost from both a product and project to derive a time to market advantage, enable customer to make tradeoffs for and target specific and different market segments with co-packaging of dies based on functionality. The trends of the industry are to reduce size weight and power (SWAP) and increase performance and capabilities.

flow, the integration of the chiplets on the silicon interposer requires a new design flow to completely model the signal impairments caused by the interposer. Fig. 3 shows the key element in the UCIe interface.

Interposers are complex in nature and this interposer incorporated trace widths of 2um, lengths of 2mm and approximately 600 TSVs (through-silicon-via). The total IO count for 24 UCIe channels on a single die edge is ~2400. The ground planes are "degassed" meaning they are rectangular grids rather than continuous ground/reference planes. This significantly increase the complexity of any EM simulations. Length matching requirements were on the order of 100um < 20ps for each channel's forwarded CLKs and data High speed signal routing was done on two signal layers separated by a degassed ground plain layers.

The main benefits of Die to Die (D2D) interfaces like AIB and UCIe are high data transfer per unit length of die periphery and low power consumption. For example, the power consumption of an AIB channel transferring 40Gbps full duplex is ~40mW or 1pJ/bit/transition. The physical connections are essentially rail to rail CMOS drivers and inverters which simplifies the design and lowers the power consumption. However, this approach violates the well-established principles of high-speed data transfer of having matched impedances on each end of the transmission lines connecting the drivers and receivers.

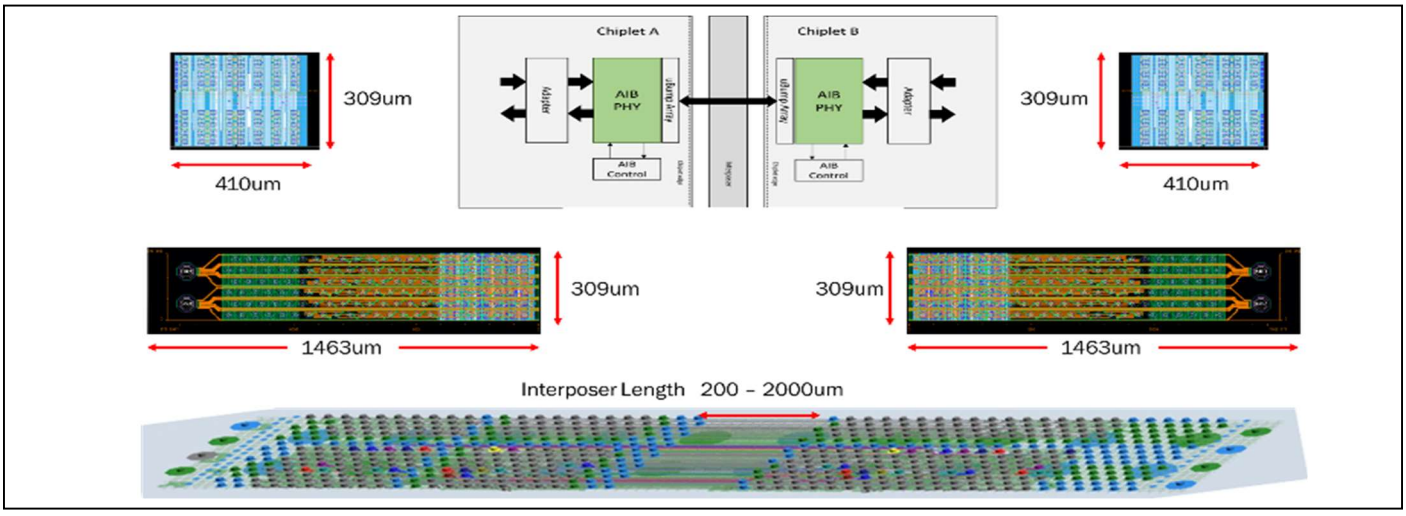


Fig. 3. UCIe Interface – Key Elements

One prerequisite for the large-scale use of chiplets is the emergence of interconnect standards such as UCIe and robust tools and design flows to support the problems unique to chiplets. In this paper we present a silicon interposer that is optimized for 960Gbps data transfer using the UCIe interface. This data rate is achieved by binding 24 UCIe channels together each running at 2Gbps full duplex. A single UCIe channel consists of 96 IO on each chiplet connected to a ubump array with 55um bump pitch. The chiplets are then flipped and mounted on a Silicon interposer which has interconnect lengths up to 2mm. While the design and verification of the IO and ubump array on the chiplets follows a standard IC development

The connection is singly terminated with partial impedance matching due to the driver pull up/pull down resistance and high impedance terminations on the receiver side.

Fig 4. shows the channel model of the UCIe interface. While a single connection can be represented by partial differential equations, the parallel combination of 960 such connections with ground plane discontinuities, imperfect shielding, poor impedance control, cross talk and IR drop requires a full 3D EM simulation to ensure compliance to the UCIe Eye Diagram requirements. It is also important that the Driver and Receiver characteristics are captured faithfully in these simulations

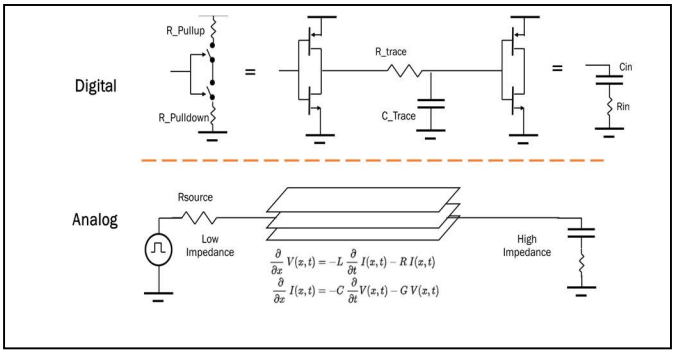


Fig. 4. Channel Model of UCIe Interface

without the need for fully extracted netlists which can easily extend to millions of lines for these advanced nodes.

IV. Full Signal Integrity Flow for 2.5D HI Design

The third and final topic is full simulation and analysis software related to signal and power integrity. Cadence multi-physics systems analysis (MSA) signal integrity (SI) software was utilized for the full simulation of the design case. Specifically, T2B (transistor to behavioral), SystemSI UCIe Compliance Kit and Clarity3D Layout. T2B was used to generate the IBIS (I/O Buffer Information Specification) model from transistor-level Intrinsix IP design. SystemSI was used for the transient (time domain) analysis and automated UCIe compliance kit checking. Clarity3DL was used for the full wave 3D FEM (finite element method) S-parameter extraction of the UCIe interface routed on the interposer.

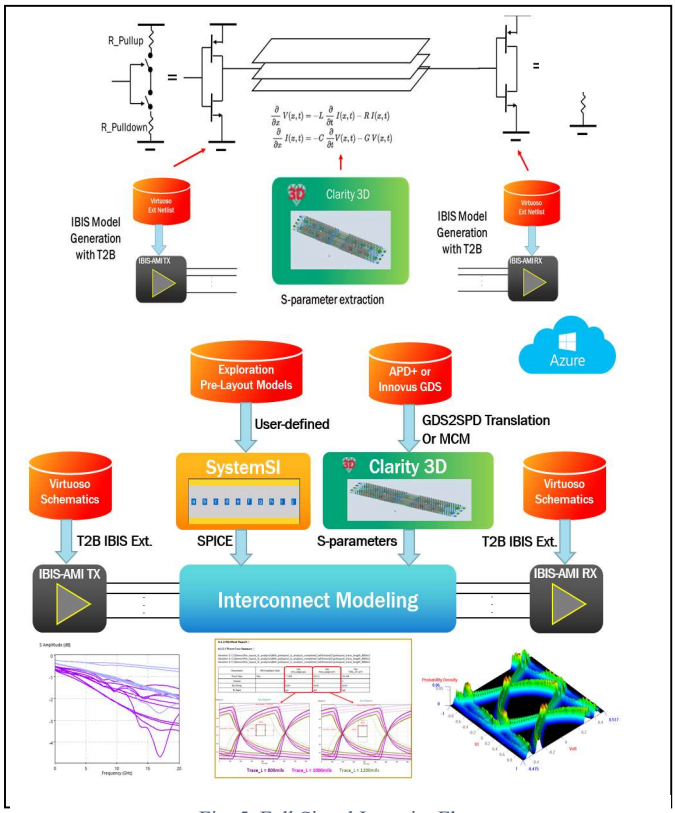
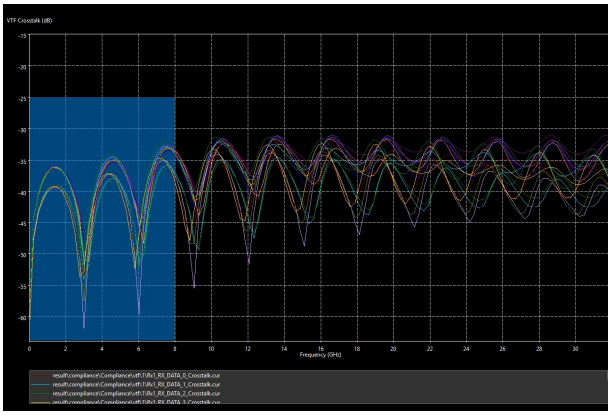


Fig. 5. Full Signal Integrity Flow

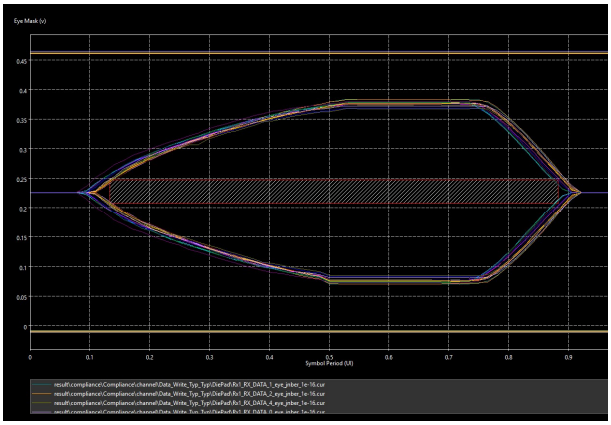
The complexity of the interposer design geometry makes it a challenge for simulation technology. Degassing planes, reference plane continuity, shielding, impedance control, crosstalk, DC/AC analysis and 3D FEM extraction is required for analysis. S-parameter extraction for UCIe nets is from DC to 25GHz.

How does one go about and model this? It consists of mainly three parts. The first one is IBIS-AMI models for the TX drivers RX blocks for each signal path in the UCIe channel. Cadence T2B was used to create IBIS models based on fully extracted Spectre netlists derived from the Intrinsix IO cell designs. These extracted netlists contain millions of lines that can be replaced by IBIS models with minimal loss in simulation accuracy. This results in reduction of simulation times from multiple hours to seconds. The second part is to generate a full wave 3D FEM model for the silicon interposer interconnect. Cadence Clarity 3D Layout extraction was used to generate an S-parameter model that was a realistic 3D FEM result from the interposer layout design. This simulation contained 43 ports, nearly 7 million elements and approximately 42 million unknowns. The total simulation time was slightly under 8hrs.

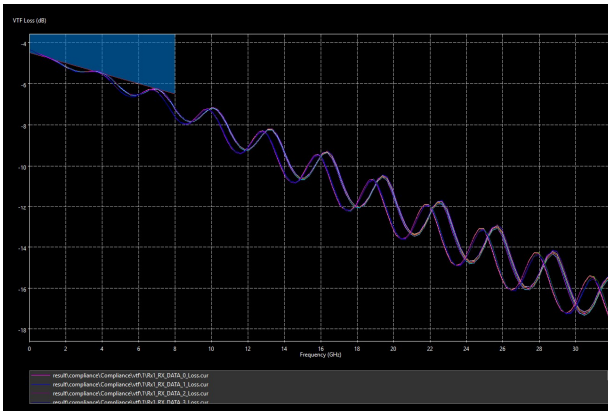
The third requirement is to run a transient analysis to generate eye diagrams, UCIe compliance checks and handle various model formats i.e., SPICE, IBIS, S-Parameter, layout files and/or others and simulate them. Cadence SystemSI was utilized for this purpose and would handle all these simulation models from one user cockpit that is used to collect, simulate, and analyze the various model inputs and then generate the reports with compliance checking for verification and validation. Compliance is needed for data rates up to 6.4 Gbps. The flow allows analysis and optimization of channel eye diagram capturing subtle affects like over-shoot, cross talk, clock, and data skew and transmission line reflections. Figure 6 shows the simulation flow and resulting eye diagrams, and UCIe Compliance Masks for Eye Diagrams (Fig. 6 b) VTF Loss (Fig. 6c and VTF Crosstalk (Fig 6a). Note that parasitic effects such as cross coupling and reflection within the interposers are the main causes of signal impairments. This can be seen clearly by contrasting the eye diagram in Figure 6 (b).



(a)



(b)



(c)

Fig. 6. UCIe Compliance Kit Eye Diagram, VTF Loss, VTF Xtalk Results

V. Conclusion

A detailed design flow to support data transfer rates of 960 Gbps over 24 AIB channels was presented and compliance with UCIe Standard was completed. This flow allows detailed simulation of transmission line affects on an interposer. Cadence Sigrity/Clarity, Allegro and Virtuoso platforms were required to comprise Full flow including a full 3D Extraction for an 8-layer silicon interposer. Additionally, an easy-to-use UCIe Compliance Kit saved hours of engineering work to build a circuit test-bench with extractions simulations and circuit simulations that are scalable with core count.

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