Using UCIe Channel Compliance Simulation for Understanding Substrate/Interposer Design Tradeoffs

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Abstract

Recent advances in IC packaging technology such as 2.5D and 3D integration have enabled the use of smaller dies known as chiplets. Unlike system-on-chip (SoC) designs which are constrained to a single process technology node and large die areas which yield poorly, chiplet-based system-in-package (SiP) designs may incorporate many smaller dies from different processes and technology nodes. The Universal Chiplet Interconnect Express (UCIe) standard provides the most comprehensive protocol for chiplet-to-chiplet communication. It specifies two interconnect channel requirements: VTF Loss and VTF Crosstalk, as well as a receiver eye mask requirement that incorporates both channel and equalization effects. Using the minimal equalization requirements from the UCIe standard during channel compliance SI simulation may underestimate actual receiver eye performance. This is because typical UCIe IP PHYs will likely offer more powerful equalization capabilities. Therefore, to make the right design tradeoffs between cost, SiP floor planning, and electrical performance, it is crucial to identify all forms of equalization available from the vendor's UCIe PHY IP and incorporate them into the UCIe channel compliance simulation of the receiver eye.

Key words

Chiplets, Signal Integrity, UCIe, Channel Equalization

I. Introduction

The semiconductor industry is witnessing a paradigm shift as chiplet-based architectures emerge as a compelling solution to sustain computing advancement beyond traditional Moore's Law scaling. This advanced packaging technology enables continued improvements in chip performance and I/O capabilities by disaggregating complex systems into smaller, more manageable die components. From a signal integrity (SI) perspective, chiplet interconnects present both advantages and unique challenges compared to traditional PCB implementations. While these interconnects benefit from shorter electrical paths and predominantly point-to-point topologies, they must contend with substantially higher transfer rates, increased substrate and interposer losses, and densely packed routing channels supporting wider data buses. The criticality of accurate signal integrity simulations for chiplet-based systems cannot be overstated, particularly when evaluating substrate and interposer design tradeoffs. These simulations become especially crucial given that physical validation through probing—a relatively straightforward task with traditional PCB traces—is virtually impossible with the microscopic, encapsulated traces typical of chiplet implementations. Moreover, the substantial costs and extended lead times associated with substrate and interposer manufacturing mandate a "first-time-right" approach, further emphasizing the vital role of comprehensive SI simulation in the design process. This necessity for precise simulation is amplified by the increasing complexity of modern chiplet interconnect architectures, where even minor design oversights can lead to significant performance degradation or complete system failure.

In this paper, the authors discuss the Universal Chiplet Interconnect Express (UCIe) specification [1] as a protocol for chiplet communication, the role of channel compliance simulations in UCIe electrical design sign-off, and correlation between channel compliance and I/O Buffer Information Specification – Algorithmic Modeling Interface (IBIS-AMI) [2] based simulations. For a Standard Package operating at 16GT/s, simulation results are compared

between the cases of minimum equalization required by the UCIe standard versus typical equalization that may be offered by UCIe PHY IP vendors. This paper considers the equalization capabilities offered by Alphawave's AresCORE36 PHY CORE IP [3] which includes a two-tap transmitter FFE and a receiver CTLE. The results indicate that significant timing and voltage margin may be recovered by including relevant equalization capabilities, which may prevent laborious substrate floorplanning iterations or costly upgrades for low-loss dielectrics.

II. UCIe Specification

The UCIe specification encompasses a comprehensive framework for chiplet-to-chiplet communication, addressing aspects from physical layer implementation to protocol-level interactions. This paper focuses specifically on the signal integrity aspects of the specification, as these requirements fundamentally determine the achievable performance and reliability of chiplet interconnects.

A. Baseline Assumptions and Simplifications

The UCIe specification adopts several significant simplifications in its signal integrity requirements to provide a standardized evaluation framework. The compliance simulations exclude several real-world phenomena that would typically impact high-speed serial links. The specification assumes ideal conditions where jitter and noise contributions are absent from eye diagram analysis. Buffer characteristics are simplified to lumped R and C parameters, eschewing detailed and potentially non-linear I-V and V-t relationships that would typically influence signal behavior. The model further omits several critical non-idealities: equalization-related effects such as receiver variable gain amplifier compression are not considered, clocking impacts are excluded, and simultaneous switching noise (SSN) effects are absent from the compliance framework.

B. Voltage Transfer Function Requirements

The specification defines two fundamental metrics for channel performance: Voltage Transfer Function (VTF) Loss and VTF Crosstalk. These parameters establish the basic requirements for signal transmission quality in chiplet interconnects. The VTF Loss requirement mandates that channel characteristics must remain above a specified maximum loss threshold across the frequency range of interest. Conversely, VTF Crosstalk must remain below maximum specified limits. Both requirements extend up to the Nyquist frequency (fN) for the intended data rate.

These VTF measurements are purely channel-centric, deliberately excluding any equalization effects. A notable aspect of the VTF requirements lies in their implementation: while the maximum VTF Loss threshold remains constant across all interconnects, the maximum allowable VTF Crosstalk varies on a per-net basis, determined by each net's specific loss characteristics at fN. This approach creates a unique maximum crosstalk threshold for each interconnect, reflecting the reality that crosstalk sensitivity varies with channel attenuation.

C. Eye Diagram Requirements

The eye diagram requirements operate under similar baseline conditions as the VTF measurements, with one crucial distinction: they permit the inclusion of equalization effects when such techniques are implemented in the Transmitter (Tx) and/or Receiver (Rx) devices. The specification mandates relatively generous eye width requirements, an approach that appears designed to compensate for the various excluded non-idealities in the compliance model. This compensation mechanism helps ensure robust operation when these systems encounter real-world conditions where jitter, noise, and various non-idealities are present.

An interesting consequence of this framework emerges in practical implementation: a channel may fail to meet VTF Loss or VTF Crosstalk requirements yet still achieve compliant eye width and height measurements when equalization is applied. This apparent contradiction reflects the powerful impact of modern equalization techniques in compensating for channel impairments, while also highlighting potential limitations in relying solely on channel-only metrics for comprehensive signal integrity assessment.

This nuanced relationship between channel-only metrics and equalized performance underscores the importance of considering both aspects in chiplet interconnect design, particularly as data rates continue to increase and channel characteristics and associated impairments become more challenging to mitigate.

III. Channel Compliance Simulations

The evaluation of signal integrity in chiplet interconnects requires careful consideration of multiple equalization strategies and their impact on channel performance. Our simulation framework implements a comprehensive analysis using a channel model specifically designed to represent a marginal case—one that fails both VTF Loss and VTF Crosstalk requirements under baseline conditions. This approach allows us to systematically evaluate the effectiveness of various equalization techniques in improving channel compliance, particularly at the demanding 16 GT/s data rate specified by UCIe. The simulations progressively incorporate different equalization methods, from the minimal requirements outlined in the UCIe specification to more sophisticated vendor-specific

solutions, providing insight into the practical limitations and opportunities for performance optimization in chiplet interconnect designs.

A. Case Study 1: UCIe Standard Package at 16 GT/s

Our baseline simulation adheres strictly to the minimum equalization requirements specified by UCIe. At 16 GT/s operation, while Tx feed-forward equalization (FFE) is recommended, it remains optional, and neither Rx continuous-time linear equalization (CTLE) nor decision feedback equalization (DFE) are mandated. This case study serves to establish a reference point for subsequent analyses and highlights the challenges faced with minimal equalization.

The VTF Loss measurements (Fig. 1) reveal channel degradation beyond the maximum allowable loss, particularly in the critical frequency range approaching the Nyquist frequency (8 GHz). Similarly, the VTF Crosstalk results (Fig. 2) exceed specified limits, indicating potential signal integrity issues in densely routed interconnects.

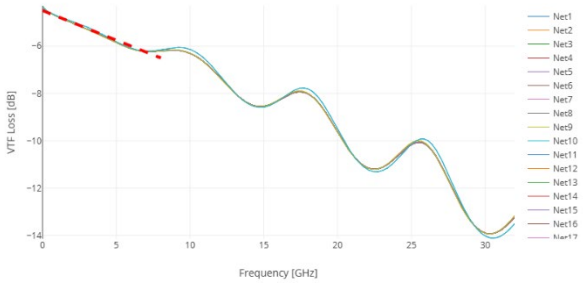

Fig. 1. VTF Loss with UCIe Mask

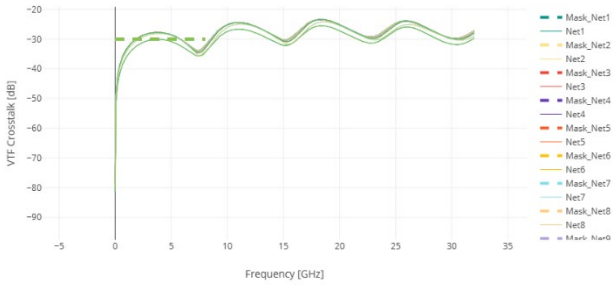

Fig. 2. VTF Crosstalk with UCIe mask

The resulting eye diagram (Fig. 3) exhibits marginal performance characteristics, showing -6 mV eye height margin, and -.0012 UI and -.00145 UI left and right width margin, respectively to the required UCIe spec.

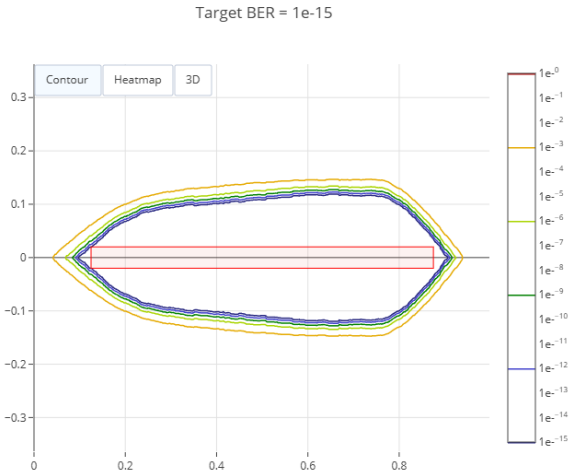

Fig. 3. Eye diagram with minimal equalization showing insufficient margins for reliable operation at 16 GT/s.

B. Case Study 2: UCIe Standard Package with Alphawave Tx FFE

The introduction of Tx FFE represents the first step toward enhanced signal integrity. This Tx FFE design features a -2.2dB de-emphasis, which matches that of the UCIe specification but is not required for Standard Package 16GT/s. While the VTF Loss and VTF Crosstalk measurements remain unchanged—as these metrics specifically exclude equalization effects—the addition of Tx FFE provides notable improvements in signal quality. The resulting eye height margin improved from -6 mV from baseline to -1.5 mV, while the timing margins were slightly worse, -.0031 UI left margin (LM), and -.039 UI right margin (RM).

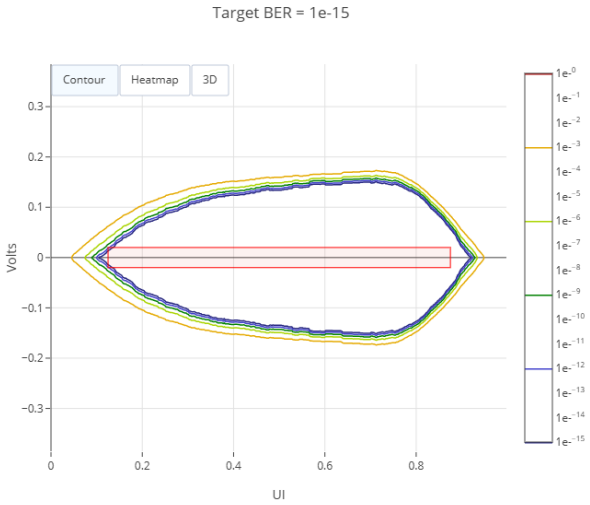

Fig. 4. Eye diagram demonstrating the impact of Tx FFE

C. Case Study 3: UCIe Standard Package with Alphawave Rx CTLE

This configuration introduces a receiver CTLE, characterized by approximately 12dB of DC gain for signal amplitude recovery and inductive frequency peaking centered at approximately 8 GHz.

The eye diagram (Fig. 5) shows substantial improvement in both vertical and horizontal margins, improving to +25 mV in eye height margin, +.0114 UI LM, and +.0339 UI RM. Note again that the VTF loss curves remain unchanged from the baseline (as EQ is not considered).

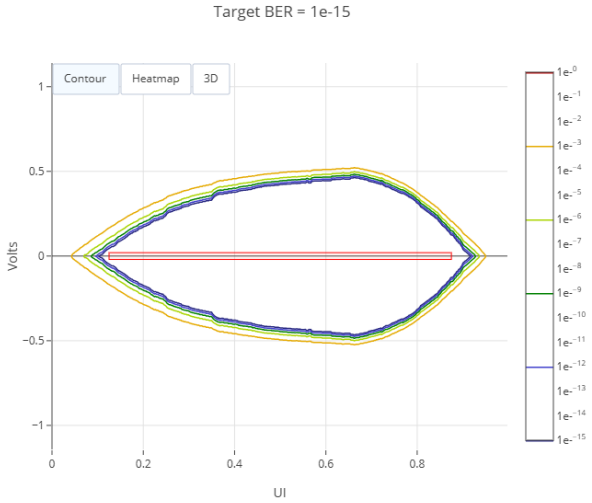

Fig. 5. Eye diagram showing significantly enhanced performance through Rx CTLE.

D. Case Study 4: Combined Tx FFE and Rx CTLE Implementation

The integration of both Tx FFE and Rx CTLE capabilities represents a comprehensive equalization approach. With both Tx FFE and Rx CTLE enabled, the eye (Fig. 6) improved to +25 mV eye height margin, +.0114 UI LM, and +.034 UI RM.

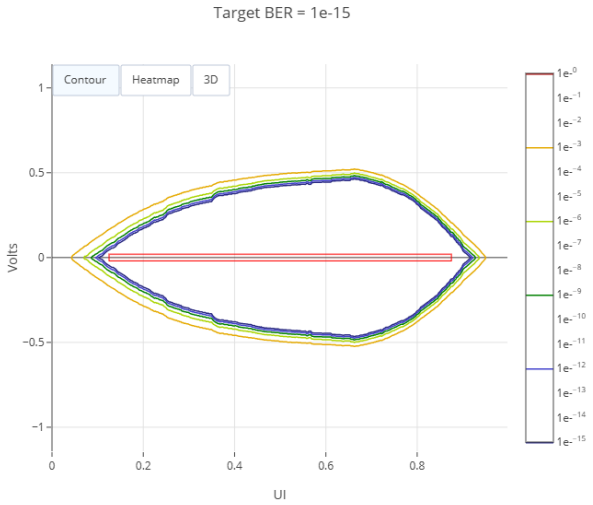

Fig. 6. Eye diagram demonstrating the cumulative benefits of combined Tx and Rx equalization strategies.

E. Case Study 5: UCIe Standard Package with Alphawave Equalization and Hypothetical 1-Tap DFE

The addition of a hypothetical 1-tap DFE to the existing equalization scheme represents the most sophisticated configuration tested, and this results in post-cursor ISI cancellation through feedback. It also allows for adaptive threshold adjustment for optimal symbol detection. The resulting eye (Fig. 7) shows the highest margins in both eye height and eye width, with +44 mV eye height margin, +.0205 UI LM, and +.041 UI RM.

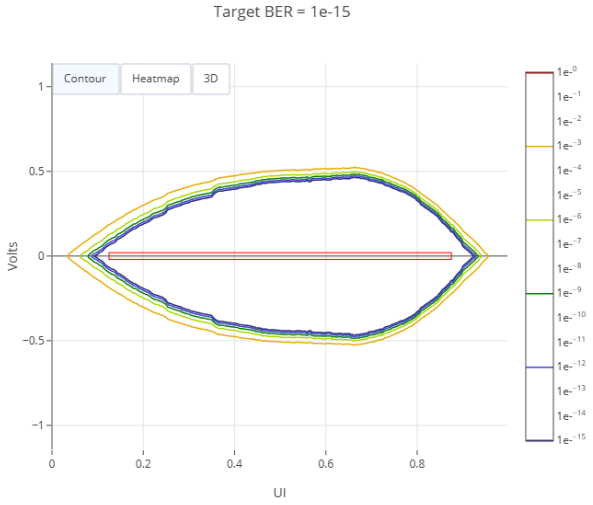

Fig. 7. UCIe Eye with Tx FFE, Rx CTLE, and 1-tap DFE.

Our analysis reveals several critical insights for chiplet interconnect design. The minimal equalization requirements specified by UCIe, while providing a baseline for interoperability, potentially underestimate the channel's true

capabilities. The specification's inherent ambiguity regarding equalization implementation creates uncertainty in performance expectations and complicates the design validation process.

The progressive improvement observed through various equalization combinations suggests that a holistic approach to equalization strategy is essential for optimal performance. Vendor-specific equalization capabilities, when properly implemented, can substantially improve margin results, providing a more accurate assessment of design viability and potentially enabling more aggressive interconnect architectures.

These findings carry significant implications for future chiplet interconnect designs, suggesting that equalization strategies should be considered early in the design process to ensure robust performance at increasing data rates.

IV. Correlation with IBIS-AMI

While UCIe channel compliance provides a foundational framework for signal integrity assessment, more sophisticated analysis methods, particularly IBIS-AMI simulation, offer opportunities for detailed, vendor-specific performance evaluation.

Initial IBIS-AMI simulations can be configured to closely parallel UCIe channel compliance conditions, providing a basis for comparative analysis. The statistical simulation flow, while maintaining the simplified approach of excluding impairments, offers greater insight into system behavior through vendor-specific models. Fig. 8 illustrates the eye diagram results using this methodology.

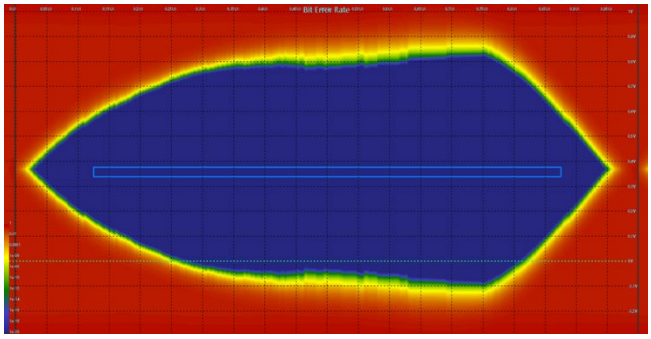

Fig. 8. Statistical eye diagram from IBIS-AMI simulation showing enhanced detail compared to basic UCIe compliance analysis.

Future IBIS-AMI simulations should incorporate several critical impairments not addressed in this analysis. Random and deterministic jitter, along with simultaneous switching noise (SSN), become increasingly significant in dense chiplet implementations. Clocking effects, particularly jitter transfer and clock recovery interaction with equalization, warrant investigation. Additionally, non-linear behaviors such as receiver amplifier saturation can significantly impact equalization effectiveness, especially where large peaking factors are employed. Understanding these relationships becomes crucial as signal swings decrease to meet power constraints while channel losses increase at higher data rates.

V. Conclusion

The design and implementation of chiplet-based systems increasingly depends on accurate signal integrity simulation to inform critical design decisions and ensure first-time-right success. This requirement becomes particularly acute given the substantial costs and extended lead times associated with substrate and interposer manufacturing.

Our simulation results demonstrate how channel compliance analysis directly influences design decisions. When considering only the minimal equalization requirements specified by UCIe, signal integrity engineers might be compelled to recommend costly modifications, such as floor plan reconfiguration for shorter routing lengths or the adoption of premium substrate materials. However, incorporating the full range of vendor-specific equalization capabilities, exemplified by the Alphawave AresCore 16 GT/s implementation, can substantially improve both timing and voltage margins, which are often sufficient to avoid such costly system modifications while maintaining robust performance.

The UCIe channel compliance framework serves as a valuable starting point for signal integrity analysis. Its streamlined approach enables rapid preliminary assessment without requiring deep signal integrity expertise, while providing useful channel design guidelines. However, important limitations exist; channels may fail VTF Loss or VTF Crosstalk requirements yet achieve compliant eye width and height measurements when equalization is applied. Additionally, the simplified simulation configuration may lead to conservative design choices that result in suboptimal system implementation.

These findings suggest that while UCIe channel compliance provides a foundation for initial assessment, comprehensive signal integrity analysis should incorporate vendor-specific equalization capabilities and detailed channel characteristics. This approach enables more accurate performance prediction and can prevent unnecessary design modifications, ultimately supporting more efficient and cost-effective chiplet-based system implementation. As data rates continue to increase, the ability to leverage all available equalization capabilities while maintaining interoperability will become increasingly critical for successful implementation.

Acknowledgment

TBD

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