Fine-Pitch RDL with High Reliability Formed on Glass for Heterogeneous Integration

Takamasa Takano, Satoru Kuramochi, Hidetoshi Iioka, Takao Shindou
Dai Nippon Printing Co., Ltd.
250-1, Wakashiba, Kashiwa-shi, Chiba 277-0871, Japan
Ph: +81-4-7134-1208
Email: Takano-T5@mail.dnp.co.jp

Abstract

As AI cloud systems and high-speed data transfer systems are expected to become more advanced, mass-produced, and high-speed in the future, chiplet-compatible interposers are attracting attention as semiconductor mounting packages required for AI data servers. In this paper, we report on the development of RDL(Redistribution Layer) interposer suitable for high density, fine wiring, and high-speed transmission, as well as on the formation technology of fine wiring at 2-μm pitch, protective film formation technology to ensure reliability, and demonstration results in a 300 x 400 mm size to accommodate the increase in chip size (13 cm^2). Furthermore, we conducted electromigration tests on our proposed inorganic dielectric-coated wiring (wiring widths of 1 μm and 2 μm) and demonstrated that it exhibits superior electromigration result compared to conventional wiring.

Key words

High-speed data transmission, High reliability, Fine line RDL, Large chip size, Inorganic dielectric-coated wiring, Electromigration.

I. Introduction

As electronic product becomes smaller and lighter with an increasing number of functions, the demand for high density and high integration becomes stronger. As AI cloud systems and high-speed image transfer information processing systems are expected to become more advanced, mass-produced, and high-speed in the future, chiplet-compatible interposers are attracting attention as semiconductor mounting packages required for AI data servers [1].

Fig.1 shows the packages using the glass materials we are developing. Previously, we announced a fine-wiring structure at the glass panel level [2]. On the other hand, fine-wiring interconnects with a width of 2 μm or less have the issue of decreased reliability caused by copper migration. In [3][4], the authors reported an interposer that enables the formation of fine and highly reliable wiring on a glass substrate coated with an inorganic material to address this issue.

Fig. 2 illustrates the structure of the fine-wiring covered with the inorganic material and the evaluation results of its reliability. Fig. 2(c) shows that the wiring covered with inorganic material gave better High Accelerated Stress Test (HAST) results than the normal structure.

Fig.3 shows the results of high-temperature storage comparing the conventional structure and our proposed structure. After the high-temperature storage test (HTS), our proposed structure (Dai Nippon Printing - Semi additive process) exhibited no change in electrical resistance in the line width range of 0.7 to 1.2 μm, compared to the conventional structure.

In [5], the authors reported the high-frequency characteristics of through glass via (TGV). We concluded that the TGV characteristics exhibit sufficient performance to achieve high-speed transmission up to 10 Gbps.

In this way, we have previously developed TGVs with excellent electrical properties and RDLs with outstanding long-term reliability. By combining these, we have the potential to meet various requirements for next-generation packages.

In this paper, we first discuss the warpage suppression effect of RDL mold formation. Next, we introduce an example of creating fine wiring (L/S = 2/2 μm) with inorganic dielectrics on a build-up layer on a glass core, with a panel size of 300 × 400 mm. Finally, we conducted

electromigration tests on our proposed inorganic dielectric-coated wiring (wiring widths of 1 µm and 2 µm) and demonstrated that it exhibits superior electromigration result compared to conventional wiring.

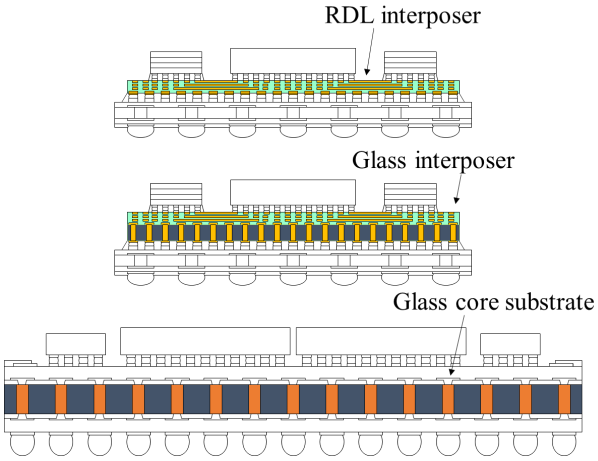


Fig. 1 Our developed package substrate with glass material

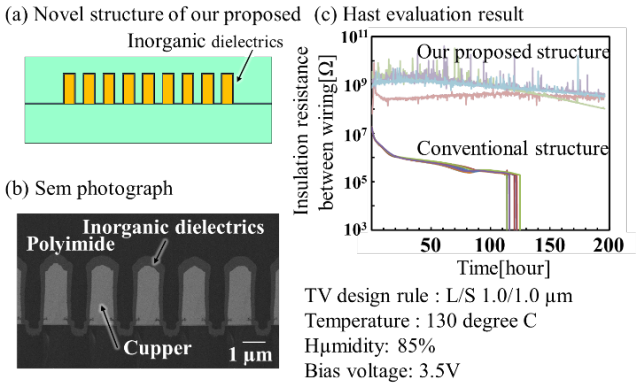


Fig. 2(a) The structure of our proposed structure with inorganic material (b)SEM photograph of the wiring cross section (c) HAST evaluation result

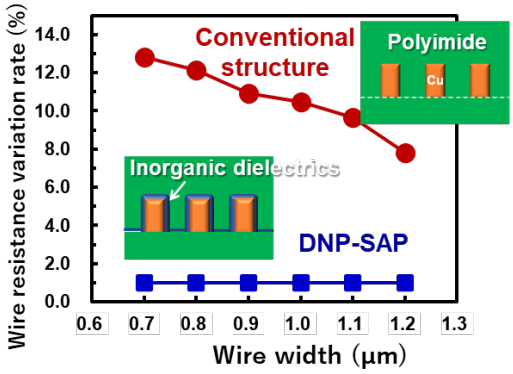
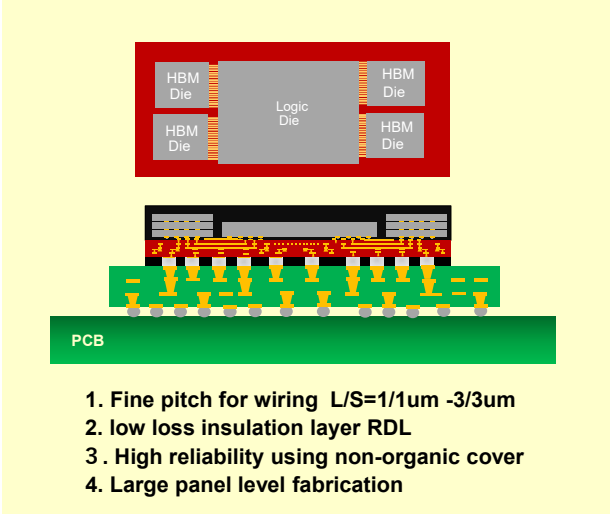


Fig. 3 Change in electrical resistance of Cu traces in high-temperature storage tests under JEDEC standard conditions (JESD22-A103E): 150 ℃,1000 hours, in air.

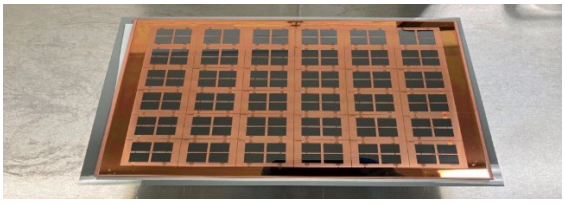
II. Development of Large Panel-Sized RDL Technology

A. Concept of development

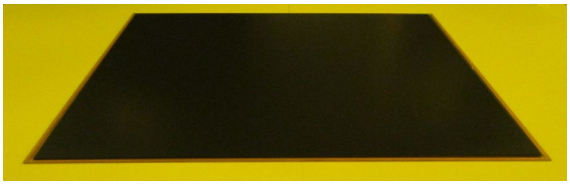
Fig. 5(a) shows schematic structure and feature of RDL Interposer for high performance computing. We fabricate reliable fine wiring protected by inorganic dielectrics on a panel size of 300 × 400mm. Fig.5(b) shows an example of a chip mounted after RDL formation. Fig. 5(c) shows after mold and carrier release.



(a)



(b)



(c)

Fig. 5 (a) Schematic structure and feature of RDL Interposer (b) Fine wiring on panel glass (c) After mold and carrier release.

Fig. 6 shows basic process flow of RDL interposer. First, a release layer is formed on the glass (a). Next, the RDL layer is formed (b). Thirdly, a chip is mounted on the surface of the RDL(C). After that, the chip is molded (d). Finally, the carrier glass is released (e). Also Fig. 7 shows Process flow of RDL layers. First, seed layer formation on lower steps on

the insulation layer. (a) Secondary, Photo resist formation and open the wiring area with developer. Thirdly, electro-plating applied open area of photo resist. (c) After resist striped(d), seed layer metal was etched. (e) And then inorganic layer deposit on the Cu trace(f). It is original process for high reliability of the RDL layer. After insulation layer formation, inorganic layer was dry-etched through opening area of insulation layer. Finally micro bumps formation on the top layer. [6]

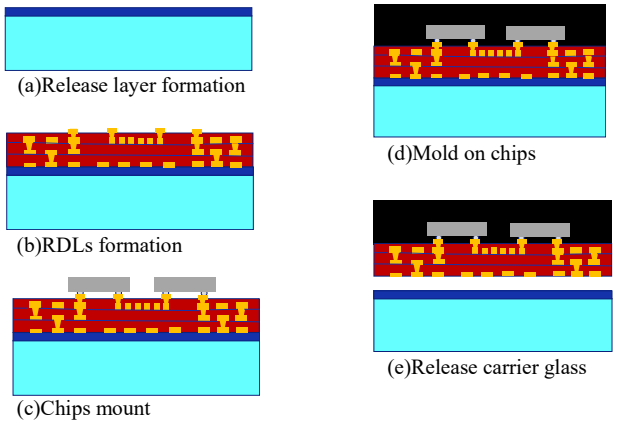


Fig.6 Process flow of RDL interposer.

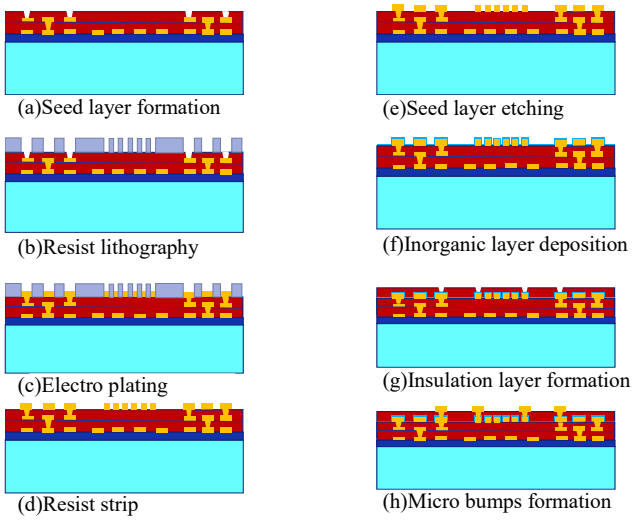


Fig. 7 Process flow of RDL layers.

B. Warping Behavior and Corrective Function of RDL Interposers in Mold Formation

Fig. 8 shows an example of forming a mold on a 300 × 300 mm RDL interposer. In this case, a 500 µm-thick mold was applied to the RDL with a total thickness of 21 µm. Fig. 9 shows warping profile of Mold resin only. After peeling off from the carrier glass, Mold resin warp with residual stress. On the other hand, Mold resin and RDL structure shows flatter warping than Mold only shown in Fig. 9. It can be observed that the warpage has decreased by approximately 300 µm. This behavior indicates that the RDL interposer has a corrective function for the warpage of the mold. (Fig. 10) [7]

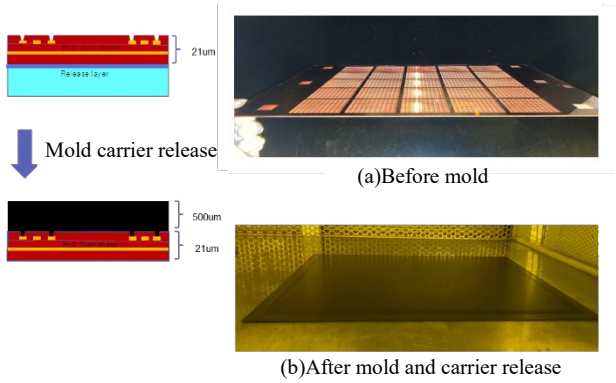


Fig.8 Mold and carrier release on the 300x400mm panel format.

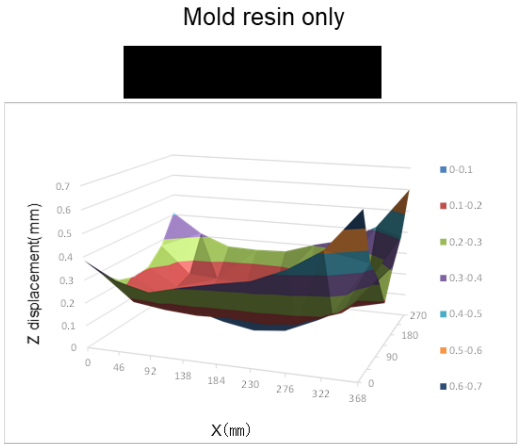


Fig. 9 Warping profile of mold resin.

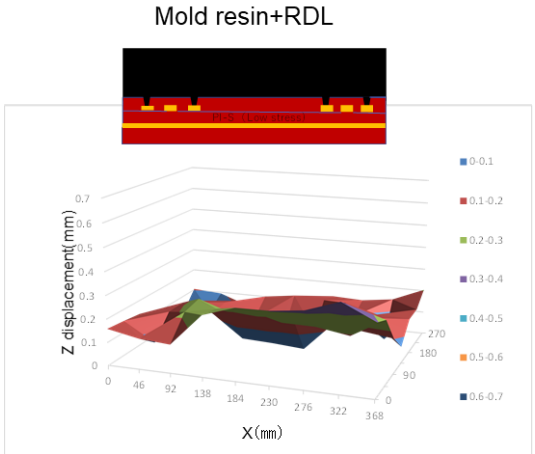


Fig. 10 Warping profile of mold resin and RDL.

C. Demonstration of build-up glass core substrate utilizing proposed SAP

Fig.11 shows a sample of fine wiring (L/S=2/2 µm) formed on a glass core at a size of 300 × 400 mm. Also Fig.12 shows Schematic structure and specification of glass core substrate. TGVs with a diameter of 100 µm were arranged at a pitch of 1mm, resulting in the formation of approximately 15,000 vias within an area of 13cm². Two layers with a L/S of 100/100 µm were formed on the glass core, followed by an additional layer with an L/S of 2/2 µm. For this demonstration, we placed only one chip within the 300 × 400 mm area. However, by changing the panel design, it is possible to fabricate multiple chips simultaneously. Fig. 13 shows a diced 13 × 13 cm chip. It can be observed that the chip has been singulated without any defects such as SEWARE. This structure enables direct chip mounting on the glass core substrate.

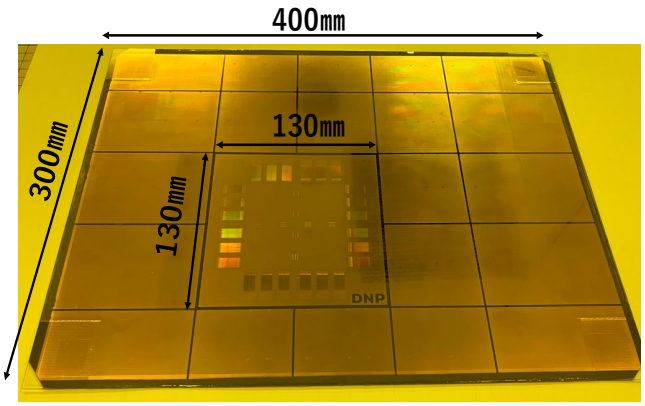


Fig.11 Fine wiring on a glass core fabricated at a size of 300 × 400 mm.

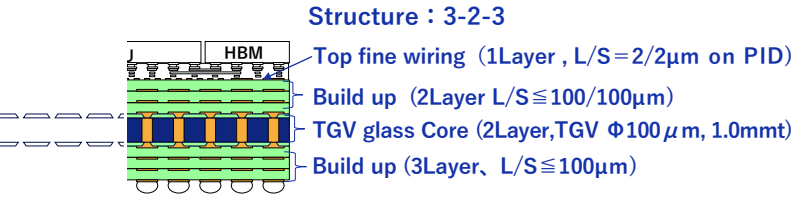


Fig.12 Schematic structure and specification of glass core substrate

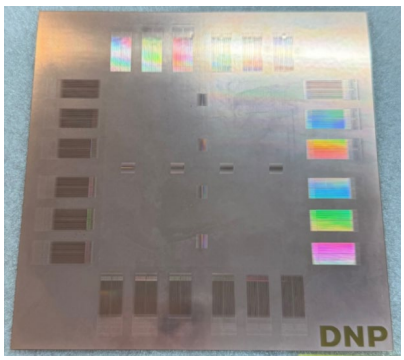


Fig.13 13 × 13 cm substrate after dicing.

III. Electromigration Reliability

A. Electromigration testing monitor.

Fig. 14 shows planar (a) and cross-sectional (b) schematic illustrations of the monitor used in the electromigration (EM) reliability testing. The monitor pattern was via-line-via, which is commonly used in EM testing of LSI interconnects. The Cu traces were 1 or 2um wide and 1600 um long. We also prepared conventional samples: Cu RDLs based on SAP with a line width of 1 or 2um. The Cu traces of the control samples were directly covered with the same type of polyimide used for the Our proposed samples.

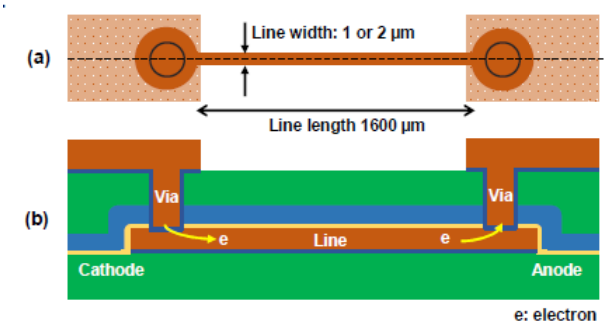


Fig.14 Planar (a) and cross-sectional (b) schematic illustrations of EM monitor with via-line-via structure.

B. Electromigration testing

Fig. 15 shows the change in the increase rate of the electrical resistance of current-stressed 2-µm-wide Cu traces at a background temperature of 130°C. The current densities for the conventional structure and Dai Nippon Printing - Semi additive process (DNP-SAP) were 2.0E6 A/cm2 and 2.5E6A/cm2, respectively. For the DNP-SAP, the current density of 2.5E6 A/cm2 increased the temperature of the Cu traces from 130°C to 230°C due to the effect of Joule heating while that of 2.0E6 A/cm2 for the conventional structure increased the temperature to 180°C. The increased temperatures were estimated by measuring the change in electrical resistance. For the conventional structure, the increase rate of the electrical resistance reached the failure criterion of +20% within 10 hours. In contrast, the increase rate for the DNP-SAP remained at 0% over the 1000 hours stressing time. We also checked the EM resistance for 1-µm-wide Cu traces (Fig. 16). To have the same acceleration for the control sample as in Fig. 15, the current density and the increased temperature of the Cu traces were set to 2.0E6 A/cm2 and 180°C, respectively. For the conventional structure, the increase rate of the electrical resistance gradually increased and reached the failure criterion of +20% within 10 hours. This EM resistance was comparable to that of the 2-µm-wide Cu traces in Fig. 15 since the acceleration was the same. For the DNP-SAP, the increase rate remained at 0% during the stressing time of 1000 hours, indicating that the DNP-SAP is useful for downsizing Cu traces. [8]

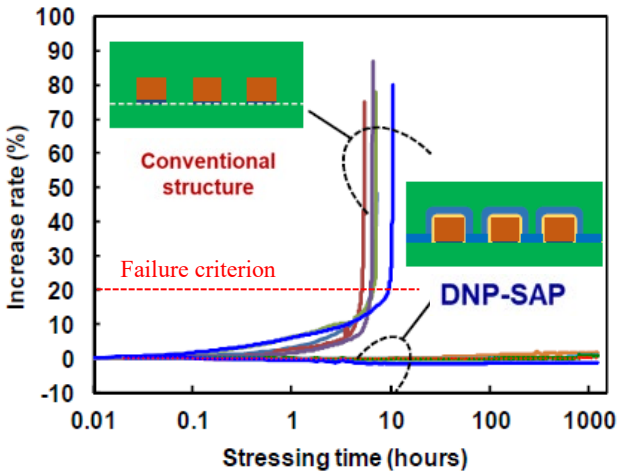


Fig. 15 Change in increase rate of electrical resistance of 2-µm-wide Cu traces stressed with current densities of 2.0E6 A/cm2 for conventional structure and 2.5E6 A/cm2 for DNP-SAP.

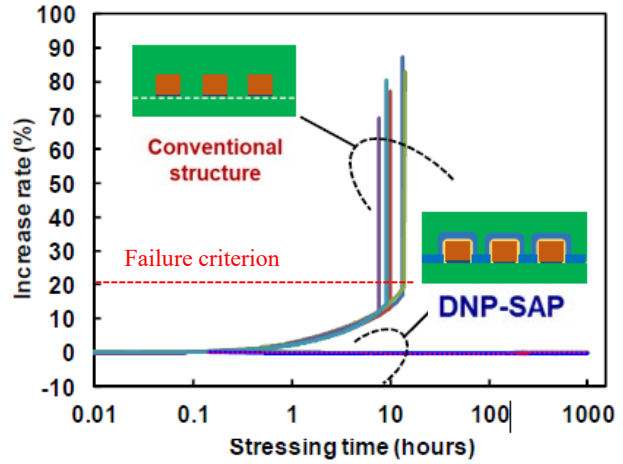


Fig. 16 Change in increase rate of electrical resistance of 1-µm-wide Cu traces stressed with a current density of 2.0E6 A/cm2.

C. Electromigration mechanism

To clarify the mechanism of the EM open failure for the conventional structure sample, we checked SEM images of the trace crosssectionalong the direction of the current flow (Fig.17). The images show many voids dispersed along the top and bottom surfaces of the Cu traces. A void as large as 0.7 µm was detected inside a trace, which is large enough to increase the EM. Close-up image B shows migrated Cu, 0.3 µm thick, on the trace surface (dotted line). The observed voids and the migrated Cu clearly indicate that the open failure was caused by a typical EM phenomenon [9].

We also checked the trace cross-section by using energy dispersive X-ray spectrometry (EDX), focusing on oxygen and copper (Fig. 18). The EDX images show that the migrated Cu was oxidized. In contrast to oxidized Al, oxidized Cu (CuO or CuO2) is porous and vulnerable, and its adhesion force to Cu is quite low [9] The oxidation of the Cu traces might have contributed to the degradation of the EM resistance.

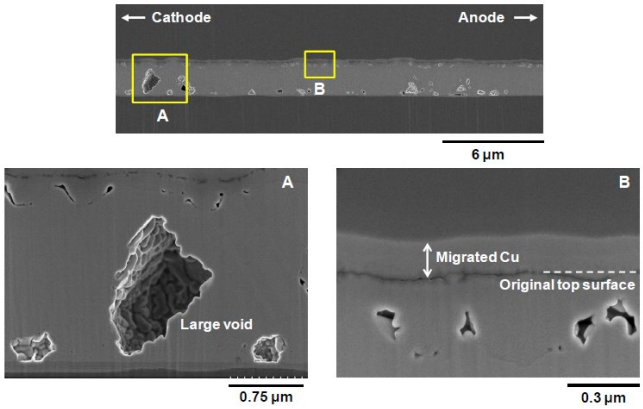


Fig. 17 Cross-sectional SEM image and close-up of control sample of 2-µmwideCu traces stressed with a current density of 2.0E6 A/cm2 at 130°C.

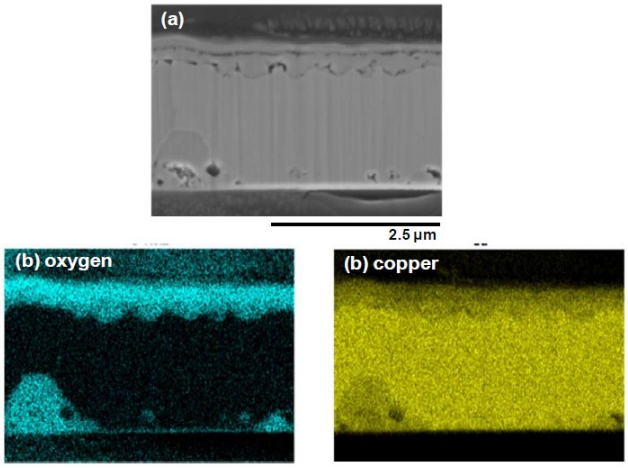


Fig. 18. Cross-sectional SEM (a) and EDX (b) images of control sample with 2-µm-wide Cu traces stressed with a current density of 2.0E6 A/cm2 at 130°C.

For the DNP-SAP shown in Fig.15, we checked its trace cross-section along the direction in the current flow (Fig.19). Voids and migrated Cu, both of which cause EM open failure, were not evident. The close-up SEM image of the top of the Cu traces shows that the first inorganic dielectric solidly adhered to the Cu without any type of failure mode such as dielectric peeling and cracking. These findings demonstrate that the Cu traces were not oxidized in contrast to those of the control sample. The barrier effect of the first dielectric

prevented oxidation of the Cu traces. The first inorganic dielectric constrained Cu migration and prevented Cu oxidation, greatly increasing EM resistance. The demonstrated interfacial modification of the Cu traces thus enhances EM resistance. [8]

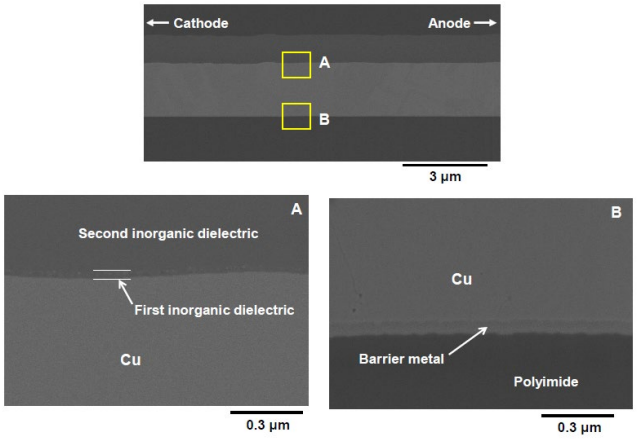


Fig. 19 Cross-sectional SEM image and close-up images of Encore sample with 2-μm-wide Cu traces stressed with a current density of 2.5E6 A/cm2 at 130°C.

Ⅳ. Conclusion

We are developing RDL interposers, glass interposers, and glass cores. This paper reports on the high reliability and future potential of the fine wiring with inorganic dielectrics protection that we propose. In the evaluation of RDL molding, the warpage reduction effect by RDL was confirmed. Additionally, for long-term reliability tests such as HAST and HTS, even at L/S = 1/1μm, better results were obtained compared to conventional structures. Regarding the electromigration test, it was demonstrated that EM resistance significantly increased compared to conventional wiring. Our proposed SAP proved to be useful for the miniaturization of Cu traces. Furthermore, to demonstrate that our proposed SAP can be applied to glass cores and multilayer structures, we fabricated fine wiring on the build-up layer of a 300×400 mm glass core and created a large chip (13×13 cm).

Finally, the glass core substrate we provide enables manufacturing of modules that require a large area. The glass substrate can serve as the ideal structure for 2.3D and 2.5D substrates, which are essential components for the assembly of the next-generation semiconductors. The packaging technology we have developed, with glass material as the core technology, holds great promise for the future. We are committed to further advancing this technology to make it commonplace in the industry.

References

[1] Heterogeneous Integration Roadmap 2021 Edition, Chapter 22 Interconnects for 2D & 3D.

[2] Hiroshi Kudo, Takamasa Takano, Masaya Tanaka, Hiroshi Mawatari, Daisuke Kitayama, Takahiro Tai, Tsuyoshi Tsunoda, and Satoru Kuramochi, “Panel-based large-scale RDL Interposer fabricated using 2-μm-pitch semi-additive process for chiplet-based integration,” IEEE 72nd Electronic Components and Technology Conference (ECTC) pp.836-844, 2022.

[3] Hiroshi Kudo, Ryohei Kasai, Jyunichi Suyama, Mitsuhiro Takeda, Yumi Okazaki, Haruo Iida, Daisuke Kitayama, Toshio Sasao, Kouji Sakamoto, Hiroaki Sato, Shouhei Yamada, and Satoru Kuramochi, “Demonstration of high electrical reliability of sub-2 micron Cu Traces covered with inorganic dielectrics for advanced packaging technologies,” IEEE 67th Electronic Components and Technology Conference (ECTC) pp. 1849-1854, 2017.

[4] Hiroshi Kudo, Takamasa Takano, Kouji Sakamoto, Daisuke Kitayama, Haruo Iida, Masaya Tanaka, Takahiro Tai, Yumi Okazaki, Jyunya Suzuki, and Shinji Maekawa, “Effectiveness of inorganic dielectric layer on submicron-scale Cu Traces against thermal oxidative stress,” IEEE 71st Electronic Components and Technology Conference (ECTC) pp.353-358, 2021.

[5] Masaya Tanaka, Satoru Kuramochi, Takahiro Tai, Yoichiro Sato, Nobutaka Kidera, “High frequency characteristics of glass interposer”, IEEE 70th Electronic Components and Technology Conference (ECTC) pp.601-610, 2020.

[6] Hiroshi Kudo et al., “A chracterized redistribution layer atchitecture for Advanced Packaging technology” Proceeding of 66th Electronic Components and Technology Conference, (2016), pp. 2063-2067.

[7] Takamasa Takano et al., “High Speed Transmission Characteristics of Fine Line Trace on RDL Interposer” Proceeding of 30th symposium on”Microjoining and Assembly Technology in Electronics” (2024), pp. 120-125.

[8] Hiroshi Kudo et al., “Demonstration of High Electromigration Resistance of Enhanced Sub-2 Micron-Scale Cu Redistribution Layer for Advanced Fine-Pitch Packaging” Proceeding of symposium on” IEEE CPMT Symposium Japan” (2017), pp.5-8.

[9] Ehrenfried Zschech, Paul S. Ho, Dieter Schmeisser, Moritz Andreas Meyer, Anand V. Vairagar, Gerd Schneider, Meike Hauschildt, Matthias Kraatz, and Valeriy Sukharev, “Geometry and Microstructure Effect on EM-Induced Copper Interconnect Degradation,” IEEE Trans. On Devices and Materials Reliability, vol. 9, no. 1, pp. 20-30, 2009.

[10] James R. Lloyd, Michael W. Lane, Eric G. Liniger, C.-K. Hu, Thomas M. Shaw, and Robert Rosenberg, “Electromigration and Adhesion,”IEEE Trans. on Devices and Materials Reliability, vol. 5, no. 1, pp. 113-118, 2005.