Fabrication and Packaging of Edge Coupled Silicon Nitride Photonic Integrated Circuits on Glass Substrates for High Performance Interposers

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Abstract
Silicon nitride photonic integrated circuits were fabricated on glass substrates for the first time using reactive ion etched edge facets, demonstrating a minimum propagation loss of 2.4 ± 0.36 dB/cm and minimum edge coupling loss of 2.17 ± 0.79 dB. Two sets of processes were developed: one including high temperature steps (T > 350°C) common to complimentary-metal-oxide-semiconductor (CMOS) foundry front-end-of-line tools and one including low temperature steps (T < 350°C) compatible with CMOS foundry back-end-of-line tools. For both the high and low temperature samples, a CMOS foundry compatible process was also established for dry etching edge facets > 85 μm deep into SiO_2 substrates using magnetically enhanced reactive ion etching with amorphous silicon hard masks without metal. Results show the viability of this glass interposer to help achieve Pbps co-packaged optics switch performance by addressing the material limitations of organic or silicon based interposers and enabling pick-and-place assembly of photonic die to package level integrated photonic waveguides.

Key words
silicon photonics, glass interposer, photonic packaging, edge coupling, co-packaged optics

I. Introduction

The global datasphere is a measure of the total amount of data created, stored, or replicated. In 2025, the global datasphere is estimated to grow to 175 ZB, with 46% of the world's stored data residing in public cloud environments [1]. To meet demand, top of rack (ToR) Ethernet switch packages have doubled total bandwidth capacity every two years [2], with current commercially available packages operating at 102.4 Tbps capacity using 512 electrical input/output (I/O) channels, each operating at 200 Gbps per lane [3, 4]. However, the power consumed by the centimeter long board level Cu traces and the limited pluggable transceiver pitch make continued scaling difficult [5,6]. This is critical when considering the energy consumption of data centers. For example, data centers already accounted for 18% of all energy consumption in Ireland in 2022 and by 2031 roughly 15% of Denmark's energy consumption will be due to data center power usage [7].

The need to reduce Cu length has forced a transition to co-packaged optics (CPO). In CPO, the pluggable transceiver is stripped down to form an "optical engine" - a small optoelectronic package composed of the Si-PIC along with other necessary microelectronics components such as transimpedance amplifiers, Si-PIC drivers, laser drivers, and digital signal processing (DSP) chips [8]. The optical engines are then packaged and assembled side by side with the high performance switch ASIC on the same package substrate. Using this approach, the PCB Cu traces leading from a pluggable transceiver to the switch ASIC are eliminated and the associated improvements in attenuation, latency, crosstalk, and bandwidth density can be realized. This transition is evidenced by the fact that those same commercially available 102.4 Tbps switch ASICs are

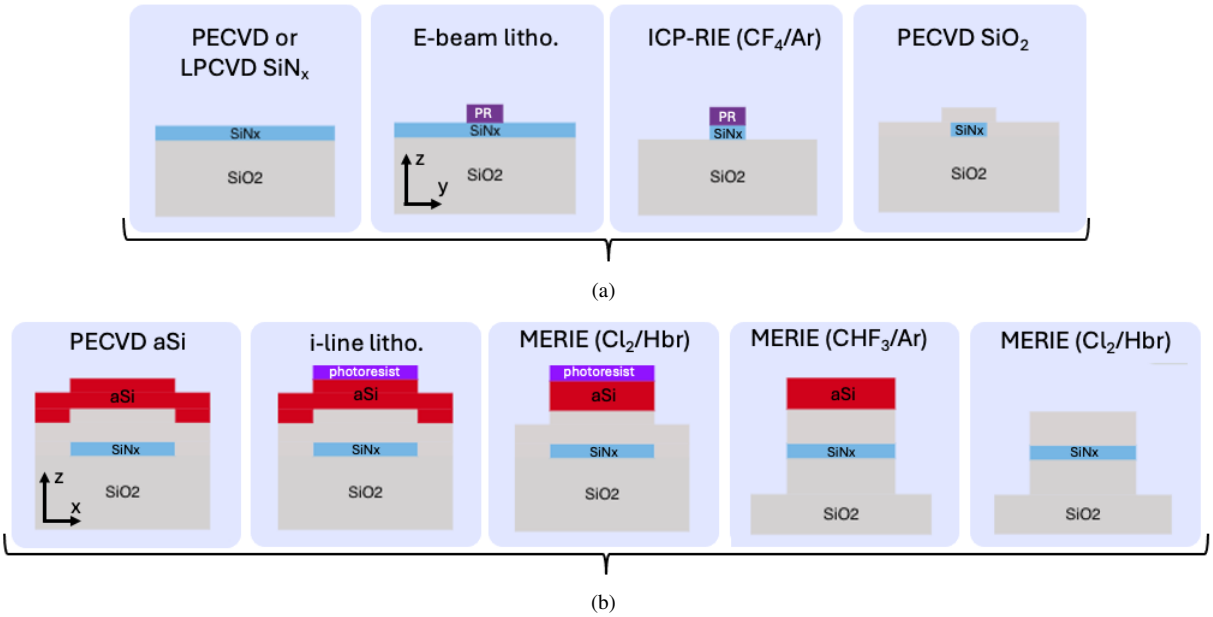
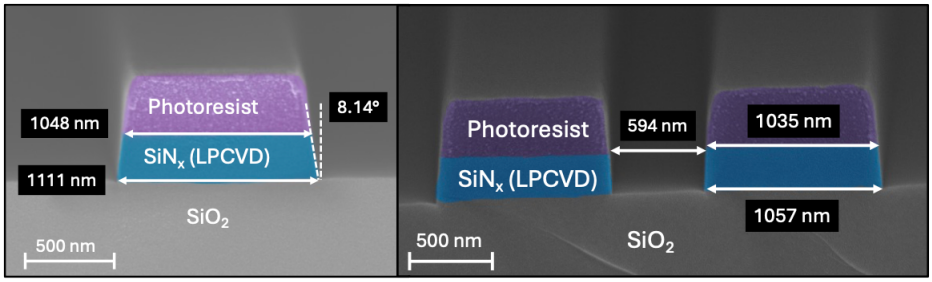


Figure 1: In (a) the procedure for formation of the SiN_x waveguides is shown. While electron beam lithography was used to pattern the waveguides, the feature sizes used were all > 1 μm, which is compatible with photolithography tools dating back to i-line technology nodes. In (b), the process flow for forming edge facets deeper than 62.5 μm such that an SMF array can be aligned to the edge. This edge facet process flow was used for the low temperature samples, while the edge facet process described in [9] (supplementary information) was used for the high temperature samples.

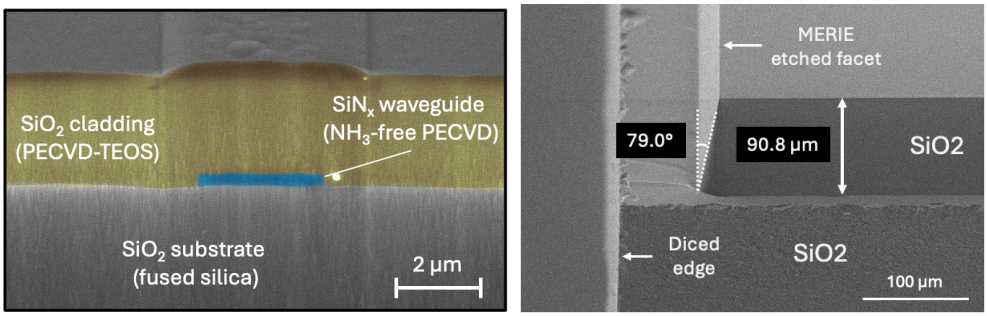
being manufactured with CPO connectivity options [4].

Continuing to scale using CPO presents its own challenges, such as the limitations of today's interposer and package substrate materials on which the ASICs and PICs are bonded. For example, while organic substrates are low cost owing to their manufacturing on > 500 mm panels [10], they suffer from a large coefficient of thermal expansion (CTE) and electrical loss tangent. A common organic such as the Ajinimoto buildup film (ABF) has a CTE > 30 ppm/K [8, 10] and a loss tangent (tanδ) = 0.011 at 5 GHz [8]. In addition, organic substrates have a low Young's modulus (approximately 7.5 GPa for ABF [8]) leading to warpage for thicknesses below 50 μm, which presents an issue for assembly when paired with their high surface roughness (typically > 0.4-1 μm [11]). Silicon (Si) substrates present a solution in many respects, boasting low electrical loss (tanδ < 0.003 [12]), CTE (2.6 ppm/K [13]), and surface roughness (< 10 nm [11]) along with a high Young's modulus (130 GPa [14]). It is for these reasons, as well as the fact that traces can easily be patterned with linewidth/spacing (L/S) < 1/1 μm and with through-silicon-via (TSV) diameters of 10 μm, that Si substrates are used in the highest performance interposers today [8]. Their downside is that they are costly - they can effectively only be manufactured on 300 mm wafers. In addition, future CPO systems may require photonic integration (i.e. waveguides and devices) at the package level in order to overcome the same attenuation and latency related issues in Cu traces for data rates >> 200 Gbps per lane. And yet, both Si and organic substrates are restricted in terms of their allowable photonic integration. For instance, the high refractive index of Si (3.48 at 1550 nm wavelength [15]), means that waveguides require either a Si rib waveguide or the costly deposition of a thick silicon dioxide (SiO_2) layer to act as a waveguide cladding for a different waveguide core material. Organic substrates see a similar issue - the only option is to fabricate waveguides with polymer cores on the surface, creating a low refractive index contrast system which does not allow for dense optical routing.

Glass substrates, and in particular fused silica (pure SiO_2), contain significant advantages over organic or silicon substrates for use as interposers and package substrates in data- and tele-communications systems. This high performance stems from the low optical absorption in the 850-1550 nm range (k < 10^{-5} at 1550 nm [16]), low electrical loss (tan(δ) < 0.005 up to 325 GHz [17]), low refractive index (n = 1.44 at 1550 nm [16]), low coefficient of thermal expansion (5.6 ppm/K [13]), low surface roughness, and ability to manufacture at the panel level [18]. Due to these advantages, there has been significant research on glass interposers; for instance, the formation of dense electrical through glass vias has been shown [19], as has the use of low refractive index contrast waveguides fabricated using ion exchange [20] or ultrafast laser inscription [21]. However, to date there has been only two instances of silicon based waveguides, which have a high refractive index contrast (Δn = 0.45-2), being fabricated on glass substrates [9, 22], and



(a)



(b) (c)

Figure 2: In (a), cross sections show open linewidth features with nominal 1 μm width (left) and 1 μm wide features with 600 nm coupling gaps (right). In (b), the dry etched edge facet with a 3 μm wide SiN_x edge coupler. The yellow region represents the PECVD-TEOS cladding while the blue region represents the PECVD SiN_x waveguide and the gray region below is the original SiO_2 substrate. In (c) SEM images of the glass die corner show the smooth, MERIE defined facet going down nearly 90 μm into SiO_2 and the rough, diced facet below it.

only one involving edge coupling [9]. The goal of this work was to build on our recent results [9] and establish a fabrication process for silicon nitride (SiN_x) waveguides on fused silica substrates, including integrated edge couplers, to determine the manufacturing feasibility of such glass interposers.

II. Device Fabrication, Edge Facet Etching, and Testing Setup

Two separate waveguide fabrication processes were used to fabricate SiN_x photonic integrated circuits (PICs) on glass substrates: one utilizing high temperature processes (> 350°C) and the other with low temperature processes (< 350°C). The generalized process flow for waveguide and edge facet fabrication on both the high and low temperature samples is shown in Figure 1. The high temperature process involved using 500 μm thick, 100 mm fused silica wafers with 220 nm SiN_x films (n = 2.16 ± 0.003 at 1550 nm) grown using low pressure chemical vapor deposition (LPCVD). Waveguides (1 μm wide) were fabricated using electron beam lithography followed by inductively coupled plasma reactive ion etching (RIE) according to the process flow described in [9]. Cross sectional scanning electron microscope (SEM) measurements demonstrated 1 μm open linewidth features, as well as coupling gaps down to 500 nm, with sidewall slopes of ranging from 6.78°to 8.14°. A few images are shown in Figure 2(a) for 1 μm open linewidth features and 1 μm wide features with a 600 nm coupling gap. The die were cladded with 2 μm SiO_2 using plasma enhanced chemical vapor deposition (PECVD) with SiH_4 and N_2O precursors. The samples were furnace annealed at 1000°C for 10 hours in an N_2 ambient environment to remove excess hydrogen in the PECVD SiO_2 cladding. The edge facet process for the high temperature samples used multiple coats of AZ nLOF 2070 photoresist, UV direct write 375 nm lithography, and RF generated, magnetically-coupled RIE (MERIE) using an Applied Materials Precision 5000 tool according to the process developed in [9].

The process flow for the low temperature samples was similar to the high temperature samples except for the SiN_x deposition, the SiO_2 waveguide cladding, and the edge facet process. The SiN_x deposition was done using an Oxford Plasma Pro 100 PECVD tool with SiH_4 and N_2 precursors only (i.e. without NH3). The same tool was used to deposit the PECVD SiO_2 cladding, which was 3 μm thick and used a 350°C process with a tetraethyl orthosilicate (TEOS) precursor. No furnace annealing was performed on the samples, making the process entirely back-end-of-line (BEOL) compatible. The edge facet process used an amorphous silicon (aSi) hard mask in place of a thick photoresist mask. The process involved depositing 7

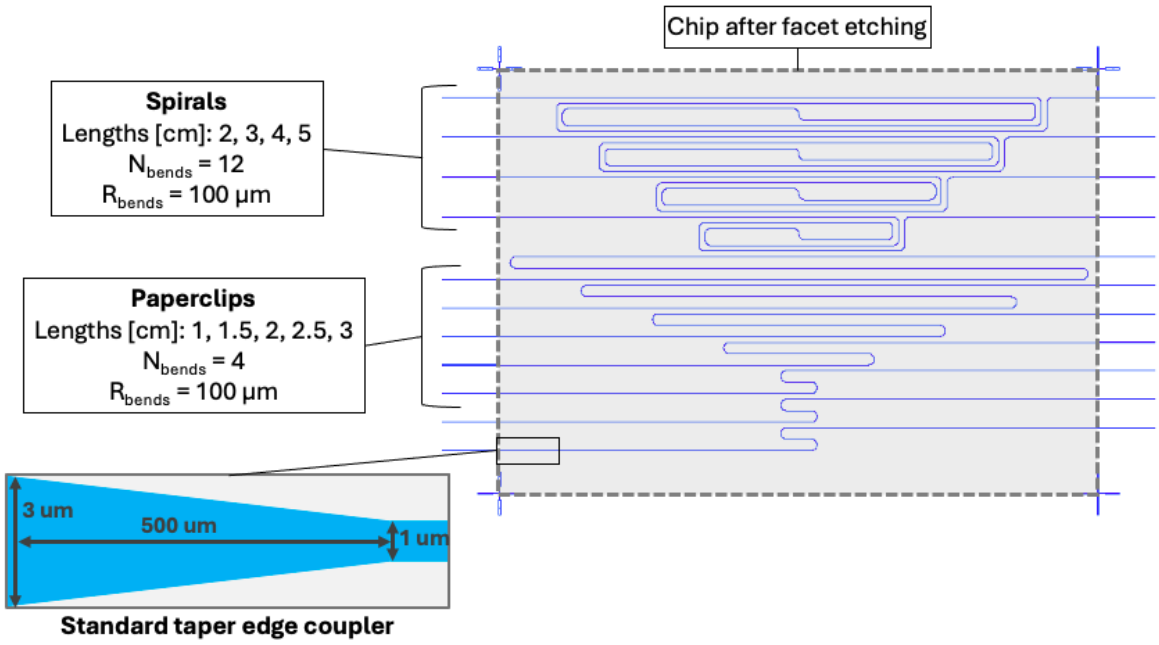


Figure 3: The glass PIC mask layout for extraction of propagation and edge coupling loss is shown, with the callout showing a top down view of the edge coupler design. While inverse taper edge couplers have a higher coupling efficiency, standard tapers were chosen due to their wider fabrication tolerance. Note that the high temperature sample also contained micro ring resonators as mentioned in [9] (supplemental information).

μm of amorphous silicon (aSi) as a hard mask using PECVD at 270°C. The hard mask was patterned using 375 nm direct write UV lithography with a 7.1 μm thick AZ nLOF 2070 photoresist mask. The hard mask was etched using MERIE with a Cl_2/Hbr gas chemistry. The deep SiO_2 edge facet was etched using the same tool, but with a CHF_3/Ar gas chemistry. The selectivity of the CHF_3 etch was 20.2 (SiO_2:aSi) and the edge facet was determined to be 88.7-90.8 μm deep with a slope of approximately 79°. Various SEM images showing the edge facet when looking directly at the waveguide and along the edge of the die can be found in Figure 2(b) and 2(c), respectively.

The testing setup consisted of a 1480-1640 nm laser injecting 0 dBm of light into a single mode fiber (SMF). The SMF connected to a tapered, lensed polarization maintaining (PM) fiber (8 μm core, 125 μm cladding, 3 μm working distance) which went through polarization controlling paddles before being connected to a piezoelectric stage for sub-micron fiber-to-chip alignment. Edge coupling was accomplished using SiN_x tapers which were 3 μm wide at the facet and 500 μm long, leading to 1 μm wide waveguides. The light traveled through the SiN_x waveguides, where it was collected using an edge coupled lensed SMF and fed into a photodetector. The die layout for the high and low temperature samples including the spirals, paperclips, and tapered edge couplers was summarized and can be found in Figure 3. The mask contained five paperclips of length 1-2.5 cm and four spirals of length 2-5 cm to determine propagation, bending, and edge coupling losses. First, the cut back method was used to determine the propagation loss and total facet loss (i.e. the loss at zero propagation length, or y-intercept, of the linear regression line) for the SiN_x by fitting the measured data for the paperclips and spirals independently. Next, the bending loss and edge coupling loss was determined by using the fact that the spirals and paperclips had a different number of bends. Specifically, this analysis was done according to the following equation:

$$P_{\text{zero, prop}} = 2P_{\text{edge coupler}} + N_{\text{bends}} P_{90^\circ \text{ bend}} + P_{\text{external}} \quad (1)$$

where $P_{\text{edge coupler}}$ is the loss through a single standard taper edge coupler in dB, N_{bends} is the number of 90° bends through the SiN_x paperclips or spirals used, and $P_{90^\circ \text{ bend}}$ is the loss per 90° bend in dB. By measuring the propagation loss using both the spirals and paperclips, each with a different value for N_{bends}, a set of two equations with two unknowns was created via Equation 1 and solved for $P_{\text{edge coupler}}$ and $P_{90^\circ \text{ bend}}$ including their respective uncertainties.

III. Results

An image taken of the finalized low temperature sample on the testing stage can be found in Figure 4(a). Note that the red light was used for fiber alignment purposes and provides the

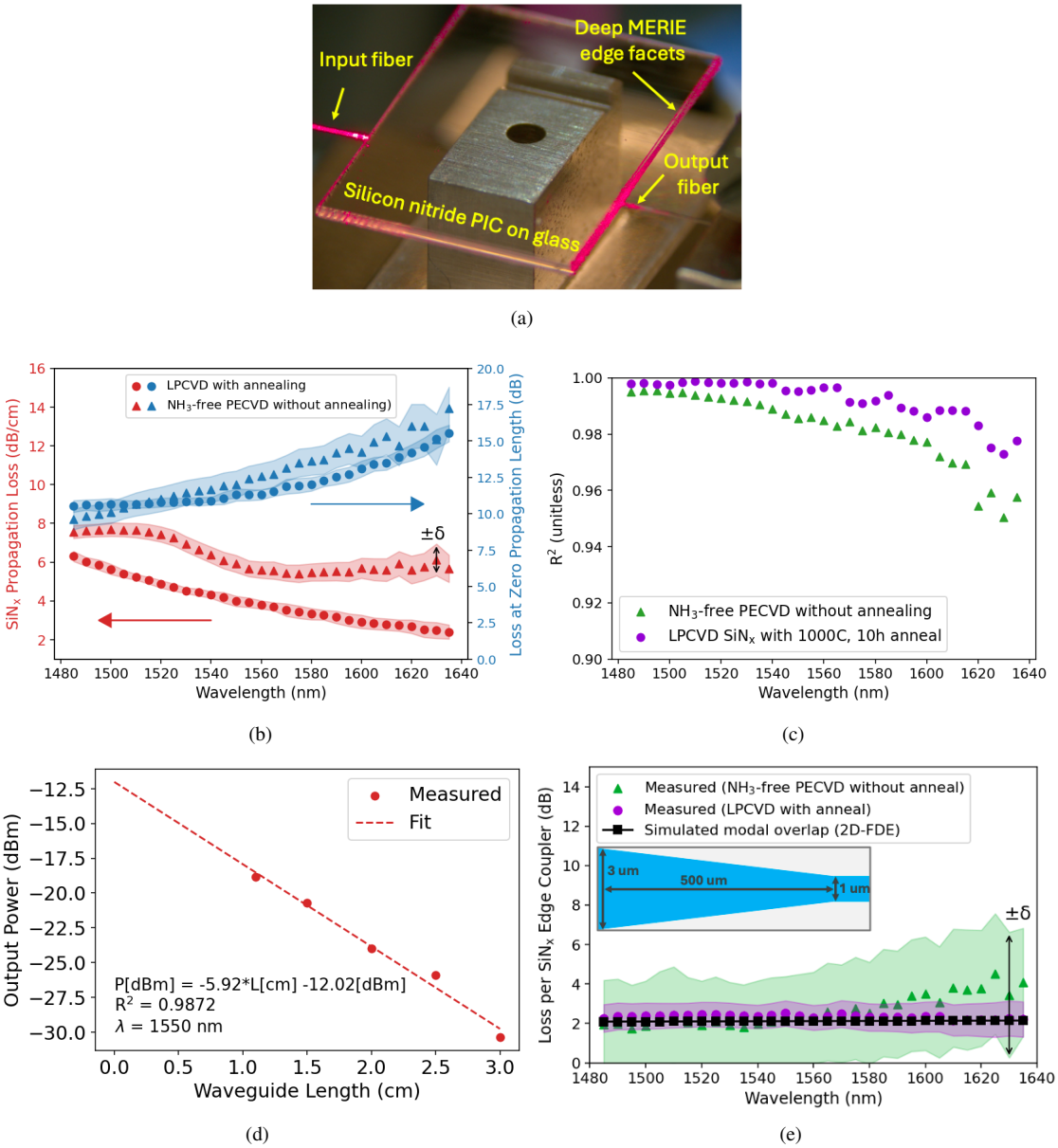


Figure 4: In (a) an image of a SiN_x-on-glass PIC on the testing stage. In (b) the propagation loss and total facet loss comparison for the high and low temperature processes. In (c) the R^2 values for the cutback method linear regression fitting process are shown. In (d) an example of the cutback method linear regression fit at 1550 nm wavelength for the paperclips of the low temperature sample. In (e) the coupling loss versus wavelength for a single SiN_x edge coupler on the high and low temperature sample is shown with 2D-FDE simulation results (which were executed assuming material parameters for LPCVD SiN_x waveguides).

ability to clearly see the input and output fibers in the final picture. Moreover, propagation loss data from 1480 to 1640 nm wavelength for the high and low temperature samples were determined by averaging within a ± 2.5 nm wavelength windows, and fitting each wavelength window using linear regression. Based on the data, a minimum propagation loss of 2.40 ± 0.36 dB/cm and 5.42 ± 0.45 dB/cm was observed for the high temperature and low temperature samples, respectively, as shown in Figure 4(b). When calculating the additional loss of the low temperature samples compared to the high temperatures samples, the average value was less than 3 dB/cm. Similarly, the total facet loss was calculated for both samples and is also shown in Figure 4(b). The linear regression R^2 values versus wavelength for the paperclips on the high and low temperature samples can be found in Figure 4(c). The data from Figure 4(c) represents an overall high quality fit to the measured paperclip

data, will all fitted wavelengths being > 0.95. An example of a single linear regression fit of the raw output power as a function of waveguide length for the paperclips of the low temperature sample at 1550 nm wavelength can be found in Figure 4(d). Furthermore, the loss per edge coupler, after propagation loss, bending loss, and external system losses have been removed using 1, for both samples from 1480-1640 nm was calculated and demonstrated a minimum coupling loss of 2.17 ± 0.79 dB, which align well with 2D Finite-Difference Eigenmode (FDE) simulation values. Note that the 2D-FDE simulations were executed using the material parameters for the LPCVD SiN_x waveguides.

IV. Discussion

There are several important trends to note, beginning with the wavelength dependencies for Figures 4(b). In Figure 4(b) the LPCVD SiN_x propagation loss has a wavelength dependence of approximately 0.0265 ± 0.0004 dB/cm per 1 nm wavelength as determined by a linear regression fit, with the PECVD SiN_x propagation loss showing a similar dependence. This can be explained by considering that near 1400 nm there is a strong absorption peak due to SiO-H bond vibrations [23], which decays as wavelength increases towards 1640 nm. Despite the PECVD SiO_2 cladding being annealed at 1000°C for the high temperature samples, this dependence indicates strong hydrogen induced absorption remained in both the LPCVD and PECVD SiN_x waveguide cladding.

While the hydrogen induced absorption dominated at lower wavelengths, at longer wavelengths the scattering resulting from waveguide roughness resulted in the trend displayed in Figure 4(c). Specifically, shorter wavelengths resulted in tighter optical confinement and less of an interaction with the waveguide sidewall. This notion, paired with the fact that as wavelength was swept the polarization was likely rotating between TE and TM in the PM fiber, meant that as the wavelength was changed the waveguide did not result in noticeably different scattering. However, for longer wavelengths and higher sidewall interaction this changing polarization resulted in a larger oscillation in output power (i.e. noise), which evidenced itself as a lower R^2 for both the high and low temperature samples as shown in Figure 4(c).

Similarly, the total facet loss increased with longer wavelengths for both the high and low temperature samples as shown in Figure 4(b). This can be explained by the same reasoning as above regarding the scattering induced losses increasing with increasing wavelength. In particular, in [9] (supplemental information) it was shown that for longer wavelengths the SiN_x bending loss increased as the optical mode becomes less confined and scattered more due to the rough sidewall. Meanwhile, the loss per edge coupler was relatively constant versus wavelength, having a mean of 2.34 dB (2.66 dB) and standard deviation of ± 0.09 dB (± 0.76 dB) for the high (low) temperature sample as shown in Figure 4(e). This is due to the fact that the beam waist output from the lensed SMF has a wavelength-limited minimum diameter of 2.3-2.7 ± 0.3 μm from 1480-1640 nm, placing an upper limit on modal overlap and, in turn, coupling efficiency. The fact that the measured data for the high and low temperature samples differs from the simulated data by less than 0.22 dB and 0.54 dB, respectively, from 1480-1640 nm supports this notion. Note that the higher uncertainty in the low temperature sample's coupler loss was a result of the significant noise in the longest spiral measured on that sample (4.49 cm in length). This increased noise did not have any wavelength dependence, and was concluded to be stemming from a waveguide or facet defect such as a particulate as shown to the immediate right of the waveguide in Figure 2(b).

V. Conclusion

For the first time, silicon nitride photonic integrated circuits on glass substrates were fabricated, with dry etching using to form high quality edge facets for optical coupling. The measured results demonstrated a minimum propagation loss of 2.4 ± 0.36 dB/cm and minimum edge coupling loss of 2.17 ±0.79 dB. This data illustrates the potential for package level passive photonic integration on fused silica interposers, a high performance substrate material. Future process optimization of SiN_x waveguide and SiO_2 cladding deposition to decrease the residual hydrogen content in the films provides an avenue to further improve upon the propagation losses measured here. Likewise, the edge coupler performance can be improved by transitioning to inverse taper designs which, for SiN_x based waveguides, can be found in current foundry process design kits. Through these improvements, and alongside other photonic packaging advancements such as pick-and-place assembly, the deployment of glass based photonic interposers in co-packaged systems can provide a cost- and energy-efficient method to scaling to Pbps data capacities in data- and telecommunications networks.

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