150 GHz-band Coreless High Multilayer Antenna-in-Package for 6G

Hiroshi Taneda[1], Naoki Kuroiwa[1], Yoshikazu Kazama[1], Kei Murayama[1], Makoto Tsukahara[1], Hiroko Ota[1], Yoko Nakabayashi[1], Noritaka Katagiri[1], Ryosuke Hasaba[2], Ken Takahashi[3], Kenichi Okada[4], Takashi Tomura[4], Watanabe issei[5]
[1]Shinko Electric Industries Co., Ltd.
36 Kita-Owaribe, Nagano 381-0014, Japan
Ph: +81 26-263-4593; Fax: +81 26-263-4562
Email: hi.taneda@shinko.co.jp
[2]Panasonic Industry Co., Ltd.
[3]Panasonic System Networks R&D Lab. Co., Ltd.
[4]Institute of Science Tokyo
[5]National Institute of Information and Communications Technology

Abstract

In recent years, data have been exchanged by communication terminals everywhere in our daily lives, and the development of low-latency communication technologies for use in medical devices, factory automation, and autonomous driving has been gaining momentum. In order to meet the increasing demand for communications in the future, MIMO (Multiple Input Multiple Output) using the sub-THz band, which has a wider bandwidth available, is expected to realize even higher speed and capacity communications. At frequencies of 151.5 to 164 GHz, the wavelength is approximately 1.9 mm, so a multi-element compact antenna module with antennas of 1 mm or less in line can be realized.

Challenges to the widespread use of MIMO antenna modules for high-frequency applications are transmission loss due to the increased number of wiring paths associated with the increased number of antenna elements, and miniaturization for installation in edge devices. In this development, we attempted to solve the problem of transmission loss by selecting low dielectric constant and low dielectric loss tangent materials and using the latest printed circuit board technology to create an antenna with a waveguide that is easy to mass-produce. We also Developed a coreless substrate process to produce small AiP (Antenna-In-Package) substrates that can be miniaturized and reduction in height. Environmental load tests (-55 ⇔ 125 deg.C) were conducted on the prototype AiP substrate, and the 7 stacked via passed 1000 cycles, confirming its practical reliability. The substrate size of this AiP is 8mm x 20mm x <1mmt, which is small enough to be mounted on wearable devices with narrow mounting areas, and it is expected to be widely used in society.

Key words

6G, AiP, coreless substrate, phased array antenna, sub-THz.

I. Introduction

In recent years, data is exchanged by communication terminals everywhere in our daily lives, and the development of low-latency communication technologies for use in medical devices, factory automation, and advanced automated driving has been gaining momentum. Around 2030, the 100~300 GHz frequency band, called the sub-THz band [1], [2], is being considered for use as 6th generation (6G) communications [3].

In order to promote the spread of devices that can support the sub-THz band, it is necessary to develop technologies for wireless modules that have low transmission loss in the high-frequency range, and that are compact and low-cost.

We approached transmission loss suppression and substrate miniaturization from the viewpoint of substrate material and structure. This paper reports on the materials, structure and process design that enable the fabrication of small AiP substrates for high-frequency signals, and the reliability of the fabricated substrates.

Ⅱ. Substrate structure and material

A. AiP substrate structure

The substrate structure for high-frequency applications requires a short wiring distance between the RFIC and antenna to suppress signal transmission loss [4]. To shorten the wiring path, we proposed a structure in which a three-dimensional antenna structure is formed using vias in a coreless build-up substrate. Glass and fluororesin offer

excellent transmission characteristics, but they are difficult to process. In order to form a three-dimensional structure, low-Dk and Df resin with excellent processability was selected as the insulating material for this project.

Figure 1 shows a schematic diagram of the conventional antenna substrate structure and the proposed structure. By shortening the wiring path between the RFIC and antenna from the conventional structure, transmission loss can be suppressed. The layer configuration is coreless 10 layers as shown in Table 1, the design rules are those feasible for antenna design and manufacturing in the frequency band 151.5-164 GHz, and the design is based on 70 µmt resin thickness, via φ60 µm, minimum L/S=30/30 µm, and maximum 4 stacked via. The substrate includes SIW (Substrate Integrated Waveguide) formed by vias with a minimum pitch of 125 µm, a structure that suppresses signal loss [5] [6]. This substrate includes the antenna and waveguide in the center of the substrate, which enables radiation from the sides of the substrate. The antenna consists of 8 elements arrayed at a pitch of approximately 1mm, which is 1/2 wavelength of 150GHz, to form a phased array antenna, as shown in Figure 2.

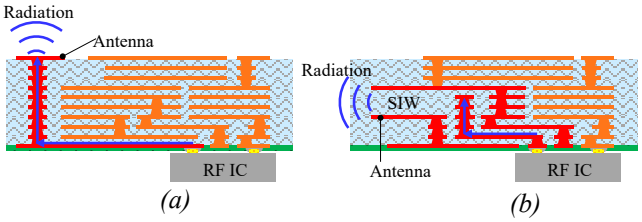

Figure 1: Schematic of AiP substrate. (a) Conventional (b) Proposed

Table 1: Design of AiP substrate

Item	Specification
Metal layer	10 layers
Dielectric layer	9 layers
Trace thickness	18µm
Dielectric thickness	65µm
Line/Space	Min. 30/30µm
Via diameter	φ70µm
Pad diameter	Min. φ110µm
Pad pitch	Min. 125µm
Substrate thickness	765µm

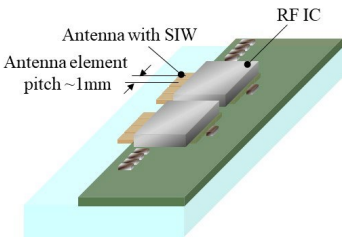

Figure 2: AiP substrate structure consisting of 8 element antenna with approximately~1mm(λ_0/2) pitch.

B. Material

In a transmitting/receiving system using high-frequency signals, as the frequency increases, signal transmission loss also increases due to conductor loss and dielectric loss in the antenna substrate, which negatively impacts system performance [7].

Microstrip lines shown in Figure 3 were fabricated on the resin material that constitutes the AiP substrate to confirm the transmission loss with respect to frequency. The evaluation materials were Df 0.01 or less and Dk 3.5 or less, and resin materials A~C were candidates. Material A is prepreg material of Panasonic's package material (R-G640(L)). Material B is RCC material of Panasonic's package material (R-G740M). Material C is prepreg. Material A has Dk 3.1 and Df 0.002 (10 GHz), material B has Dk 2.6 and Df 0.003(10 GHz), and material C has Dk 2.9 and Df 0.002 (10 GHz) properties.

Figure 4 shows results for transmission loss in differential microstrip line. Evaluated at frequencies up to 110 GHz, measurement temperatures R.T. (Room Temperature) ~150 deg.C, and wiring lengths of 10~40 mm. Transmission loss versus frequency is best for material B and second best for material A in the R.T. environment. In the high temperature range, material A is good and has excellent temperature stability. Since the AiP substrate to be developed this time aims to shorten the transmission path by making it coreless, glass cloth-filled resin A was selected as the build-up material because of its rigidity and temperature stability of transmission characteristics even in a coreless board.

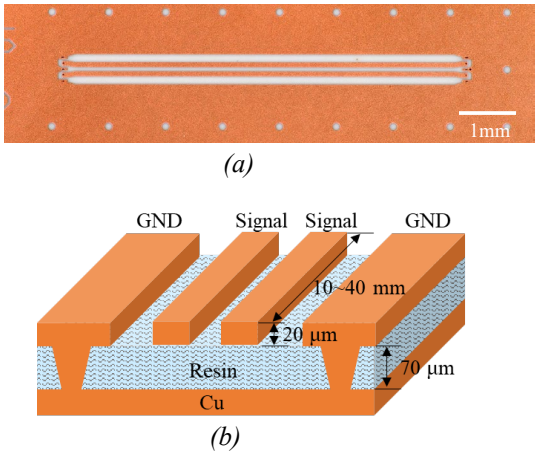

Figure 3: Substrate for signal characterization. (a) Substrate appearance (b) Cross-section model

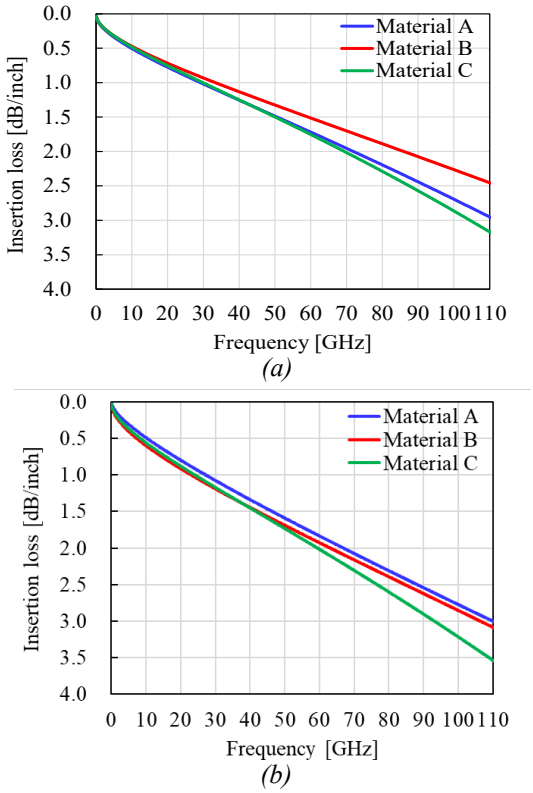

Figure 4: Result of signal characteristics. (a) Room temperature (b) 150 deg.C

III. Process of core less AiP substrate

Figures 5 and 6 show the AiP module appearance and cross section of the fabricated coreless AiP substrate with SIW structure. The package substrate size is 8 mm × 20 mm × >1 mmt, which is small enough to be mounted on a wearable device. The cross-sectional view of the substrate shows that SIWs are incorporated in the center L4-L7 layers of the substrate, and the X-ray CT image shows that the SIW sides are formed by via walls.

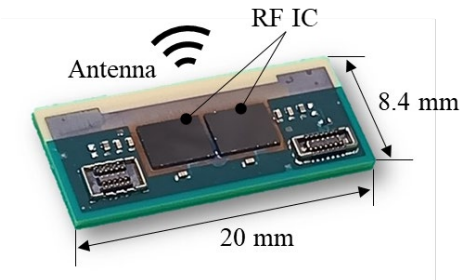

Figure 5: Sub THz antenna module.

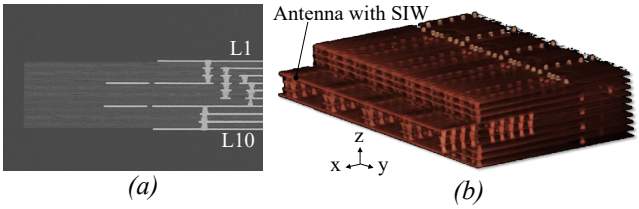

Figure 6: Antenna and SIW substrate structure. (a) Cross section (b) X-ray CT image

The process flow of a coreless AiP substrate with SIW structure is shown in Figure 7. Although the resin is a rigid material with glass cloth, process flow with a resin thickness of 70 µmt carries the risk of substrate damage and substrate deformation. Therefore, a support carrier process was adopted to improve handling during process flow. The surface of this support carrier is laminated with peelable copper foil to create a separable structure. First, a Cu pattern, resin, and Cu pattern are formed on the support carrier in sequence. The addition of the Cu pattern on both sides of the resin increases the rigidity of the substrate compared to the resin alone, and the substrate can be safely handled after separation from the support carrier. After separating, the substrate is built up on both sides to the target number of layers.

The Cu trace and via processes are formed by MSAP (Modified Semi Additive Process) instead of subtractive method to achieve a design with a minimum diameter of 70 µm via, minimum via pitch 125µm via and a minimum L/S=30/30 µm without roughening the low Dk, Df resin surface. Via processed by CO_2 laser can be filled with electrolytic copper plating to reduce surface recesses, allowing multi-stacked vias. Multi-stacked vias are expected to shorten wiring paths and provide design flexibility.

The via waveguide walls in SIWs must have a via pitch sufficiently narrower than the frequency to prevent radio wave leakage. Compared to machine-drilled vias, laser via processing can be formed narrower pitches, allowing more freedom in waveguide path design, and has the potential to support even higher frequency bands. In the mounting process of each component and RFIC, SMT (Surface Mount Technology) using SAC solder was used for mounting the components, and low temperature flip chip mounting using SnBi solder was used for mounting the RFIC [8].

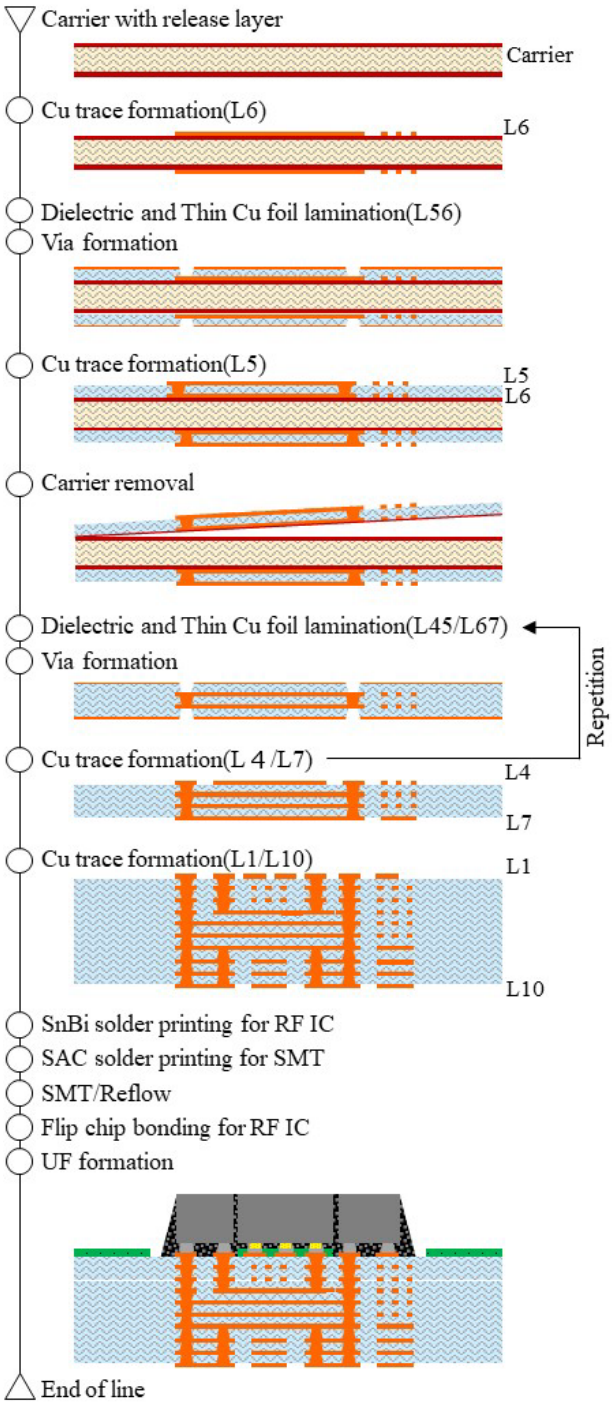

Figure 7: Process flow of coreless AiP substrate with carrier.

IV. Experimental Results

A. Stacked via reliability

TS(Thermal Shock) reliability test condition is -55⇔125 deg.C 1000 cycles after pre-condition MSL Lv.3A (HTS 125 deg.C x 24 hr.) + THS (60 deg.C/60% RH x 40 hr.) + Reflow (260 +0/-0 deg.C x 3 times). The acceptance criteria for the TS test was set at 1000 cycles. The test sample was N=8, and via diameter is 70um with 125um pitch. The breakage criterion for the via daisy was defined as ±10 % change in electric resistance and above. Figure 7 shows the reliability test results, which confirm that 7 stacked vias passed the 1000 cycles test. In this AiP module substrate, the maximum number of stacked vias is 4, which is considered to meet the reliability criteria.

Figure 8 shows the via cross section after the reliability test. 9-stacked vias had more pronounced cracks at the bottom of the vias and were more prone to breakage than 7-stacked vias. From this, it can be said that 9-stacked vias have a higher failure rate in the TS test.

Figure 9 shows the stress simulation results for full-stack and staggered vias. The simulation conditions were analyzed at 25 deg.C with 260 deg.C as the stress-free temperature. High multilayer stacked vias have stress concentrated at the bottom of the vias. On the other hand, staggered vias have lower stress values. From the results, it is preferable to design with staggered vias rather than stacked vias.

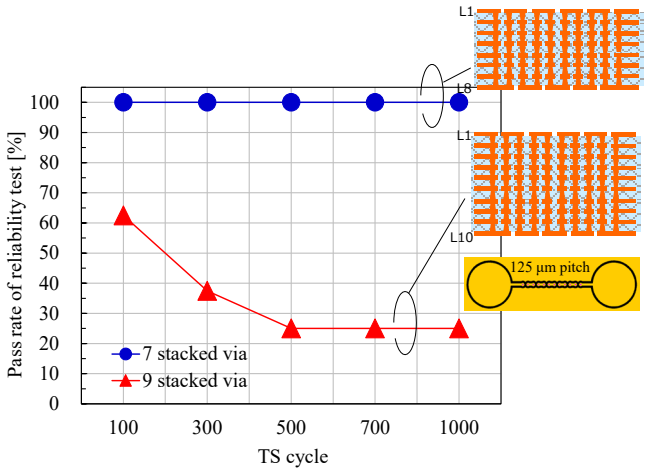

Figure 8: TS test results of Stacked vias.

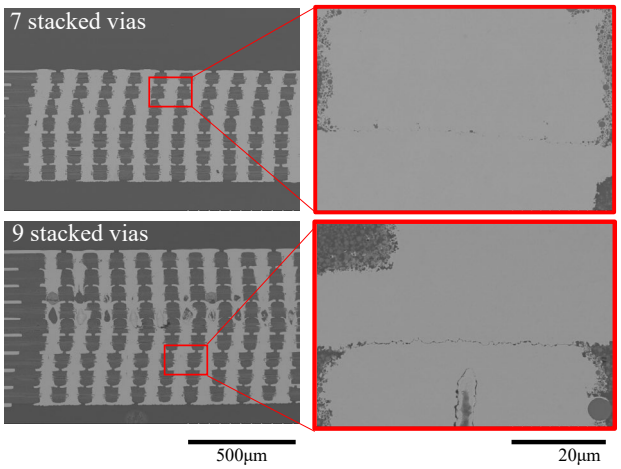

Figure 9: Cross section of vias after TS test.

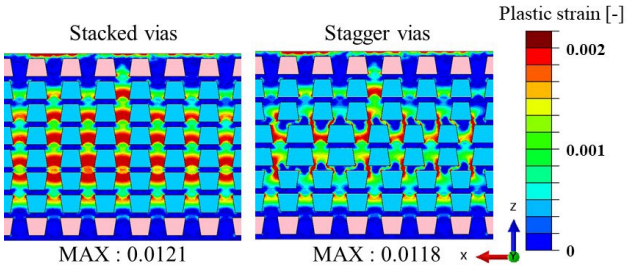

Figure 10: Stress simulation at reflow.

B. Antenna characteristics

Table 2 shows simulated and measured peak gains of an 8-element array antenna in the AiP at 150GHz band. The measured antenna gains of 14.5~15.2 dBi agree with that of the simulation results. This agreement means a fact that the fabricated substrate is very close to the physical properties used in the design and has made with high process accuracy, so the expected antenna performance has been obtained [9][10].

Table 2: Antenna gain in frontal direction

Frequency [GHz]	Simulation	Sample		
		No.1	No.2	No.3
151.50	15.2	14.9	14.9	15.2
157.75	15.5	14.7	14.7	14.7
164.00	15.7	14.7	14.5	14.9

V. CONCLUSION

We have approached the reduction of transmission loss and miniaturization of AiP substrates for terahertz waves in the 100 to 300 GHz band from the viewpoint of substrate material and substrate structure. Microstrip lines were fabricated and evaluated, and low-dielectric material with low transmission loss was selected. The use of a support carrier and MSAP microfabrication technique enabled flexible designs and the formation of coreless AiP substrates with SIW within low Dk and Df materials. The module size (8mm × 20mm × >1mmt) is small enough to be mounted on a wearable device. The developed substrate demonstrated reliable performance with up to 7 stacked via. Antenna characteristics showed a peak gain of 14.5~15.2 dBi, and both antenna gain and antenna pattern were consistent with those expected in the design, indicating that the AiP substrate was manufactured as designed.

Acknowledgment

This work was supported in part by the Ministry of Internal Affairs and Communications, Japan, under GrantJPJ000254.

References

[1] ECC Recommendation (18)01, CEPT ECC, April 2018.

[2] Michael J. Marcus “6G Spectrum Policy Issues above 100 GHz”, IEEE Wireless Communications, Dec. 2021.

[3] White paper 5G Evolution and 6G,” NTT Docomo, Inc., Jan. 2020. [Online].Available: https://www.nttdocomo.co.jp/english/binary/pdf/corporate/technology/whitepaper_6g/DOCOMO_6G_White_PaperEN_20200124.pdf

[4] H.Utsunomiya, “Jisso Technologies and Packaging for 5G Mobile Communication Era,” J. Electron. Pack. Soc., Vol. 24, No. 1, pp. 15-14, 2021 (in Japanese).

[5] D. Deslandes and K. Wu, “Integrated microstrip and rectangular waveguide in planar form,” IEEE Microw. Wireless Compon. Lett., vol.11, pp.68-70, Feb. 2001.

[6] Y. Morishita, K. Takahashi, R. Hasaba, T. Murata, K. Takinami, H. Kitamura, U. Sangawa, T. Tomura, I. Watanabe, "Comparison between Microstrip-line and Substrate Integrated Waveguide on Package Substrate in 170 GHz and 300 GHz Bands", 2022 Asia-Pacific Microwave Conference (APMC), pp. 196-198, Dec. 2022.

[7] R.Hasaba, et al., “150 GHz Embedded Patch Antenna With Radiation From the Substrate Edge for Antenna-in-Package,” IEEE Int’ l Symp. on Antennas & Propag., Oct. 2023.

[8] K.Murayama, et al., 2024 IEEE 26th Electronics Packaging Technology Conference (EPTC)

[9] Y.Morishita, et al., “150GHz-Band Compact Phased-Array AiP Module for XR Applications toward 6G”, IEEE MTT-S International Microwave Symposium (IMS), July. 2025

[10] Y. Yamazaki, et al., "A 150 GHz High-Power-Density Phased-Array Transceiver in 65nm CMOS for 6G UE Module," IEEE Symposium on VLSI Technology and Circuits, June 2025