High-Performance PCB Materials for Next-Generation Electronics Packages, driving Signal Integrity, Power Handling, and Reliability.

John Coonrod, Lance Blaskowski, Vitali Judin, Karl Sprentall, Mike Kuszaj
Rogers Corporation
100 N Dobson Rd,
Chandler, Arizona 85224 USA
Email: John.Coonrod@rogerscorporation.com

Abstract

This paper provides an overview in the advancement of high-frequency, high-speed and high thermal-conductivity PCB materials critical for next-generation electronics packages, with a focus on enhancing signal integrity, power handling, and reliability. Specifically, we address the interface challenges between PCB materials and electronic packages. Further, the paper provides insights into specific aerospace and defense needs and demonstrates the practical benefits of materials in relation to environmental requirements and fabrication processes. The study aims to provide a PCB material "toolbox" to the assembly and packaging community, highlighting the importance of these materials in meeting the demands of evolving high performance electronic applications.

Key words

High-frequency, Thermal-conductivity, Signal integrity, Reliability, Aerospace and Defense.

I. Introduction

Designing IC packages for operation at high frequencies, using high-speed channels and/or high thermal loads requires careful selection of PCB materials. Specifically, considering the current trend towards higher speed transmission channels in the modern digital electronics, pushing Nyquist frequencies beyond the 50GHz range, the requirements for PCB materials tends to get closer to mmWave RF applications. At these frequencies, PCB material properties critically impact signal integrity (SI). Furthermore, the need to navigate complex fan-out topologies in packages with numerous I/Os drives high-layer-count constructions employing plated through-holes (PTHs), stacked or staggered microvias, and selective back-drilling. This often coincides with requirements to operate in a wide range of temperatures, which push the boundaries of required thermo-mechanical reliability. Additionally, package size evolution pulls in two opposite directions. Miniaturization drives thermal densities up, creating hotspots with significant thermo-mechanical stress and demanding materials with high thermal conductivity to spread and remove heat efficiently. Conversely, highly integrated SoC devices increase BGA body size, placing greater thermal expansion mismatch stress on solder joints and dielectric materials in both PCB and Package. Selecting laminates with matched in-plane CTE in combination with appropriate material elastic modulus, elongation of copper, and adequate copper-foil adhesion is therefore essential for solder joint and long-term surface mount reliability. Advanced thermoset and PTFE-based laminate families, reinforced or non-reinforced with engineered ceramic fillers, have emerged to meet these combined electrical and thermal demands. The following sections provide an overview of their performance and reliability, with special emphasis on the PCB-to-package interface.

II. Advancements in PCB Materials

A. High-frequency and high-speed performance

The transition to higher Nyquist frequencies impacts not only board-level material choices but also the design and integration of IC packages. PCB-to-package interface and its co-design are becoming increasingly critical. For package designers and manufacturers, this means working with PCB material specifications that ensure consistent SI at interfaces as well as along PCB traces. At the PCB-to-package interface, BGA pad size and pitch constrain available space for routing, limiting trace widths of the transmission channel. At a given impedance, the trace width primarily depends on PCB layer thickness and dielectric constant (Dk), which support impedance continuity. Traditional materials with Dk

in the range of 4.0-4.4 are adequate only for low-frequency applications, exhibiting poor SI, low stability, and insufficient power handling capability at higher frequencies. For demanding SI applications, a variety of newer materials are available with Dk typically ranging from 2.2 up to 3.5, alongside specialized variants at 6.15 and 10.2. Lower Dk is advantageous for multiple reasons e.g., it directly reduces dielectric loss according to the relationship:

$$Dielectric\ Loss \sim f \cdot \sqrt{D_k} \cdot D_f \quad (1)$$

Furthermore, reducing Dk at a given impedance and PCB layer thickness allows wider trace widths, significantly reducing the skin effect driven conductive losses, which often make the predominant contribution to the total insertion loss (IL), especially for very thin dielectric layers. However, as mentioned above, wider traces may not always be feasible due to limited fanout space and pad size constraints at the package interface, making Dk selection a critical trade-off decision. Additionally, designers must consider the thermal coefficient of the dielectric constant (TcDk). A high TcDk could result in different dielectric behaviors across thermal operating points, creating lateral gradients in Dk and position-dependent signal timing differences that introduce fractions of skew into the channel, degrading overall timing budgets in modern SerDes links. State-of-the-art PTFE-ceramic composites achieve |TcDk| around 3-12 ppm/°C and engineered low-loss thermoset composites |TcDk| around 30-50 ppm/°C keeping phase variation at minimum over a wide temperature range [1]. In contrast, legacy thermosets can exceed 100 ppm/°C, which is an order of magnitude worse [2].

Add to this, it should be considered that Dk is a tensor that is represented by a 3x3 matrix. Technically, it goes a bit deeper, the tensor varies as a function of location in the material. The off-diagonal components of this tensor can be neglected in linear dielectric materials. Three main diagonal components D_{kx}, D_{ky} and D_{kz} should be ideally all equal. However, materials often demonstrate anisotropy that typically corresponds to inhomogeneity in composition such as glass-weave, self-oriented fillers or filler distribution. An effect of anisotropy is an orientation dependent behavior in circuitry. As an example, there might be shift in RF filter characteristics oriented in x- direction vs. y-direction. In digital boards, anisotropy introduces skew – a small mismatch in signal arrival time. Three types of skew effects can be distinguished: intra-pair skew (arrival time difference in differential transmission lines) [3], inter-lane skew (arrival time difference in parallel communication e.g. 1.6T Ethernet = 8 x 224Gbps) [4], as well as inter-eye skew (in higher level modulations, horizontal offset between different eyes) [5]. Intra-pair skew is the type that PCB materials influence most,

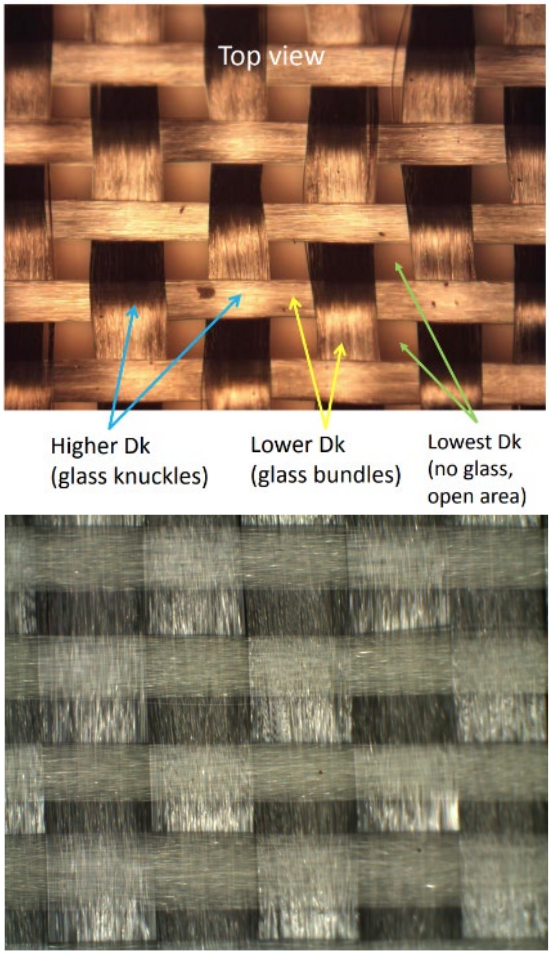

Fig. 1, Exemplary standard weave glass 1080 (top), spread-weave glass 1078Dk distribution (bottom). Later one has a very homogenous lateral yarn distribution.

because fiber-weave dielectric-constant variations and copper-etch differences cause the conductors to experience slightly different propagation velocities. The other two skew types are driven largely by routing topology or transmitter linearity. In practice, intra-pair skew is addressed using spread-glass reinforcement [6] (see Fig. 1), which has been proven effective in controlling weave-based Dk variation. Add to this, there are other mitigation methods e.g. "zigzag" routing or rotating of PCB artwork to average Dk seen by each conductor [7]. For example, skew budgets at 224Gbps PAM4 are in sub-1 ps range, which many designers adopt PTFE spread-glass cores coupled with thin spread-glass thermosets in this situation. To address the digital communication skew budget requirements using engineered full thermoset stack-ups, higher-end low-Dk-glass types for PCB material reinforcement are unavoidable. This solution, however, requires more costly and rare raw materials, and needs thorough supply chain risk-management.

In addition, the Dk value also depends on frequency, which, in unfavorable cases, introduces group-delay dispersion. Beyond that, we can find Dk also influencing latency, crosstalk and EMI susceptibility, as well as parasitic capacitance. Precise test and measurement of dielectric characteristics in PCB materials helps to improve simulation accuracy in package-to-PCB impedance continuity and positively impacts SI debug time.

In high frequency and high-speed digital communication, IL of the transmission channel in circuit board co-defines specifications of IC package. E.g., a loss budget in device-to-device or die-to-die link drastically limits the available physical channel length. At transmission rates above 112Gbps, the routing length can get quickly down to impractical values [8]. In RF antenna applications, transmission line loss will directly impact realized gain. In general, channel loss directly contributes to thermal load in high power use cases and to device power consumption in low power applications. Conclusively, a thorough material choice with application specific, sufficiently low IL is critical to success. During the material down-selection phase, the only direct side-by-side testing using identical representative test vehicles will lead to secure determination of material fitness. Conversely, comparison of data sheet values alone will often lead to famous "apples vs. oranges" analysis. A commonly misused example is the reliance on split-post dielectric resonator (SPDR) measurements solely for datasheet values. However, due to the nature of the electric field distribution in this method, the extracted values represent only the in-plane Dk and Df. These can differ significantly from the nominal z-axis values based on IPC TM650 2.5.5.5, particularly Df in glass-reinforced materials.

As shown above, from an electrical standpoint, IL is one of the most critical factors in PCB material shortlisting. According to (1), the dissipation factor Df, also referred to as tan(δ), is the biggest contributor to dielectric component of IL. Low Df (<0.002) materials, such as PTFE-based and/or highly engineered thermoset materials, are therefore preferred solutions. In a study characterizing multiple PCB dielectrics at 60–81 GHz, PTFE-composites showed consistently lower loss compared to high-performance thermoset substrates [9]. This is due to lower intrinsic dielectric loss characteristics of PTFE polymer.

It should not go unmentioned that copper-foil roughness in PCB also substantially influences conductor loss contribution to total IL, especially above 20-30 GHz or 56Gbps transmission rates. Furthermore, above 50 GHz conductor losses can absolutely dominate IL, since skin depths approach the copper roughness profile. In addition to IL effects, it has been demonstrated that the copper profile at the interface between the copper foil and dielectric, can significantly alter a circuit's effective Dk [10]. In sum, a rough copper profile causes the wave to see a higher effective Dk and greater conductor loss that must be considered in package-to-PCB system design. For this reason, designers should specify low-roughness copper options to minimize attenuation and signal dispersion at high frequencies and high data rates. It should be noted that modern ultra-low-profile electrodeposited foils get closer to rolled annealed copper surface roughness, helping to preserve SI, while reducing cost and improving adhesion.

B. Thermal Conductivity Improvements

Higher power densities elevate local board temperature. Reducing ΔT between junction and ambient requires material with low thermal resistance along the heat dissipation path, which often perpendicularly crosses the PCB stack. Higher average thermal conductivity of the stack not only extends device life but also avoids introducing mechanical stress. Ceramic-filled PTFE laminates with intrinsically low dissipation factors achieve through-plane thermal conductivity near 1.4 W/m/K and can significantly reduce copper trace temperature rise in comparison to standard materials with typical thermal conductivity values of <0.4 W/m/K. It is important to note that these values are extracted using the ASTM D5470 test method, commonly referred to as the "TIM tester." Other measurement methods can yield significantly different results, some with deviations of up to an order of magnitude. There are numerous materials available in the market that exhibit excellent thermal conductivity characteristics but fail in demanding applications due to higher dissipation factor. The circuits on these materials generate more heat than the material can dissipate. Specialized high-thermal-conductivity materials show excellent power handling capabilities [11]. Latest engineered thermoset formulations can also exceed 0.6 W/m/K while maintaining reasonable dissipation factor and offering a cost-effective solution for many package-to-PCB systems. An important consideration in high-thermal-conductivity material down-selection is the ease of material processing since most thermally conductive fillers inside the PCB dielectric are mechanically very abrasive. The right balance between thermal advantages and ability to preserve drill-bit life is what determines the best material solutions.

C. Thermo-mechanical matching

IC package CTE_{xy} values range from 5 ppm/°C (ceramic BGAs) to 18 ppm/°C (organic substrates). Matching averaged board CTE helps to mitigate solder and material stress and fatigue at the PCB-package interface. Engineered high-end PTFE composites can provide extremely stable x-y behavior down to 8 ppm/°C in combination with very-low Young's modulus (represents elasticity of the material).

Whereas thermoset PCB materials can be tuned down to 10-16 ppm/°C by adjusting the filler-to-resin content with glass reinforcement, but they inherently exhibit higher stiffness than PTFE solutions. This elevated stiffness, when combined with CTE mismatch and copper density asymmetry, can increase the risk of warpage during lead-free reflow or thermal cycling, potentially compromising BGA coplanarity and solder joint reliability. For extremely critical interfaces, e.g. die- or component-embedding, highly filled specialty thermoset materials with matched CTE_{xy} in single-digit range are applied.

D. Additional relevant parameters

The sections above focused on key material characteristics that can significantly impact the performance and reliability of an IC package. Beyond that, water absorption, surface & volume resistivity can also play a significant role in the signal or power integrity debugging process. There are thermoset materials that exhibit reversible, but significant degradation of IL performance and shift in Dk due to moisture exposure and thus require operation in a controlled environment [12].

III. Manufacturing and Reliability Testing

Intrinsic material properties determine not only performance, but also manufacturability, processability, and reliability of the PCB and final assembly with components, including the IC package. For surface mount assemblies, these properties directly influence solder joint quality, stress distribution during thermal cycling, and long-term mechanical stability, particularly in demanding environments.

A. Solder-Joint Reliability

To evaluate the performance of BGA packages mounted on PTFE- and thermoset-based hybrid board constructions, a dedicated study was conducted, using controlled thermal cycling and failure analysis protocols. BGA patterns were processed onto the outer layers of multilayer board constructions using each tested core type. The stack-up consisted of one 0.005” thick core of each material type bonded to both sides of a 1.52 mm thick thermoset spacer with bonding accomplished using a compatible thermoset bondply. The inner layers, including those in the 0.005” cores and the central spacer, had full copper planes that were completely etched to remove any influence on thermal mass or interlayer continuity. SMT coupon patterns with fine-pitch features were then fabricated on both sides of the board, followed by copper plating of approx. 0.75 to 1.0 mils. Two of the assembled boards received hot air solder leveling (HASL) surface finish, and one received electroless nickel immersion gold (ENIG). Lead-free solder paste was applied to attach BGA devices via a seven-zone convection reflow process reaching a peak temperature of 265 °C. The mounted components included TBGA352 (352 solder joints, 38 mm × 38 mm), BGA272 (272 joints, 25 mm × 25 mm), and FlexBGA144 (144 joints, 13 mm × 13 mm), covering a range of package sizes and thermal expansion profiles. Assembled boards were subjected to thermal shock cycling between -40 °C and 125 °C, with cycle counts extending up to 3150 for certain configurations. Coupons were incrementally removed after each 350-cycle interval for HASL finishes, and at five key intervals for ENIG-finished samples.

After thermal conditioning, two methods were employed for reliability assessment. In the dye-and-pry method, machinist’s dye was applied beneath the SMT components and dried prior to mechanical removal of the devices. Inspection followed to assess dye penetration, which would indicate cracking or voiding at the solder joints as shown in Fig. 2. In the second method, components were detached using solder rework, and conductor continuity was verified by inspecting for open circuits or physical damage such as pad lifting or copper trace fractures.

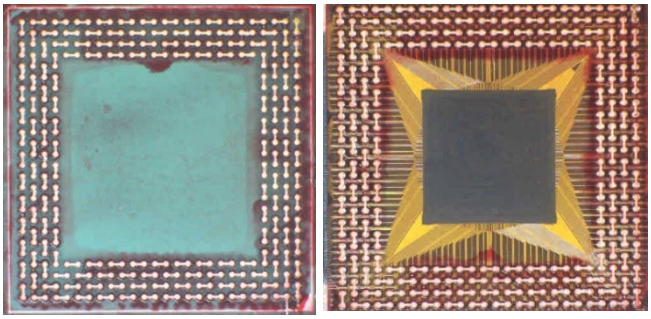

Fig. 2, Exemplary TBGA352, 38 x 38 mm², dye-and-pry test demonstrates reliable solder joints after exposure.

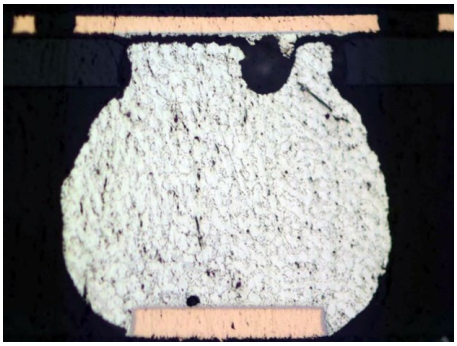

Fig. 3, Separation at device side pad has been observed.

All tested material types in this study (including RO3003™, RO3003G2™, RO4830™, CLTE-MW™ high frequency laminates, as well as XtremeSpeed™ RO1200™ extremely low loss digital circuit material), successfully passed dye and pry testing through 3152 thermal shock cycles for all BGA

device types and surface finishes. While some solder separation was noted beyond 2100–2450 cycles, it was attributed to suspect solder joint quality on the device side rather than the laminate construction or board surface as shown at Fig. 3. No conductor cracks or pad lifting were detected in any configuration across all material combinations, BGA types, or surface finishes.

This evaluation study, though only representative for mentioned above Rogers' PCB materials, is an exemplary demonstration of test methodology to determine reliability of BGA solder joints assembled on hybrid constructions when processed under controlled conditions and subjected to extended thermal cycling. Solder joint integrity is only one aspect of ensuring long-term reliability at the package-to-PCB interface. As package densities increase and BGA designs scale vertically through multiple board layers, the mechanical and thermal performance of the via structures beneath the device becomes equally critical. Failures originating in stacked or blind vias can undermine solder joint reliability, especially under repeated thermal cycling or reflow conditions.

B. Microvia and blind via Reliability

In a complementary study, via reliability evaluations were conducted to assess the behavior of blind, stacked and staggered microvias in multilayer constructions built with low loss thermoset laminates and prepregs. Although the results reflect the characteristics of a specific material set (RO4835T™ Laminate and RO4450T™ Bondply), the objective of the study was to demonstrate a robust and transferable methodology for assessing via reliability under representative assembly and thermal stress conditions. Initial evaluations focused on establishing basic process parameters for sequential bonding and microvia formation using various bondply thicknesses and via diameters. In an early phase, six-layer boards were constructed with two sequential bonding cycles and tested using thermal shock from -65°C to 150°C after 10x 256°C reflow exposures. All test-via topologies, including stacked microvias, showed complete survivorship through 500 thermal shock cycles. Building on these results, more complex follow up studies on 10-layer and 12-layer test vehicles were assembled using corresponding four and five sequential bonding steps and tested with various via structures, stacked, semi-stacked, and staggered, across multiple diameters. Figure 4 shows an example on a 10-layer design that visually demonstrates how stacking of vias supports densifying interconnects under IC packages. In the 12-Layer evaluation test with topology shown in Fig. 5 and Fig. 6, boards were subjected to 500+500 thermal cycles in both HATS (partly representing the IPC D-coupon approach; evaluation of D-coupon is ongoing) and dual-chamber test protocols, simulating -40°C to 150°C and -65°C to 150°C cycling ranges respectively, both before and after six simulated 265°C reflow events. Additional thermal stress testing included Z-axis CTE measurements and time-to-delaminate (T-288) endurance at 288°C for two hours. The testing confirmed excellent survivability for most microvia designs across all tested via topologies and board constructions. When late cycle count failures occurred, they were limited only to the most complex via topologies in 100um via size (>680 cycles) and 125um via size (>980 cycles).

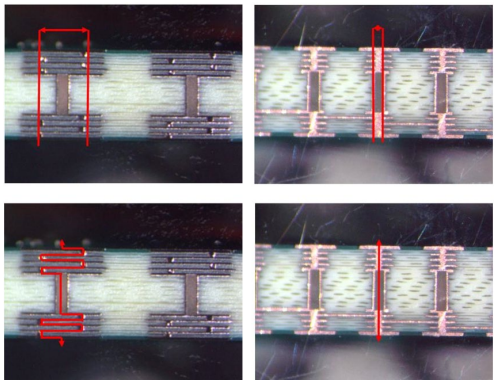

Fig. 4, Visual demonstration of different via topologies in multi-layer construction - staggered (left) vs. stacked (right). The choice of the topology can influence signal path length, signal integrity as well as lateral space requirements.

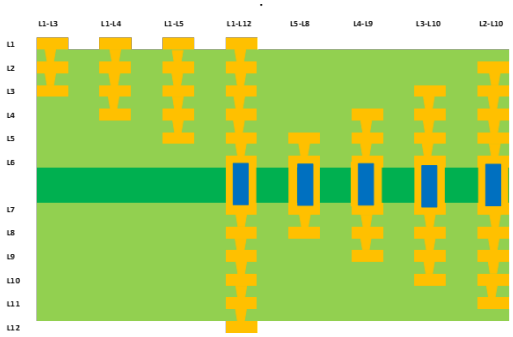

Fig. 5, 12-layer (5 sequential lamination steps) test vehicle for HATS evaluation study shows via topologies under conditioning and test.

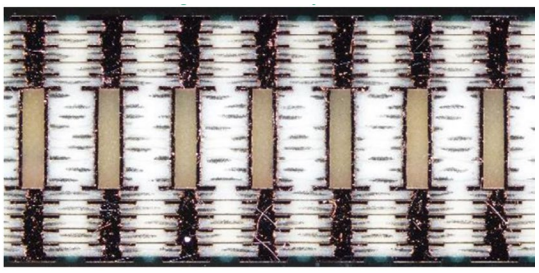

Fig. 6, Cross section microscopic picture of L1-L12 stacked via topology in 5 sequential lamination steps.

This study reinforces the importance of validating sequential bonding, microvia design, and PCB behavior under combined reflow and thermal cycling conditions. While based on a specific low loss thermoset system (as mentioned previously), the testing approach provides a framework for evaluating via reliability in advanced multilayer PCB applications, especially where BGA packages and HDI structures demand high thermal and mechanical robustness as well as limited space for a BGA escape routing.

An additional factor to consider in complex high-speed BGA fan-outs that differential links routed through multiple layers may require intensive back-drilling to remove unused stubs. PTFE cores can be designed to tolerate aggressive mechanical drill parameters due to low glass content and smooth filler geometry, enabling cleaner stub removal compared with glass-woven thermosets. However, the softer PTFE matrix necessitates tighter process control by PCB fabricators to prevent smear due to limited tool life. Beyond this, in engineered thermoset solutions designed for frontier digital electronics applications, regular use of quartz glass yarns is considered to address the IL requirements. This can introduce additional challenges in drill process control. As noted in [13], *"Hole drilling, cleaning and routing are the principal processing steps that are non-standard for quartz-reinforced laminates. In particular, these laminates produce much higher drill wear than their E-glass counterparts."*

C. Laser Via Process Development

In a further study, microvia processing and reliability were evaluated with the aim to examine the performance of blind vias and plated-through-holes (PTH) in hybrid multilayer boards using thin PTFE-based and low-loss thermoset laminate cap layers over thicker FR-4 cores. The purpose of this study was primarily to establish robust application methods for microvias that demonstrate consistent thermal stress survivability. Laser and mechanical drilling methods were applied to fabricate blind vias (0.1–0.2 mm diameter) and mechanically drilled through-holes (0.25–0.50 mm). Evaluated materials included RO3003™, RO3003G2™, RO4830™ and CLTE-MW™ high frequency laminates, as well as XtremeSpeed® RO1200™ extremely low loss digital circuit material. Pre-testing demonstrated that copper surface roughness, filler geometry, glass reinforcement, and resin chemistry significantly affected laser drilling efficiency. Specifically, smoother copper foils, smaller spherical fillers, absence of glass reinforcement, and thermoset resin systems allowed more effective laser processing. For PTFE materials, a dedicated UV laser cleaning step was applied to remove resin residue from the microvia bottom, which significantly enhanced via reliability, as depicted in Fig. 7.

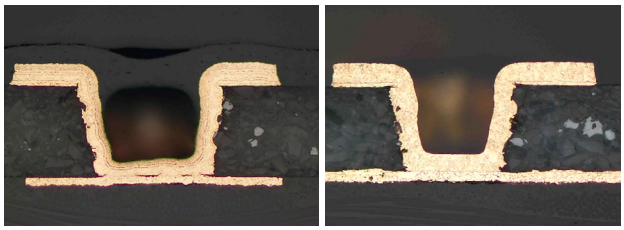

Fig. 7, Left image displays a microvia in non-reinforced PTFE without application of developed UV laser pre-cleaning step. Right side image shows plated microvia after UV laser pre-cleaning has been applied. A consistently more homogenous plating of via bottom is the result of pre-cleaning.

Subsequent reliability testing included thermal shock cycles between -65°C and 150°C for 1000 cycles, with half the samples subjected to 10x reflow cycles at 265°C prior to testing. Most via structures demonstrated excellent survivability across all tested configurations. Also in this study, failures occurred at late cycle counts (>600 cycles) only in high-aspect-ratio blind vias fabricated in materials containing larger filler particles or glass reinforcements. Conversely, non-reinforced constructions using smaller filler particles consistently showed superior microvia reliability.

This study highlights the importance of carefully considering material properties and detailed laser processing methods when evaluating microvia performance. Although in the same way as above, the evaluations utilized specific laminate materials, the conclusions can be generalized, providing IC package designers an additional perspective on microvia integrity and robustness within multilayer PCB assemblies subject to demanding thermal and mechanical stresses.

IV. Application Focus: Aerospace & Defense

Ensuring robust PCB reliability through controlled via formation and optimized laminate selection, as detailed in prior sections, is even more critical in aerospace and defense (A&D) applications, where designs face particularly demanding operational conditions. Radar, electronic warfare, and space-based systems must operate reliably under harsh thermal environments e.g. MIL-STD-883 specify range from -55°C to +150°, often while handling high RF power densities. High thermal conductivity laminates with embedded copper structures and/or thermal via farms offer effective solutions by significantly reducing localized temperature rise. In mission critical applications, direct component placement on PCBs with heavy copper, aluminum or brass metal backing is often applied as an immediate heat spreader.

Environmental durability is another essential factor driving material selection in A&D applications, particularly for airborne systems, and systems exposed to the vacuum of space. High-performance PTFE-ceramic-based laminates inherently exhibit low outgassing characteristics, making them ideal for long-term spacecraft missions, as proven by decades of successful use in deep-space exploration probes [14]. For these applications, laminates also must possess extremely stable dielectric properties (TcDk), across wide temperature extremes, essential for maintaining consistent RF performance. Add to this, material selection with appropriate elastic modulus (e.g. higher elasticity in PTFE-composites, higher rigidity in thermoset-composites) can provide additional resilience to vibration and shock environments routinely encountered in military platforms. Beyond that, the mechanical adaptability of PTFE-based laminates allows significant bending and shaping, supporting innovative form factors and conformal electronic assemblies. In practical experience, these laminates demonstrate reliable conformability down to small bend radii, unlike traditional commercial thermoset laminates which typically only accommodate very large bending radii, as demonstrated in rotating RF joints for CT scanner systems.

Collectively, these attributes: environmental robustness, stable dielectric properties under thermal cycling, mechanical resilience to vibration, effective heat dissipation strategies, and conformability establish advanced PTFE-based (e.g. RT/duroid® 5000 and 6000 Series) and engineered thermoset-composite laminates (e.g. RO4000T, TMM) as reliable solutions in modern aerospace and defense electronics. Leveraging such materials enables IC package and PCB designers in the A&D industry to confidently address performance and reliability trade-offs, achieving critical design goals without sacrificing long-term operational integrity.

V. Conclusion

In summary, designing IC packages for high-frequency, high-speed, or high-power applications requires comprehensive consideration of PCB material properties. By carefully selecting suitable dielectric characteristics, thermo-mechanical stability, and copper surface quality, and rigorously validating these choices through representative PCB test vehicles, IC package engineers can reliably achieve their signal integrity, power integrity, and long-term reliability goals. Applying these considerations enables engineers to confidently pursue performance-critical solutions and push the boundaries of next-generation electronic systems.

Acknowledgments

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