

Facilitating High-Reliability Cu-to-Cu Direct Bonding via Tunable Cu-selective Oxide suppression Coating for Advanced Interconnects

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Abstract

The continuous scaling of semiconductor devices, driven by Moore's Law, demands advancements in interconnect technologies. Cu-to-Cu direct bonding has emerged as a critical solution for enabling ultra-fine pitch, high-density interconnections with superior electrical and thermal performance compared to traditional Cu-to-solder joints. This bonding method is pivotal for applications such as 3D integration, FOWLP, and 2.5D/3D packaging, supporting miniaturization, high-speed data transfer, and improved thermal management. However, Cu oxidation during processing presents a major barrier, degrading bond integrity, increasing interfacial resistance, and complicating backend-of-line (BEOL) packaging integration. To address these challenges, we developed an ultra-thin (2–5 nm) Cu-selective oxide suppression coating using standard industry-compatible techniques such as chemical vapor deposition (CVD) and liquid-phase deposition (LPD). The coating effectively prevents Cu oxidation during high-temperature thermal compression bonding (TCB) without requiring high-vacuum equipment or costly metal coatings, enabling scalability for heterogeneous packaging. RAIRS-QCM metrology validated the coating's chemical stability and persistent oxidation resistance even after two months of ambient storage. RAIRS analysis confirmed ~52% oxidation suppression after 1-hour annealing at 300°C in air. Bonding tests on 5 nm passivated Cu at 300°C, 40 MPa for 1 hour showed strong Cu–Cu bonds with a shear strength of 40.7 ± 4.2 KgF, exceeding MIL-standard. STEM-EDX confirmed a defect-free interface and effective oxidation suppression without hindering bonding. This work establishes the developed coating has strong potential as a scalable, high-throughput solution to enhance Cu-to-Cu bonding reliability, enabling next-generation semiconductor packaging with improved electrical, mechanical, and thermal performance.

Key words

Cu-to-Cu bonding, RAIRS-QCM metrology, ultra-thin passivation coating, Oxide suppression coating

I. Introduction

Over the past six decades, Moore's Law, which predicts that the transistor counts on integrated circuits (ICs) double every two years, has epitomized the simultaneous miniaturization of components and expansion of functionality, driving ongoing reductions in device dimensions, enhanced performance, and deeper functional integration in semiconductor technology [1]. As device geometries have contracted from the micrometer (μm) to nanometer (nm) scale, conventional transistor scaling has encountered fundamental limitations in lithographic resolution, power-density management, and RC delays in interconnects [2]. To extend Moore's Law beyond these limitations, heterogeneous integration has emerged as a vital

strategy. By assembling multiple “chiplets” and die stacks into high-density 2.5D and 3D IC architectures, designers can leverage optimal process nodes, integrate specialized functions, and reduce overall system volume. However, sustaining signal integrity and managing heat in finely pitched interconnect networks demands new materials and bonding methods [3,4].

As illustrated in Figure 1, progressive miniaturization of flip-chip interconnects from $>130 \mu\text{m}$ solder bumps through $60\text{--}140 \mu\text{m}$ solder-capped Cu pillars and $20\text{--}80 \mu\text{m}$ micro-bumps to $<30 \mu\text{m}$ Cu-to-Cu micro-bumps enables higher I/O density. Cu-to-Cu direct bonding has rapidly gained prominence as a foundational technology for next-generation heterogeneous IC assemblies. Enabling

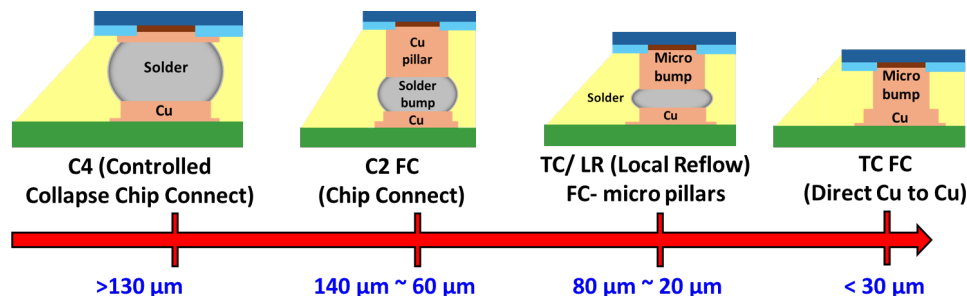


Fig. 1: Evolution of Cu interconnect geometries IC Packaging: Driven by Moore's Law

ultra-fine-pitch 2.5D and 3D integrations, Cu-to-Cu bonding underpins wafer-to-wafer, die-to-wafer, and chiplet-to-chiplet interconnects with pitches well below $20\ \mu\text{m}$ [5]. Such direct metal-to-metal interconnects have become crucial for the development of high-bandwidth memory (HBM) stacks, compact logic-memory integrated modules, and power-intensive AI accelerators that require terabyte-per-second data throughput [6]. Unlike traditional solder-based joints, Cu-to-Cu bonding eliminates intermetallic compounds (IMC) and flux residues, thereby reducing process complexity and contamination risk. Furthermore, Cu's intrinsic properties deliver exceptionally low interconnect resistance, minimizing RC delay and superior thermal conductivity, which is critical for heat dissipation in densely packed die stacks [7]. Cu-to-Cu direct bonding's high electrical and thermal performance enables high-density, high-speed, and thermally efficient topologies in modern heterogeneous IC packaging [8].

Despite its advantages, Cu-to-Cu direct bonding faces significant challenges that hinder its widespread adoption in advanced semiconductor packaging and 3D integration. A primary obstacle is the rapid formation of native Cu-oxide ($\text{CuO}/\text{Cu}_2\text{O}$) layer even in tightly controlled, low-oxygen environments, creating insulating layers that impede atomic diffusion at bonding interfaces [9]. Achieving planar, oxide-free surfaces typically demands aggressive cleaning or surface activation processes, while surface activation methods like acetic acid pretreatment can remove oxides temporarily, reoxidation occurs within minutes if bonding delays exceed 3 minutes [10]. And any residual topography or surface roughness and planarity further complicate bonding mechanics. Electroplated Cu films typically exhibit roughness values between 3-12 nm depending on crystal orientation, necessitating chemical-mechanical planarization (CMP) to achieve sub-10 nm smoothness for reliable thermo-compression bonding (TCB) [11]. The crystallographic orientation also influences diffusion kinetics, with (111)-oriented surfaces showing faster atomic migration but requiring precise nanostructuring to minimize oxidation rates [9]. Long-term reliability concerns persist due to residual interfacial defects. Void ripening occurs during thermal cycling, with grain boundary diffusion driving pore

coalescence at bonded interfaces [12]. Subcritical oxidation at bonding boundaries progresses over time, particularly in (100)-oriented Cu films, which oxidize $2.3\times$ faster than (111)-oriented counterparts at 250°C [9]. These failure mechanisms necessitate comprehensive solutions addressing both initial process limitations and operational degradation pathways to enable robust Cu-to-Cu interconnects for next-generation electronic systems.

To overcome the challenges inherent to Cu-to-Cu direct bonding, industrial research has focused intensively on surface preparation and protection methods. Plasma treatments employing Ar/H_2 mixtures have become a common approach to remove native copper oxides by chemically reducing surface layers and sputtering contaminants away. Similarly, formic acid vapor treatments effectively reduce Cu-oxides at mild conditions, promoting clean metallic interfaces suitable for bonding [10,13]. Additionally, protective metal coatings, including gold (Au), palladium (Pd) [14], and silver (Ag) [15], have been explored as diffusion barriers and oxidation-resistant capping layers, significantly enhancing surface stability and bondability. However, despite their proven efficacy, these strategies have notable drawbacks. Plasma and formic acid cleaning typically require costly ultra-high vacuum chambers and specialized handling equipment, escalating capital investment and operational complexity. Residual contaminants and by-products from cleaning processes pose further complications, especially at ultra-fine pitch interconnects below $10\ \mu\text{m}$, where even trace residues significantly degrade bonding reliability and yield. The incorporation of protective metal coatings, while effective, introduces new process integration hurdles and potential intermetallic compound formation, thus complicating downstream manufacturing steps.

Additionally, maintaining precise control and consistency during cleaning treatments becomes increasingly challenging as device interconnect pitches continue to shrink. Surface activation processes designed for low-temperature bonding (typically below 200°C) are under investigation to address these issues. Still, their application in high-volume manufacturing environments remains limited

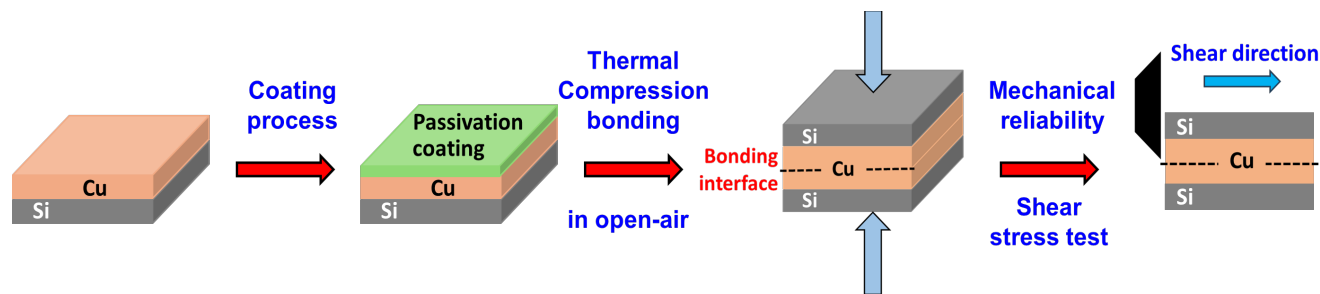


Fig. 2: Coating and Thermal Compression Bonding (TCB) Scheme

due to difficulties ensuring uniform activation and long-term stability [16].

In our previous research, we addressed the persistent challenge of solder flux residue difficult to remove in fine-pitch Cu-to-solder interconnects by eliminating the need for solder flux altogether [17]. To achieve this, we developed an ultra-thin (2–5 nm), Cu-selective oxide suppression coating capable of significantly reducing copper oxidation at elevated bonding temperatures (250–300 °C). This protective coating ensures optimal formation of intermetallic compounds (Cu_6Sn_5 and Cu_3Sn) through enhanced Cu-Sn interdiffusion, selectively adhering to Cu while exhibiting no reactivity towards other common materials such as Al, Ni, Au, Ag, dielectric materials, or polymer substrates [18]. Reliable Cu-to-Cu direct bonding is similarly impeded by copper oxidation, which disrupts atomic-scale interdiffusion and compromises bond strength. To overcome this issue, we applied the same Cu-selective ultra-thin passivation coating, deposited via industry-standard methods such as liquid-phase deposition (LPD) or chemical vapor deposition (CVD), ensuring straightforward integration into current manufacturing processes. By effectively preventing oxide formation, our passivation layer facilitates robust Cu–Cu bonding, even in open-air conditions without the necessity for ultra-high vacuum environments.

II. Experimental Methods and Materials

A. Chemical quantification of passivation coating and Copper oxide:

Passivation coating and bonding assessments were performed on CMP-polished substrates consisting of a 2 μm -thick Cu layer deposited over a tantalum (Ta) barrier and a silicon dioxide (SiO_2) dielectric on a Si wafer. The crystallinity of the Cu surface was characterized using grazing incidence X-ray diffraction (GIXRD) with a Rigaku SmartLab diffractometer at a fixed incident angle of 0.5° . Surface morphology was examined using a Thermo Scientific Quattro S Environmental Scanning Electron Microscope (ESEM) operated in backscatter mode at an accelerating voltage of 10 kV. Surface roughness was quantitatively assessed with atomic force microscopy (AFM) using a Nanosurf Mobile S system.

In our prior publication, we established a robust calibration methodology to quantitatively evaluate passivation coating and oxide growth on Cu surfaces. This approach integrates Fourier-transform infrared (FT-IR) spectroscopy with Reflection Absorption IR Spectroscopy (RAIRS) and Quartz Crystal Microbalance (QCM) techniques, which respectively measure IR absorbance and coating thickness, enabling a precise correlation between spectroscopic signatures and mass-based measurements for accurate thickness quantification [19]. Chemical bonding features of the passivation coating and Cu-oxide were identified through characteristic IR absorbance peaks, notably at 788 cm^{-1} for the passivation coating and 650 cm^{-1} for Cu-oxide. Spectral measurements were performed using a Thermo-Nicolet iS50 FTIR instrument equipped with a VeeMax II reflection accessory. To correlate absorbance and physical thickness, thickness changes data were obtained via QCM analysis using CHI 440A Potentiostat and 8 MHz quartz crystals sputtered with 99.99% Cu, followed by passivation coating and oxide growth.

Oxide suppression rate of the passivation coating was assessed by comparing uncoated (control) and passivated Cu substrates (3 samples per set) when thermally annealed on a hot plate at 300°C for 60 minutes in ambient air, simulating conditions of the TCB process to evaluate its oxidation behavior. To track oxide formation dynamics and evaluate how well the passivation layer suppressed oxidation, FT-IR measurements were taken at 5-minute intervals across the annealing duration. These findings provide useful analysis of the thermal stability and oxidation resistance of the coated surfaces under TCB-relevant thermal stress.

B. TCB set-up and bonding profile and shear test setup Description:

Figure 2 illustrates the process flow for evaluating passivated Cu-to-Cu bonding. The purpose-designed coating process outlined in our patent application [19,20], was applied to Cu substrates with a bonding area of $0.5 \times 0.5\text{ cm}^2$. The coating was deposited by using either LPD or CVD, with thickness tailored by optimizing key parameters such as solution concentration, bath temperature, and coating duration. Following surface preparation, thermal compression bonding (TCB) was conducted in ambient air using a lab-built thermal hydraulic press, with bonding

temperatures ranging from 250 to 300°C, by applying pressures between 20 and 40 MPa, and with a bonding duration of 1 hour. A post-bond annealing step was performed at 220 °C for 1 hour under ambient condition to further stabilize the interface. The bonded structures were subsequently subjected to shear stress testing to evaluate the mechanical integrity of the bonding interface. A minimum shear strength of ~ 31 kgf/cm² was established as the required threshold for bonded samples, calculated following the MIL-STD-883G Method 2019.7 standard [21].

C. Post-bonding analysis description:

Mechanical cross-sectional polishing was conducted on Cu-to-Cu bonded samples to assess interfacial bonding quality. High-resolution interface analysis was performed using a Talos F200X G2 Scanning Transmission Electron Microscope (STEM) (Thermo Fisher Scientific), operated at an accelerating voltage of 200 kV, to investigate atomic diffusion characteristics and determine any potential influence of the passivation coating on bond formation. Samples were precisely prepared using focused ion beam (FIB) milling, following the established procedure described in [22]. Elemental composition and distribution across the bonded interface were further characterized by energy-dispersive X-ray spectroscopy (EDX) mapping.

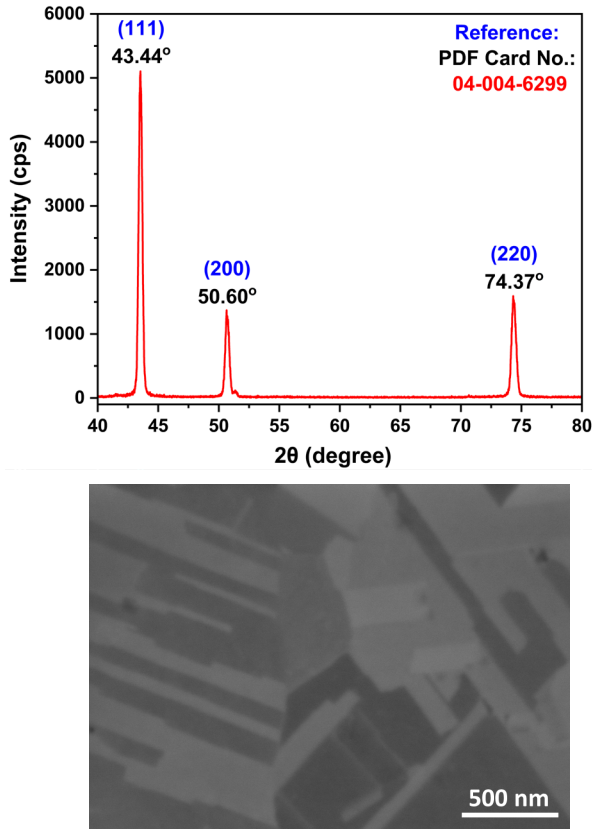


Fig. 3: a) Grazing angle XRD pattern and b) SEM backscatter image of CMP Cu substrate

III. Results and Discussion

A. Surface Crystallinity and Morphology Analysis on Cu substrate:

Substrates composed of CMP-polished 2 μm-thick Cu deposited over a Ta barrier and SiO₂ dielectric on a silicon wafer were characterized to assess their structural and morphological properties. As shown in figure 3 (a), the XRD pattern exhibits sharp and well-resolved diffraction peaks at 2θ values of 43.44°, 50.60°, and 74.37°, corresponding to the (111), (200), and (220) lattice planes of face-centered cubic (FCC) Cu, indicating a high degree of crystallinity. The presence of multiple reflections confirms that the deposited Cu film is polycrystalline in nature, with grains oriented along various crystallographic directions. The absence of secondary phases or impurity peaks further validates the phase purity of the Cu layer in agreement with the standard reference (PDF Card No.: 04-004-6299). Complementing this, the SEM image in Figure 3(b) reveals a dense and uniform surface morphology with well-defined grain boundaries and elongated grains, further supporting the polycrystalline nature of the Cu film.

Figure 4 shows the AFM analysis of the CMP-polished Cu surface, captured over a 10 μm × 10 μm scan area to assess its nanoscale topography. The 3D surface profile demonstrates a uniformly smooth, with almost no surface irregularities, reflecting effective planarization. The average surface roughness (R_a) was measured at 0.5 ± 0.03 nm, while the root mean square roughness (R_q) was 0.7 ± 0.01 nm, confirming the surface's suitability for high-precision bonding applications.

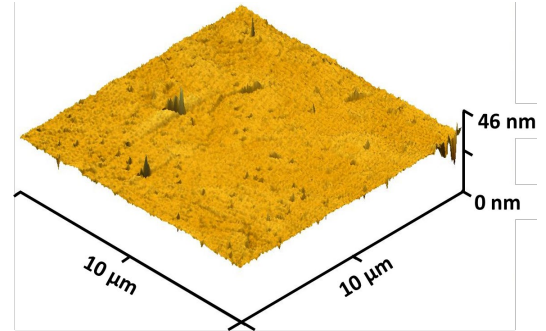


Fig. 4: AFM 3D surface image of CMP Cu substrate

B. Passivation coating thickness quantification:

Thickness quantification for precise control of the ultra-thin passivation coating was performed using the established RAIRS-QCM metrology approach, as detailed in our previous study [18]. According to the calibration curve developed therein, an absorbance intensity of 1 mAbs at the characteristic vibrational peak located at 788 cm⁻¹ corresponds to a coating thickness of ~ 5 nm. Figure 5 presents the RAIRS spectra for Cu substrates coated with 5 nm and 10 nm passivation coatings. The absorbance at

788 cm^{-1} increases proportionally with coating thickness, validating the reliability of the calibration method. The distinct peak intensity variation confirms the ability of RAIRS to non-destructively resolve sub-10 nm thickness differences with high sensitivity, making it a valuable tool for monitoring ultrathin film deposition in advanced packaging processes.

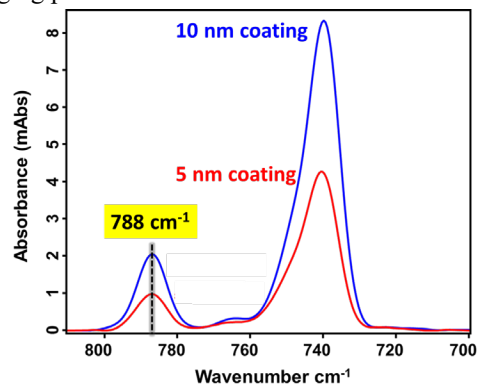


Fig. 5: RAIRS spectra for passivation coatings of different thicknesses

C. Copper-oxide suppression quantification:

The comparative analysis of oxide growth on bare Cu and 5 nm passivated Cu substrates subjected to thermal annealing at 300°C for 60 minutes in ambient air, simulating conditions relevant to TCB. Oxide thickness was monitored using RAIRS by measuring the IR absorbance in the $650\text{--}600\text{ cm}^{-1}$ range, which corresponds to the vibrational mode of Cu-oxide. The bare Cu sample exhibits a rapid increase in oxide thickness over time, reaching $\sim 180\text{ mAbs}$ after 60 minutes of annealing. In contrast, the 5 nm passivated Cu sample shows significantly slower oxide growth, with a final thickness of $\sim 86\text{ mAbs}$. This represents $\sim 52\%$ of oxide suppression rate, demonstrating the effectiveness of the ultra-thin passivation coating in mitigating Cu oxidation under elevated temperatures associated with bonding processes (Figure 6).

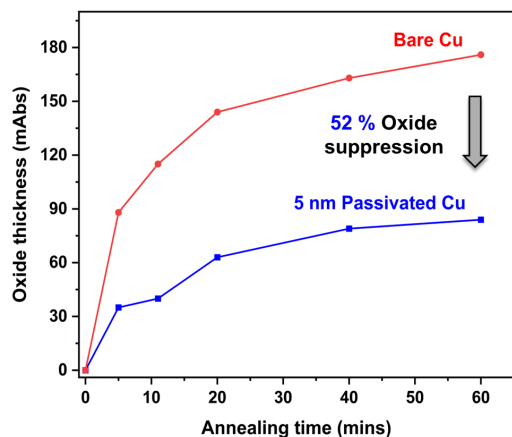


Fig. 6: RAIRS analysis of oxide suppression at 300°C on bare Cu versus 5 nm passivated Cu substrates.

Figure 7 illustrates a time-resolved RAIRS analysis performed over a 30-day period to evaluate the long-term stability of the passivation coating on Cu substrates under ambient storage conditions. Spectra were collected at regular intervals of every 10 days and plotted to monitor changes in the characteristic absorbance features of the coating and any potential oxidation. The characteristic absorbance peak at 788 cm^{-1} , associated with the passivation layer, remains consistent in both position and intensity across all periods, indicating no significant change in coating thickness or chemical degradation. Additionally, no new peaks appear in the $650\text{--}600\text{ cm}^{-1}$ region, corresponding to Cu-oxide, confirming the chemical stability and protective efficacy of the passivation coating, with no substantial degradation or oxide breakthrough even after 30 days of air exposure.

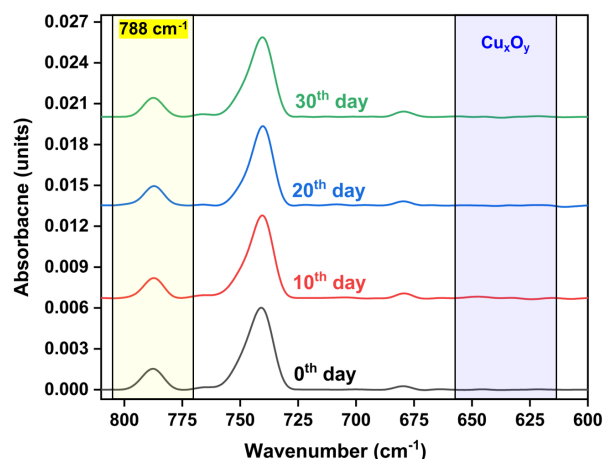


Fig. 7: Queue time evaluation of 5 nm passivated Cu after one-month of open-air exposure

D. Post-bonding analysis and STEM/EDX results:

Bonding assessments using passivated Cu substrates were conducted under ambient conditions, employing thermal compression bonding (TCB) at 300°C with a bonding pressure of 40 MPa for 1 hour, followed by post-annealing at 220°C for an additional hour. After bonding, the samples were cold-mounted and cross-sectioned for detailed interfacial analysis. Figure 8 presents high-angle annular dark-field (HAADF) STEM imaging along with EDX elemental mapping of the Cu-to-Cu bonded structure. The cross-sectional STEM image clearly identifies the bonding interface (highlighted in red) between the top and bottom passivated Cu substrates. Elemental mapping was performed for Cu, O, C, Ta, and Si to evaluate the interfacial composition. Notably, the oxygen (O) map shows minimal intensity at the bonding interface, indicating the effective suppression of oxide formation, a critical factor for reliable Cu-to-Cu bonding. Furthermore, the absence of carbon (C) signals at the interface confirms that no detectable passivation residue or contamination remains post-bonding.

Figure 9 presents a low-angle annular dark-field (LAADF) STEM image of the Cu-to-Cu interface between passivated

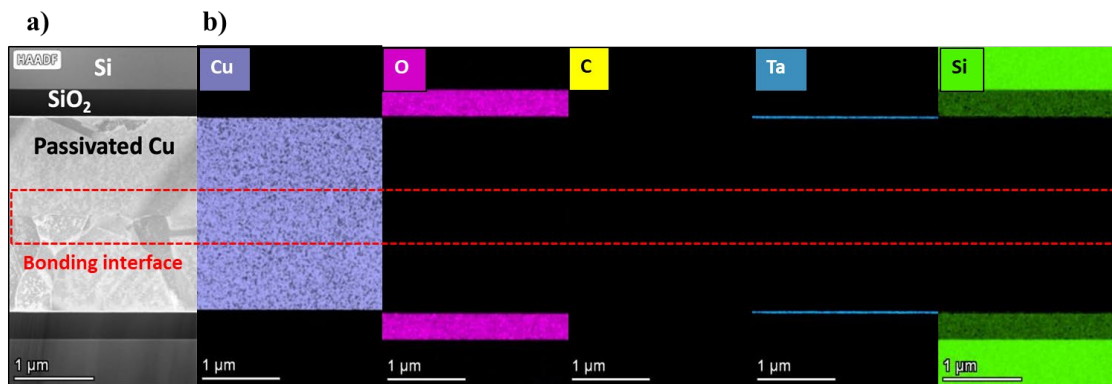


Fig. 8: a) Cross-sectional STEM image and b) EDX mapping at the passivated Cu to Cu bonding interface

substrates, revealing good contact across the Cu-Cu interface was present during TCB. This indicates effective Cu-to-Cu interdiffusion and grain growth, which are characteristic of a strong metallurgical bond. Notably, no residual passivation layer is observed, confirming unobstructed atomic transport and a clean, chemically bonded interface.

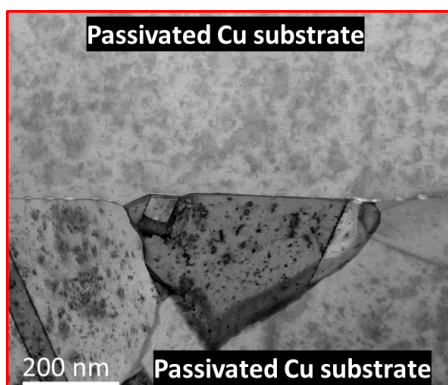


Fig. 9: Cross-sectional STEM LAADF image at the bonding interface.

E. Mechanical reliability testing:

Following the bonding process, shear stress testing was performed on the passivated Cu substrates to assess the mechanical strength of the bonded interface. As depicted in Figure 10, the Cu-to-Cu bonded samples achieved an average (3 sample set) shear strength of 40.7 kgf/cm², surpassing the minimum threshold calculated using MIL-STD 883G Method 2019.9 for a 0.5 × 0.5 cm² bonding area. Notably, post-fracture analysis revealed that failure propagated through the silicon substrate rather than the Cu-to-Cu interface, further confirming the superior interfacial strength achieved during bonding. The absence of failure at the metallurgical junction underscores the effectiveness of the passivation strategy and its compatibility with ambient bonding conditions. These findings collectively validate the mechanical reliability and interfacial integrity of the Cu-to-Cu bonds for advanced packaging applications.

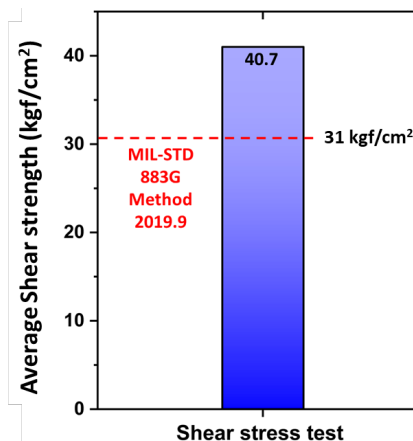


Fig. 10: Mechanical assessment using shear stress test.

IV. Conclusion

This study presents a novel approach to advancing Cu-to-Cu direct bonding reliability by introducing a Cu-selective, ultra-thin oxide suppression coating. Applied via scalable CVD or LPD, the 2 to 5 nm passivation layer significantly reduces copper oxidation during high-temperature thermal compression bonding (TCB) at ~300°C, achieving an oxidation suppression efficiency of approximately 52% as validated by RAIRS-QCM analysis. The coating also maintains chemical integrity under ambient storage, demonstrating long-term stability without an increase in Cu-oxide. Mechanical and interfacial evaluations confirmed robust bonding performance, with average shear strength (40.7 kgf/cm²) exceeding MIL-STD-883G benchmarks and STEM/EDX analyses verifying clean, oxide-free interfaces with excellent Cu-Cu bonded interface. In-depth interfacial research will be pursued to further elucidate the atomic-scale bonding mechanisms and optimize coating-bond interactions. This passivation approach provides a promise solution for cost-effective, high-throughput fabrication of fine-pitch interconnects, supporting advanced heterogeneous integration in high-performance computing and next-generation semiconductor packaging.

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