RF-SiP Chip Package Interaction Finite Element Analysis

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Abstract

Radio frequency (RF) system in package (SiP) is a packaging technology that integrates multiple chips (including RFICs, digital ICs and passive components) into a single package to form a compact RF system. It enables smaller form factor by placing different functional components into one single package. While most finite element analysis (FEA) of chip package interaction (CPI) study cover details on either die back end of line (BEOL) or under bump metallization (UBM) structure, this paper adopts a different approach. It uses a global model type approach and focuses on relative comparison in RF design CPI study. RF-SiP related features, such as die to die/component interaction, double side related influence; die size and die aspect ratio impact are discussed. The findings hope to shed light on the design of new SiP Packages.

Key words

RF SiP, double sided, die to die interaction, bump distribution.

I. Introduction

5G RF (radio frequency) packaging presents new challenges due to the high-frequency range required by next-generation wireless systems. Modules are becoming more compact, multifunctional due to integration of antenna, filters, power amplifiers and other components. Those components usually encompass multiple bands and frequencies and need to work seamlessly together. Industry demands smaller, denser, and thinner packages. Package type has evolved from single-sided to double-sided. RF shielding for the full module as well as individual components is also becoming more important. On the other side, die comes with different size and shape to maximize the real estate available and minimize the cost. To qualify the full module, each individual die needs pass stringent RF reliability test.

Currently system-in-package (SiP) is a popular technology for packaging RF front end modules. There has been a lot of modeling work on multi-chip module (MCM) or SiP structures [1]-[2]. While a lot of those work has been focused on structures like chip back end of line (BEOL) or under bump metallization (UBM) [3]-[5], this paper adopted a different approach. This paper utilizes a "global" type approach to examine the CPI stress due to coefficient of thermal expansion (CTE) mismatch between the die, laminate and mold. In this case, the study does not go into many details of the die/bump structure itself. The papers aim to shed some light on the design of RF SiP modules, although not able to cover the full spectrum surrounding this big topic.

II. FEA Simulation Model Setup

A. Model Setup

As shown in Fig. 1, there are several unique features of RF-SiP packages. Multiple dies with different interconnect technology and components can pack closely together, and compartmental shielding wires or blocks can be used. The die size and aspect ratio can vary across different designs. The module can be single sided or doubled sided.

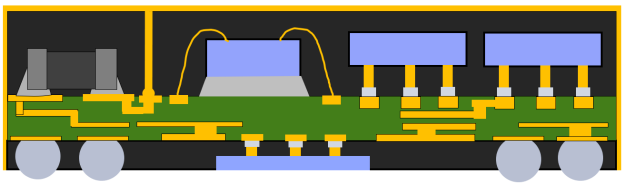

Fig. 1. Double side molded RF-SiP structure schematic

In our simulation, a test package (7x5x0.7mm) as shown in Fig. 2 and Fig. 3 is used for most of the simulations and its variants. It is a molded land grid array (LGA) package. On top of this package, there are three silicon dies, S1, S2 and S3. Also, C1-C5 are surface mount device (SMD) components. In some of the DOEs, some dies would be depopulated/shifted, as in Fig. 4. And SMD components can be modified to block shielding components or wire shielding components by disabling some elements. Silicon dies have uniform bump pitch in the test vehicle.
Most of the simulations are performed on a remote Linux cluster with 256GB memory, 8 CPU cores. ANSYS Mechanical software 2019 R1 is used. Result postprocessing has used customized ANSYS ACT (ANSYS customization toolkit) extension.

extension

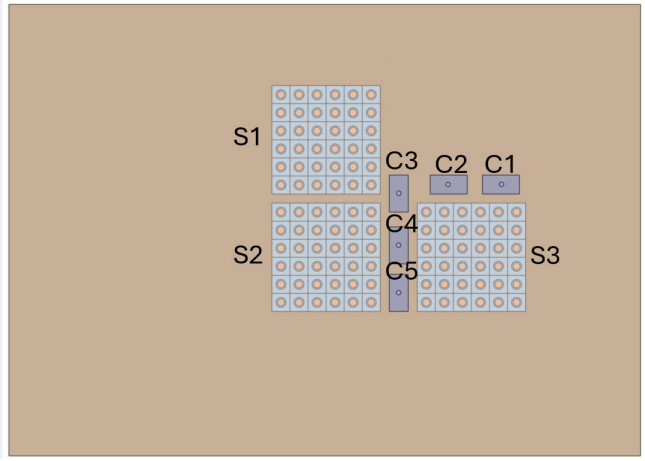

Fig. 2. Package configurations with S2 placed in the center, with neighboring dies and surface mounted components.

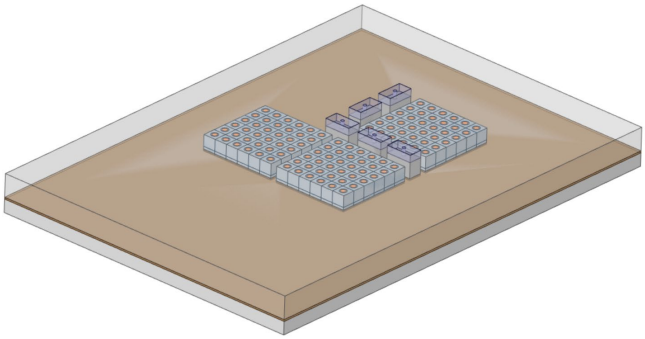

Fig. 3. Isometric view of the test single sided package

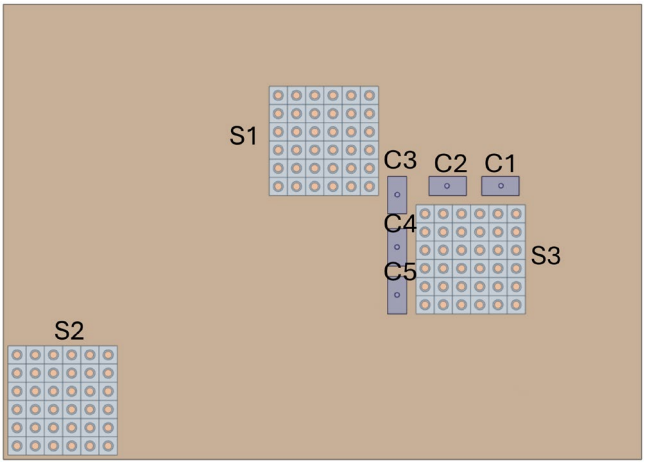

Fig. 4. Package configurations when S2 placed to the left bottom corner

B. Stress Metrics

For all the results, a cross-section volume averaged equivalent stress is used, averaged across in each bump. Thus each bump would have a single stress number reported. And for the full die like S2, a stress map can be bubble plotted which covers all the bumps. This bubble plot is important as it tells the distribution of stress.

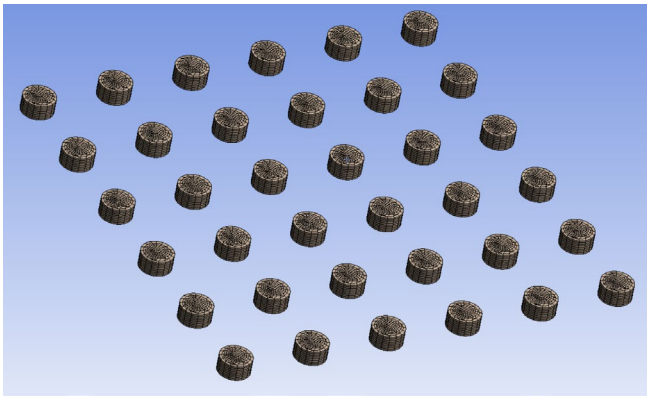

Fig. 5. FEA mesh showing all the bumps where the stress is volume weight averaged in each bump

III. RF SiP CPI Stress Influence Factors Study

A. Die to Die, Die to Component Study

If we depopulate S1 die and other components, the S2 die all four corners initially would have same stress values (normalized value ~ 1.0). However, the stress shifted due to the presence of S1 die. As shown in the stress bubble plot of Fig. 6, the bubble size represents the stress values and four corners of S2 die have largest stress numbers. Due to the influence of S1 die nearby, the upper side bumps of S2 die showed smaller stress numbers than counterparts of the lower side. The result suggests that nearby die could help relieve bump stress.

Fig. 6. Bubble plot of normalized bump stress for S2 die placed in the center with the influence of S1 die and other components. Top corner bumps showed smaller stress than bottom row due to influence of S1 die.

In another study where examine the placement of the S2 die(other die and SMD depopulated/disabled to isolate the influence), as shown in Fig. 7, when we move the S2 die from the center (where initially all four corner stress numbers are 1.0) to the left bottom corner of the package, all four corner stress number dropped, with especially the left corner has dropped to 83% of its original value. Other bumps have also dropped by different percentages. This is because when placing the die to the edge, the package can deform more to accommodate the CTE difference between the chip and the laminate. This bending is beneficial for stress reduction. When the die placed in the center, it is more difficult to deform the laminate, thus the stress level would be high. From the application side, it tells us that if there is a chip passed CPI related qualification in one module when placed near the package edge, it is not risk free to re-use it in another package where it is placed more toward the center.

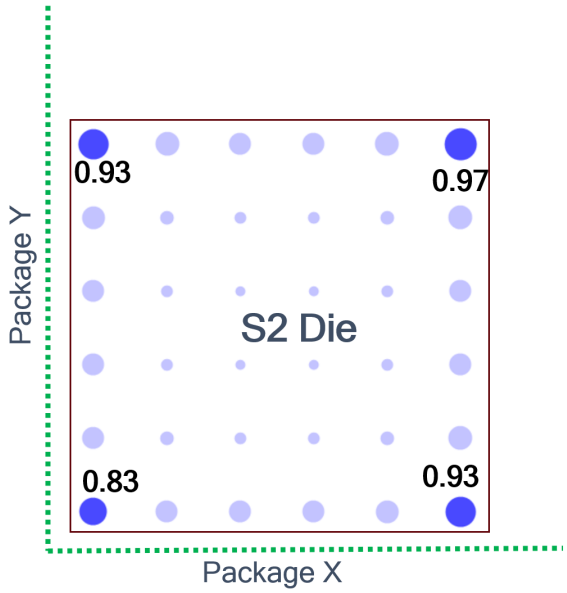

Fig. 7. Bubble plot of normalized bump stress after moving S2 die from center to left bottom corner of the package. In this study, all dies and components other than S2 are not included

In order to better understand the influence of die-to-die distance to CPI stress, more design legs are simulated. S1-S2 die distance varies from 50um to 600um, together with one case where S1 die depopulated, and another case where S1-S2 die completely merge to a single die. As shown in Fig. 8, stress number goes up by 4% when S1-S2 die distance goes from 50um-600um. This indicate it is a relatively weak influence. Completely remove S1 die stress increases by 7.7%. When we merge those two dies to a single large die (not simply bring gap to 0um), stress dropped significantly, high stress pins appear at the combined S1-S2 die corners and the original S2 top left corner pin stress dropped significantly, to 68% of its original value. This is because the stress neutral point (NP) is different, rather than two NPs at original each die's center, the combined die has a new NP at their combined die center. The original S2 top left bump's distance to neutral point (DNP) become smaller when merged and thus stress get reduced. The reason CPI stress in the current configuration is not very sensitive to die relative distance is because the above simulation is primary driven by the CTE mismatch between the die and its underlying laminate and without the existence of the mold, die is relatively small compared with the full package. Factors like mold, thinner package, larger die could make the influence more obvious and requires further study.

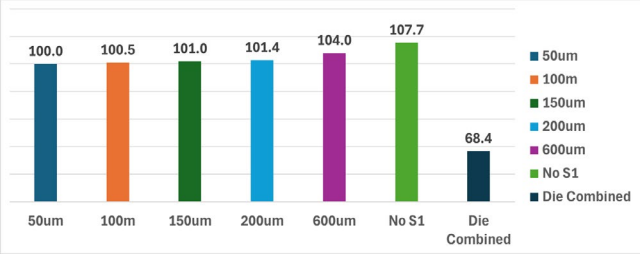

Fig. 8. S1-S2 die distance's influence to S2 bump stress (S2 top left corner normalized bump stress shown).

Another study performed is to examine the SMD component and compartmental shielding's impact. As shown in Fig. 9, SMD component presence near the die lowers the stress by about 3%. Presence of copper shielding block of same size as SMD component (but taller up to the mold top surface) showed the stress increase about 5%. While a wire shielding (small circles in the component as shown in Fig. 2) shows almost negligible influence. The reason SMD and copper block shielding showed different trends is because of their different CTE values. SMD has lower CTE values than the laminate, while copper shielding block has higher CTE than the laminate. Thus, SMD helps with stress reduction and copper shielding block make it worse. On the application side, one lesson could take away is try avoiding putting large copper block near stress critical bumps as it can cause CPI stress increase.

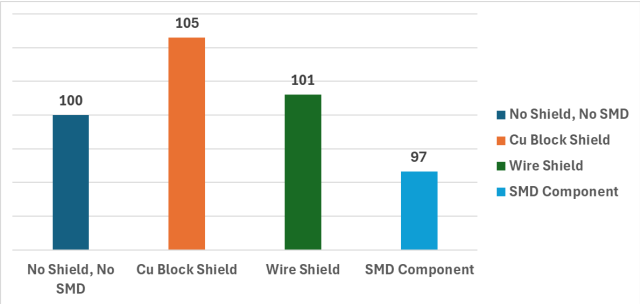

Fig. 9. Shielding and SMD component's influence to S2 bump stress (S2 top right corner bump normalized stress shown).

B. Laminate Impact

One important finding in the laminate design is the bump stress shows sensitive to its underlying metallization. As shown in Fig. 10, in the test package where the square regions surrounding the capture pad switched to fully copper material, the stress jumped up by 4% as shown in Fig. 12. The difference can be higher in realistic designs. For instance, in one of a realistic package where the underlying metal shown in Fig. 11, the stress value jumped by about 15%. The reason the stress increased is because the presence of copper made the laminate stiffer and also increased the CTE surrounding the bump region. Because of this, it is suggested to avoid having large metal piece on M1 layer for the stress critical pins. Instead, via in pad structure can be used to route the signal out in other layers.

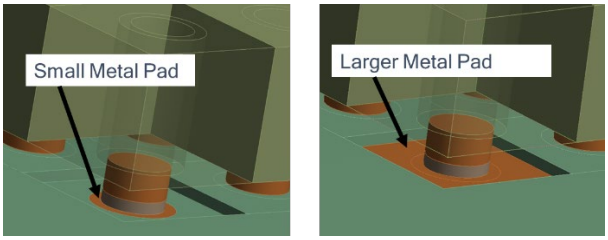

Fig. 10. Test package metal pad difference under the pin.

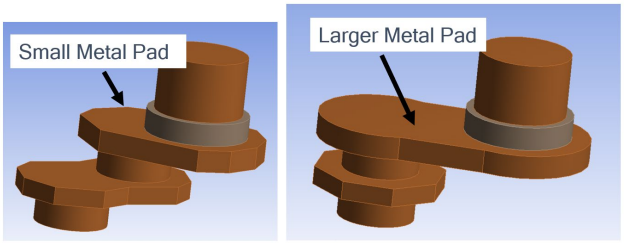

Fig. 11. Realistic design metal pad difference under the pin.

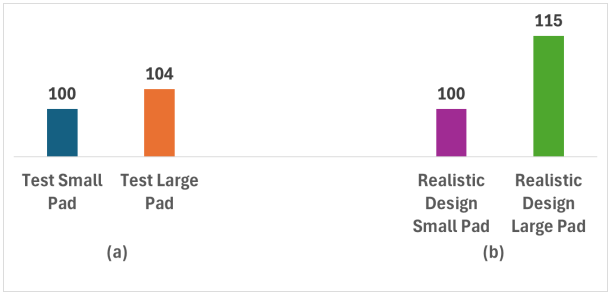

Fig. 12. Under pin laminate metallization impact to stress (a) Test package. (b) Realistic package.

C. Double Side RF SiP module

In double side molded SiP package, dies are assembled from both top and bottom sides (Fig. 13). In the top first assembly process flow, one question is how does the top assembled components affect the bottom assembly stress? We did one study as shown in Fig. 14. The result indicates that for the same die, bottom die attach showed lower stress numbers than the top die attach.

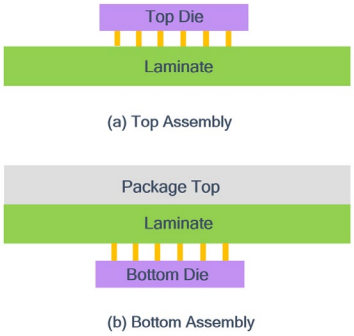

Fig. 13. Schematic showing: (a) top die attach and (b) bottom die attach for double sided RF SiP module.

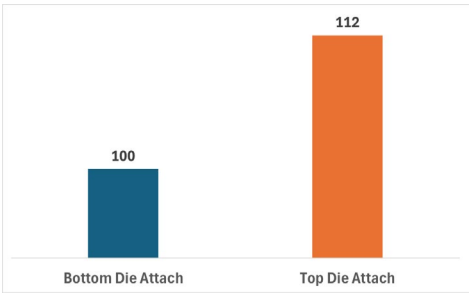

Fig. 14. Stress comparison for top die attach and bottom die attach.

However, caution should be taken as this is not a monolithic trend. As shown in Fig. 15, when the top mold thickness varies, the stress first drops down, then goes up. And the deflection is in the opposite direction, first goes up, then goes down. So the top assembled component's influence to bottom assembly stress is case dependent and can vary from package to package.

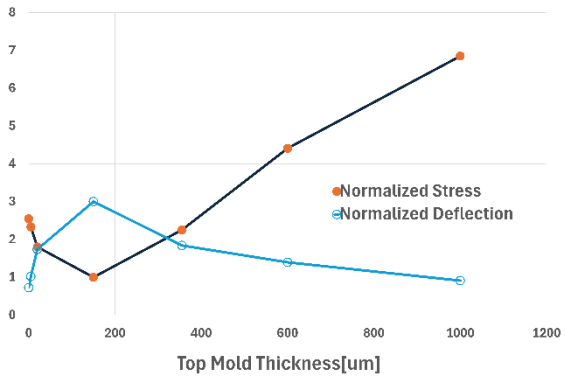

Fig. 15. Top mold thickness influence to bottom die stress and deflection (Uz) in double sided RF SiP package.

Why would the double side package have such a non-monolithic trend? This could probably be explained using the bimetallic strip example as shown in Fig. 16. Top strip lumps top mold and components, and the bottom strip lumps laminate and bottom die. With their thickness, modulus and CTE defined as t_a, E_a, γ_a and t_b, E_b, γ_b for top and bottom strip respectively. Assuming length of the strip is L. stress free reference temperature is T_0 and current temperature is T,

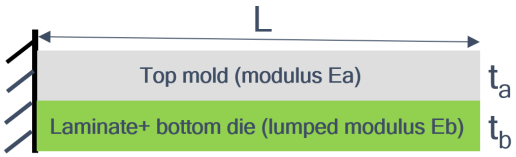

Fig. 16. Schematic drawing showing bimetallic strip setup.

There is a classical analytical solution to account for the deflection U_z due to the CTE mismatch of the bimetallic strip [6], as shown in equation below:

$$U_z = \frac{3L^2(\gamma_b - \gamma_a)(T - T_0)}{t_b} \cdot S \quad (1)$$

Where dimensionless variable S and K_1 are defined as:

$$S = (t_a + t_b)/(t_b K_1) \quad (2)$$

And

$$K_1 = 4 + 6\frac{t_a}{t_b} + 4\left(\frac{t_a}{t_b}\right)^2 + \frac{E_a}{E_b}\left(\frac{t_a}{t_b}\right)^3 + \frac{E_b}{E_a}\frac{t_b}{t_a} \quad (3)$$

If we define thickness ratio R as

$$R = t_a/t_b \quad (4)$$

Then dimensionless variable S becomes:

$$S = \frac{1+R}{4(1+R^2)+6R+(E_a/E_b)\cdot R^3+(E_b/E_a)/R} \quad (5)$$

S is a dimensionless variable defined here; it depends on R and Young's modulus ratio E_a/E_b. S can be plotted as in Fig. 17.

For a fixed set configuration of L, T, T_0, γ_a, γ_b and t_b, when we vary the thickness of mold t_a, the deformation U_z varies proportionally with S. As shown in Fig. 17, S is not monolithically increasing with R. instead, it peaks at certain R value and then drops down again. Which means there is an optimum mold thickness for maximum deflection U_z.

This behavior explains why in our actual study, the normalized deflection curve in Fig. 15 showed a peak and then drops. There is an inflection point, where top components and bottom laminate/die's equivalent stiffness are most compatible, thus at this inflection point, the deformation reaches maximum value and stress reaches minimum.

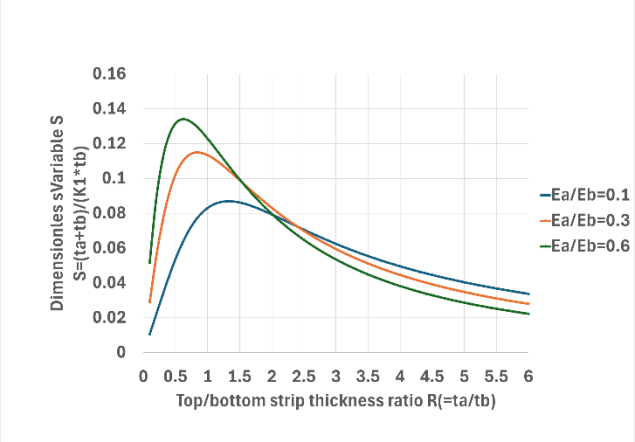

Fig. 17. X dimensionless variable S varies with top/bottom strip thickness ratio (parameter R) for different Young's modulus ratio combination (E_a/E_b).

D. Die Size and Aspect Ratio Variations

RF SiP package comes with different die sizes and die aspect ratios. Controlled FEA study showed their impact in Fig. 18. When the die size is small, the stress increases dramatically with area growth, but the trend slows down when the die size is larger and more compatible with the package size. Die aspect ratio showed a weak dependency, meaning with similar die area, there isn't a large difference on the CPI stress between different aspect ratios. The result suggests larger aspect ratio die can be used to fit into the design space.

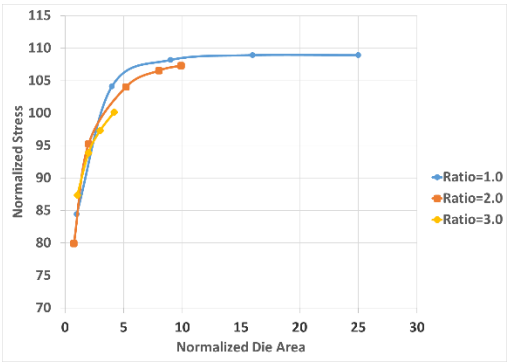

Fig. 18. Die area and aspect ratio influence bump stress.

E. Bump Distribution

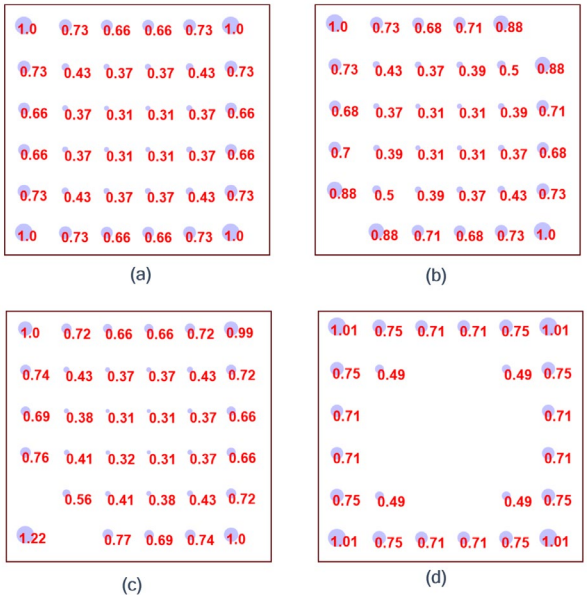

Fig. 19. Bubble plot of stress values on S2 die for (a) reference design with all pins populated (b) two corner pins depopulate (c) two neighboring pins depopulated (d) center depopulated

Bump distribution pattern study has also been carried out by FEA. As shown in Fig. 19, all the stress levels have been normalized by the max corner stress value in the reference design of Fig. 19(a). If depopulating the corner pins, the stress of neighboring pins has gone up from 0.73 to 0.88 as shown in Fig. 19(b). If depopulating two neighboring pins, the corner pin stress has gone up from 1.0 to 1.22 as shown in Fig. 19(c). If depopulating a group of center pins as shown in Fig. 19(d), the stress value has limited change. The result suggest that corner pins are very crucial, local reinforcement near the corner may need to reduce the CPI stress. Center pins have relatively more flexibilities.

F. EMI Shielding

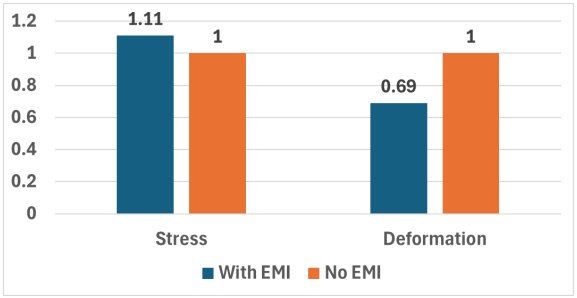

Fig. 20. Stress and deformation comparison for with/without EMI conditions.

Lastly, RF electromagnetic interference (EMI) shielding's impact on CPI stress in the package is studied. Where the module is compared with no EMI shielding and with EMI

on the top and four side faces of the package. As shown in Fig. 20, the EMI shielding reduces the magnitude of the deformation significantly. Meanwhile, it increased stress by about 11%. This is because EMI metal act similar as a structure stiffener surrounding the package which dampens out the deformation. And by limiting the deformation, which is crucial for stress reduction, it increases the stress levels.

III. Conclusion

Laminate metallization, die size, bump distribution are all shown as important factors for CPI stress in RF SiP package. RF shielding (either EMI or compartmental) can bring negative impact to CPI stress. In general, the addition of neighboring die seems helps lower CPI stress, but its proximity seems not very sensitive per our study. Chip CPI qualified in one package does not necessarily mean it can survive in the other package, factors like die to package edge distance need be taken into consideration as well. In double sided package, how does the top assembly affect the bottom CPI stress need to be studied case by case. And per the bump distribution pattern study, die corner are more sensitive to bump patterns as it usually carries the largest stress levels, and center pins have more flexibilities. Future work along this topic can be extended to cover more use cases on mold study as it showed difference to die attach conditions. When the mold exists, the shear effect caused by the CTE mismatch between die and laminate would couple with the tensile effect because of mold expansion and shrinking. High stress pins may exist in more inner part of the die if there is not enough bump density. And the ratio of the die/mold in a package may affect the total deformation and thus stress levels. Those topics would require further discussions which could not be covered here.

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References

[1] K. Dhandapani, B. Roggeman and D. Rae, “A Systematic Approach to the Reliability Characterization of System in Package (SiP), *International Symposium on Microelectronics*, 2018,

[2] P. Rajmane, K. Dhandapani, M. Schwarz and A. Syed, “Investigation of the Factors Affecting the Warpage Prediction of Multi-Chip Package”, *2021 IEEE 71st Electronic Components and Technology Conference (ECTC),* 2021, pp. 1514-1520.

[3] Z. Wu, C. Carey, S. Donavan, D. Hunt, P. Justison and T. Anemikos, “Chip-Package Interaction Challenges for Large Die Applications”, *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, 2018,

[4] W. Wang, D. Zhang, Y. Sun, D. Rae, L. Zhao and J. Zheng, “Study of Polyimide in Chip Package Interaction for Flip-Chip Cu-Pillar Packages”, *2018 IEEE 68th Electronic Components and Technology Conference (ECTC),* 2018,

[5] S. Han, D. Li, X. Feng, Y. Guan, Bo. Li and D. Li, “Chip-Package interaction stress analysis and optimization for a 14nm extreme low-k chip of FCCSP package”, *2022 23rd International Conference on Electronic Packaging Technology (ICEPT)*, 2022

[6] W. Yang, R. Budynas, and A. Sadegh, “*Roark's Formulas for Stress and Strain*”, 8th Edition. New York: McGraw-Hill, 2011.