Validating Reduced Order Model for Solder Reliability of Leadless Ceramic Chip Component during Temperature Cycling

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Abstract

Solder fatigue failure of electronics is a widespread problem, especially when the field conditions involve temperature excursions either as power cycling or diurnal cycling. The finite element method for predicting cycles to failure using damage indicators such as inelastic strain range or creep strain energy density is by far one of the most accurate methods to get detailed insights into solder reliability of electronic components. However, running detailed analysis for all the components on the board to get a realistic prediction is computationally heavy and to an extent impractical. As a first pass filter having a reliable reduced order model for predicting solder failure becomes essential. Engelmaier model is one of the most used reduced-order models for predicting solder fatigue failure of electronics due to temperature cycling. The model is based on inelastic strain as damage indicator which then gets used in Coffin-Manson power law for solder failure prediction. The prediction model is tuned based on experimental results from Wild to account for temperature and dwell time. In this paper, Blattau's model for ceramic chip components is evaluated against experimental data. The model calculates stress on the solder joint and uses Morrow's strain energy model for life prediction. The temperature range and dwell time effect are accounted by adjusting strain range due to global coefficient of thermal expansion (CTE) mismatch between the package and the printed circuit board (PCB) using Norris-Landzberg model. 2512 and 1206 chip resistors were subjected to thermal cycling at four temperature conditions: (1) -40ºC to 125ºC, (2) -15ºC to 125ºC, (3) 10ºC to 125ºC, and (4) 35ºC to 125ºC. Resistance was monitored during cycling and 50% increase in resistance was considered a complete failure. The model shows excellent fit with experimental data.

Key words: BGA, Solder Joint Reliability, 2512, Finite Element Analysis, Garafalo Model

I. Introduction

One of the key aspects in product designing is minimizing development lead time, which directly influences its time-to-market. The quicker the product is launched; the sooner it will gain its competitive edge. Electronics, being one of the most competitive business units, it is imperative for the engineers to accelerate the design phase without compromising on its quality to deliver reliable products. For solder reliability prediction in electronics, it is common practice to use analytical models as a first pass filter during the initial stages of development. Empirical models, such as those available in MIL-HDBK-217, also provide an avenue for quick reliability predictions. However, these are models based on field failure data that could be useful for predicting reliability of existing packages. When it comes to a new package or an existing package exposed to a new load condition, models based on handbook calculation may not be highly effective. In such situations, having a predictive model based on reliability physics is a far better tool to be equipped with than the models based on empirical observations.

Two of the most widely used models for making solder fatigue prediction has been Basquin [1] and Coffin-Manson [2], [3] for high cycle fatigue and low cycle fatigue failures respectively. Though the early application of the Coffin-Manson model was in predicting the life of structural elements of nuclear reactors, gas and steam turbines at elevated temperatures; many researchers have adopted the model for making solder fatigue prediction [4], [5].

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f'}\right)^{\frac{1}{c}} \quad (1)$$

where,

N_f , Number of cycles to failure
ε_f' , Ductility coefficient
$\Delta\gamma$, Plastic strain range
c , Ductility exponent

The model, however, does not account for cyclic frequency, solder temperature and stress relaxation effects which are inherent to thermal cycling events. Also, the model is based on plastic strain range, while the solder deformation mechanics are usually driven by creep behavior at elevated temperature. This makes assessing true cyclic plastic strain range difficult for solder [6]. Engelmaier [7] addressed these drawbacks and proposed a semi-empirical approach based on Coffin-Manson model to predict fatigue life of leadless chip carrier during power cycling. The model uses cyclic shear strain range evaluated using equation (2) with Coffin-Manson model to determine mean cycles to failure (50%) for near eutectic tin-lead solder.

$$\Delta\gamma = \frac{L}{\sqrt{2}h}\Delta(\alpha\Delta T)_{SS} \text{ x } 10^{-6} \quad (2)$$

In the above equation, L is the length of the ceramic chip carrier, h is the height of the solder joint and $\Delta(\alpha\Delta T)_{SS}$is the in-plane steady state thermal expansion mismatch between the substrate and the package. The ductility coefficient and exponent were then determined (equation (3) & (4)) from Wild test data [8] for tin-lead solder alloy.

$$2\varepsilon_f' \approx 0.65 \quad (3)$$

$$c = -0.442 - 6\text{x}10^{-4}\bar{T}_s + 1.74\text{x}10^{-2}\ln(1+f) \quad (4)$$

In the above equation, $\bar{T}_s$ is the mean cyclic solder joint temperature and f is the cyclic frequency. Engelmaier later modified equation (2) to address certain second order effects listed in [7] and rewrote the frequency effects in equation (4) in terms of dwell time as shown in (5) & (6) respectively.

$$\Delta\gamma = F\frac{d}{2h}\Delta(\alpha\Delta T) \quad (5)$$

$$c = -0.442 - 6\text{x}10^{-4}\bar{T}_s + 1.74\text{x}10^{-2}\ln\left(1+\frac{360}{t_D}\right) \quad (6)$$

'F' in equation (5) is an empirical factor accounting for the second order effects and d is the longest distance in the component between the solder joints. Although the model has been used across the industry, many authors have pointed out drawbacks with it. Preeti et al [9], gave an in-depth literature review discussing the articles that presented the deficiencies with Engelmaier model. Reimer [10], noted that the model does not contain any interconnect or board specific information making it difficult to evaluate any design study. Hillman [11], pointed out that Engelmaier approach may limit insights into fatigue behavior at colder temperatures, as Wild [8] data was characterized only for temperatures above room temperature. He further added that tests by Wild were in a frequency range between 4-300 cycles per hour which is higher than a typical thermal cycling frequency. Such variations may contribute to an inaccurate failure prediction. Clech et al. [12], [13] adapted Engelmaier's model and incorporated strain energy instead of strain range. Blattau [14] proposed a closed form analytical model based on strain energy by incorporating foundational stiffness between the copper pad and PCB to improve stress prediction on the joints. The model also accounts for temperature and dwell time effects by adjusting strain range due to differential thermal expansion between the package and the printed circuit board (PCB) using Norris-Landzberg model. In this paper, reliability prediction from the model is discussed and is compared against thermal cycling test data for 2512 and 1206 chip components.

II. Test Setup

Thermal cycling tests were conducted on 2512 and 1206 surface-mount chip resistors to evaluate their reliability under varying thermal stress conditions. The packages were mounted on a 1.6 mm thick FR-4 substrate using standard lead-free paste. The board was designed to accommodate 80 samples (40 samples per package type) as shown in Figure 1 and a total of two boards were evaluated per thermal load condition.

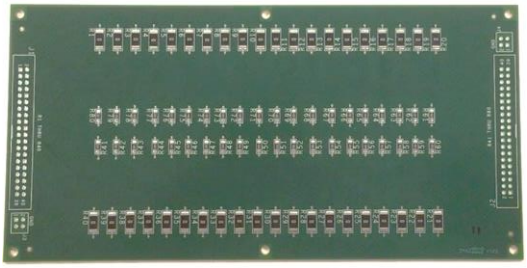

Figure 1: Test Coupon

Four distinct thermal cycling conditions with varying temperature ranges were used for the test. The thermal profiles evaluated are listed below.

- TC1: -40°C to +125°C, 10°C/min ramp, 15 min dwell
- TC2: -15°C to +125°C, 10°C/min ramp, 15 min dwell
- TC3: +10°C to +125°C, 10°C/min ramp, 15 min dwell
- TC4: +35°C to +125°C, 10°C/min ramp, 15 min dwell

All the packages were monitored for resistance and a complete failure of a package was categorized as 50% increase in its resistance. Chamber air temperature was monitored for thermal profiling and thermal cycle count calculation. Thermocouples were affixed to the center of the board to record board temperature to guarantee that the boards reached the set temperature at dwell. The boards were hung in a thermal chamber to replicate free warp conditions as shown in Figure 2.

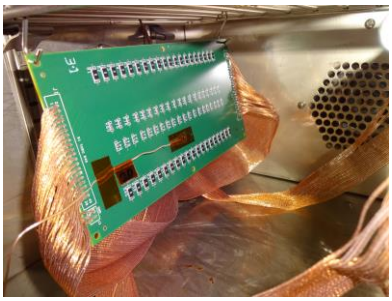

Figure 2:Test Set-up

Thermal profile tests were conducted to identify any cold spots in the chamber before running the life test. A sample of the measured temperature is shown in Figure 3 for thermal condition, TC1.

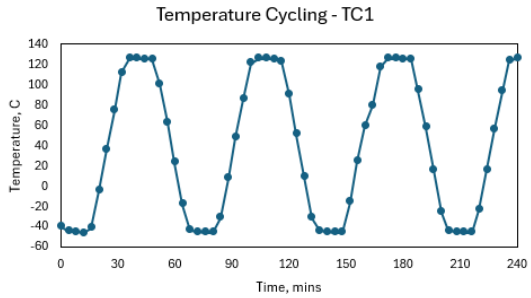

Figure 3: Test Profile: TC1

III. Test Results

All 2512 chip resistors failed across the four-temperature ranges. However, due to time constraint, testing of 1206 was stopped with minimal failure. Samples that did not show failure were suspended from Weibull analysis. All the failed packages were electrically characterized, and the results were plotted on a 2-parameter Weibull distribution chart for characteristic life as shown in Figure 4. Table 1 & Table 2 gives the characteristic life for all the four conditions for 2512 and 1206, respectively.

Table 1: Cycles to Failure, 2512

Temperature Condition	Beta	First Failure	Characteristic Life (63.2%)
TC1	4.47	395	709
TC2	4.34	481	911
TC3	3.94	642	1279
TC4	3.71	897	1830

Table 2 : Cycles to Failure, 1206

Temperature Condition	Beta	First Failure	Characteristic Life (63.2%)
TC1	4.95	1768	3825
TC2	3.71	2446	7158
TC3	5.47	2806	6557
TC4	6.57	4031	7017

The Weibull plots show that all failures had a beta greater than 3, which is characteristic of wear-out type failures. It was also clear that higher temperature ranges led to quicker failure due to increased shear loading of the solder. Cross sections of the failed samples, as shown in Figure 5 & Figure 6, showed typical crack trajectory for both 2512 as well as 1206. As the tests on 1206 resistor were halted due to time constraint, failure of only less than 20% of the samples were noted. However, the failed 1206 samples showed a consistent trend, except under condition TC2.

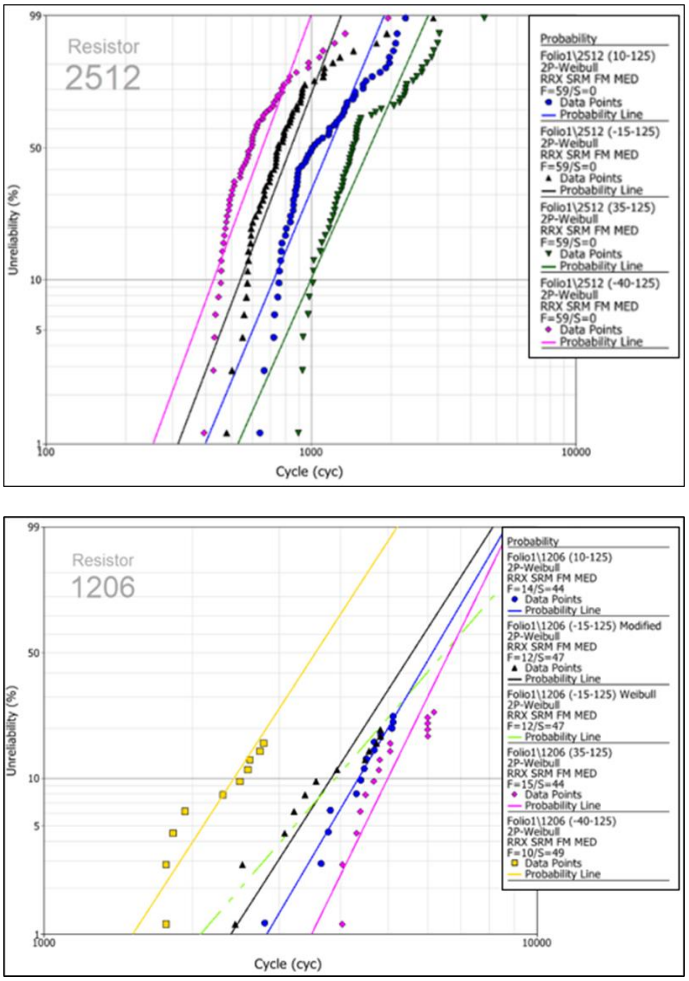

Figure 4: Weibull Plots, 2512 (top), 1206 (bottom)

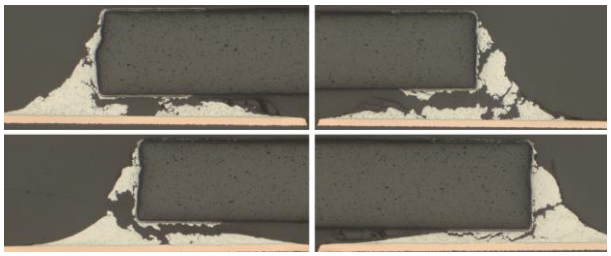

Figure 5: 2512 Cross Sections

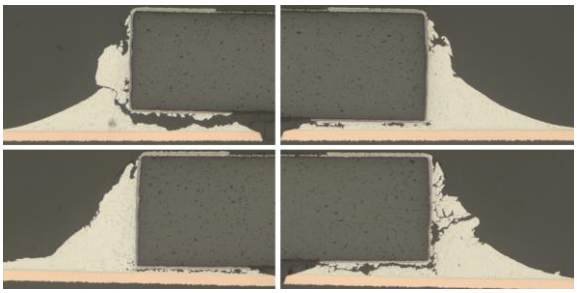

Figure 6: 1206 Cross Sections

At TC2, the Weibull slope was noted to be 3.7, while it was approximately 5 or higher for the other test conditions.

Although TC2 operated at a higher temperature range (ΔT = 140°C), its characteristic life was longer than that of TC3 (ΔT = 115°C) & TC4 (ΔT = 90°C). From the 1206 Weibull plot in Figure 4, we can see that the slope for TC2 was biased based on the failures occurring around 5000 cycles. With higher samples failing, the Weibull slope could have been better. Assuming a beta of 5 to match other test conditions, the characteristic life was found to be ~6000 cycles, which shows the expected trend. The black triangles in the Weibull plot for 1206 shows the data point for TC2. The black line shows the Weibull with the adjusted beta of 5 and the green dashed line indicates the Weibull without any adjustment. Comparison of all the test results were made with the predictions reduced order model, and the results are discussed in the following section.

IV. Prediction Model

Blattau's [14] solder fatigue model is a strain-energy based reduced order method based on Engelmaier's model. The approach determines shear stress available to drive the solder joint deformation during temperature cycling events based on effective stiffness of the system (surface mount chip component soldered to printed circuit board). The total strain on the solder is based on the global CTE mismatch between the PCB and the package. Temperature and dwell time effects are accounted by adjusting the determined strain based on Norris-Landzberg equation. Strain energy per thermal cycle is then found from solder stress and the adjusted strain. The calculated strain energy is finally used to determine the number of cycles to failure. For stiffness calculation, the structure of chip components on a printed circuit board as shown in Figure 7 is represented by combination of springs in series.

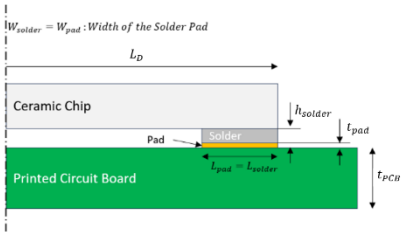

Figure 7: Chip Component on PCB Substrate

By displacement compatibility equation, the differential displacement due to thermal expansion of the system (PCB, package, and interconnect) is given by equation (7). PCB and package displacements (stiffness given by equation (9)) are assumed to be in tension, while the solder and copper pad are assumed to be in shear (equation (10)). Additionally, foundation stiffness equation is introduced representing the interfacial stiffness between the copper pad and the PCB. This term is given by the shear stiffness of a rigid square foundation on an elastic half-space [15]. The pad, the solder and the interfacial stiffness represents the interconnect system.

$$F = (\alpha_{PCB} - \alpha_{CC})\,\Delta T\, L_D k_{eff} \tag{7}$$

$$\frac{1}{k_{eff}} = \frac{1}{k_{PCB}} + \frac{1}{k_{CC}} + \frac{1}{k_i} \tag{8}$$

$$k_{PCB} = \frac{E_{PCB}A_{PCB}}{L_D}\ ;\ k_{CC} = \frac{E_{CC}A_{CC}}{L_D} \tag{9}$$

$$\frac{1}{k_i} = \frac{1}{\frac{G_{pad}A_{pad}}{t_{pad}}} + \frac{1}{\frac{G_{solder}A_{solder}}{h_{solder}}} + \frac{1}{\frac{9\,G_{PCB}W_{pad}/2}{2 - v_{PCB}}} \tag{10}$$

where,

α_{PCB} , Board CTE
α_{CC} , Chip component CTE
ΔT , Temperature range
L_D , Package half diagonal length
F , Shear force in the system
k_{eff} , Effective stiffness
k_{PCB} , PCB Axial stiffness
k_{CC} , Package Axial stiffness
k_i , Interconnect Shear stiffness
$G_{pad}, G_{solder}, G_{PCB}$, Shear moduli
v_{PCB} , PCB Poisson's ratio

Shear stress on the solder is determined from the solder area and the force determined from equation (7) as shown below.

$$\tau_s = \frac{F}{L_{solder}W_{solder}} \tag{11}$$

The total strain on the solder is calculated by differential thermal expansion of the PCB and the package. Inelastic strain is then found from total and elastic strain as shown in equation (12).

$$\Delta\gamma_{in} = (\alpha_{PCB} - \alpha_{CC})\,\Delta T\ -\ \tau_s/G_{solder} \tag{12}$$

The model assumes that the solder is fully stress relaxed and this inelastic strain is then adjusted to account for dwell time and temperature per Norris-Landzberg equation.

$$\Delta\gamma_{in}^{adj} = \Delta\gamma_{in}\left(\frac{t_F^{dwell}}{t_C}\right)^{0.136} e^{\frac{E_a}{k}\left(\frac{1}{T_C} - \frac{1}{T_F}\right)} \tag{13}$$

All the calculations are conducted for temperature range with respect to mean temperature, allowing for temperature dependent calculations at both the minimum and maximum temperature in the thermal profile as shown in equation (14) & (15). Strain energy is determined from stress and the adjusted strain; and life is calculated per Syed's approach as shown in equation (17).

$$\Delta T_{hot} = T_{max} - T_{mean}\ ;\ \Delta T_{cold} = T_{mean} - T_{min} \tag{14}$$

$$T_{mean} = \frac{T_{max} + T_{min}}{2} \tag{15}$$

$$\Delta W = \Delta W_{hot} + \Delta W_{cold} \tag{16}$$

$$N_f = (C\,\Delta W)^{-1} \tag{17}$$

T_F and t_F^{dwell} in equation (13) are the field condition temperature in kelvin and its corresponding dwell time in minutes. Other parameters such as t_C, critical dwell time,

E_a/k, activation energy over Boltzmann constant, T_C, critical temperature in kelvin are solder specific properties. C in equation (17) is solder specific strain energy coefficient. Figure 8 shows the comparison between cycles to failure (CTF) prediction between the reduced order model and experimental result. The dotted line in the plot represents an ideal prediction line. Any point lying on this line shows that the model predicted the same CTF as recorded from the experiment. If the point shifts below this line, it is representative of the model predicting a lower CTF than noted in experiment. Such a prediction represents conservative prediction by the model. Likewise, a point above the ideal line shows that the model overestimated the experimental CTF. Overall, the model prediction is within a 2x band limit.

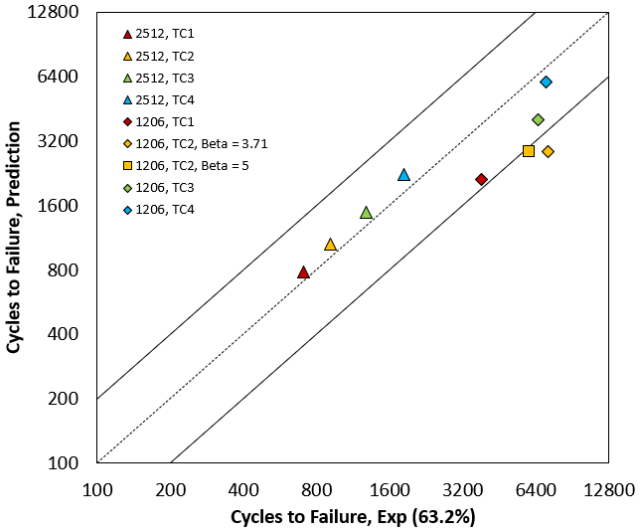

Figure 8: CTF comparison between Prediction and Experiment

Although the model shows good predictive capability, recognizing its limitations is important when interpreting the results. One of the drawbacks of the model is that it does not address system-level effects such as mirroring, mounting stresses, and interactions with adjacent components. Such a limitation is generally considered to be inherent in any analytical based modelling method. Additionally, the model assumes simplified solder geometries. Despite these limitations, the model still provides a reliable first-order approximation of solder joint behavior during thermal cycling events allowing engineers to identify potential risks, compare design alternatives quickly and guide early-stage decision making.

It should be noted that significant variability can be seen in thermal cycling tests of electronics, owing to manufacturing and testing variations. Datasets, even if identical, can produce two different responses during the accelerated tests. Maintaining solder joint quality requires tight controls around the solder prints and reflow profiles, which is difficult to achieve with test coupons due to the nature of low-volume production. In such a process, having variations in parameters like solder thickness, fillet size, as shown in Figure 9, void formation, and microstructural changes are natural and expected. Such variability within a dataset is generally quantified by the Weibull slope (β) which reflects the spread in the data. Therefore, a thorough knowledge of these variations is critical for establishing robust correlations between empirical observations and results from predictive models.

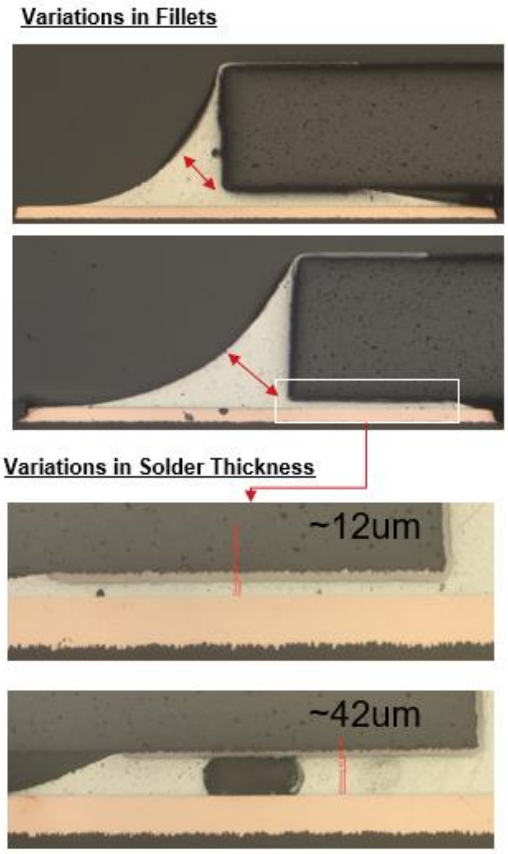

Figure 9: Fillet and Solder Thickness Variations

V. Conclusion

A closed form reduced order model for predicting solder reliability for chip component was discussed. The prediction from the model was compared with thermal cycling test data for 2512 and 1206 surface mount components. The tests were conducted at four distinct temperature ranges with a dwell time of 15 minutes at the two extreme temperatures. The model showed an excellent correlation with its predictions within a 2x band limit. Additionally, work is underway to extend the model to incorporate reverse termination packages and to capture crack propagation through the solder fillets. In parallel, a finite element-based framework is also being developed that provides improved computational efficiency while maintaining predictive accuracy, thereby enabling accelerated assessment of board-level reliability that incorporates system level effects.

VI. Acknowledgement

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