# BEOL Film Crack Mechanical Reliability Mitigation

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## Abstract

Flip chip (FC) packaging technology with copper bump interconnects has been widely used for highly integrated semiconductors to meet specific industrial requirements, contributing to dramatic body-downsizing, fine pitch, and improved electrical and thermal performance. However, FC copper bump interconnects are susceptible to mechanical reliability issues like interfacial delamination and inter-layer dielectric (ILD) passivation film cracks, while under reliability testing due to the marginality of fracture strength with the brittle mechanical behavior of BEOL film layers. For example, in a flip-chip chip-scale-package (FCCSP) device, especially one with copper bumps, an ILD crack was observed under temperature cycling (TC) loading. The crack was consistent with the new failure mode (i.e., the unique inter-layer mechanical interaction due to aggressive stacking), thus necessitating new design considerations for future devices and other multi-layer substrate package technologies. This paper comprehensively investigates this new failure mode, the root cause, and the innovative mitigation approach. This study developed the finite-element-analysis (FEA) based silicon (Si)-die level and package-level models to understand the root cause of ILD/passivation film crack risk. Additionally, the metal density transition impact on the top-metal layer (METTOP) to package metal interaction created a unique crack initiation and propagation situation to evaluate.

## Key words

Flip-Chip Package, BEOL Film, ILD Crack, Passivation Film Crack, Metal Density Transition, Image Processing, Finite Element Method.

## I. Introduction

The stacking of intermediate metal, inter-layer dielectric (ILD), and copper-bump-flip-chip (Cu bump FC) technology helps facilitate fine pitch routing to meet electrical and thermal performance. Figure 1 shows an example of the cross-sectioned image of Cu bump FC. However, the complex silicon back-end-of-line (BEOL) stacking and aggressive package design is prone to mechanical failures (e.g., interfacial delamination and ILD cracking) due to the marginality of fracture strength with the brittle mechanical behavior. In particular, ultra-low-k (ULK) films are liable to show poor fracture strength compared to other ILD films due to the high porosity of the ULK films. The porosity is an artifact of the doping process. Flip-chip (FC) technology representative flip-chip chip-size-package (FC-CSP) was developed in the semiconductor industry to meet the requirements of chip scale packaging efficiency and high-power applications. However, due to the drive for highly integrated devices, these film cracks were observed at unexpected locations. Figure 1 shows an example of an ILD crack post the temperature cycle loading (TC) for the FC-CSP device. Figure 2 shows the cross sectioned image of Cu bump FC. The dependability of utilizing an optimal combination of finite-element-analysis (FEA) based thermo-mechanical simulations and analysis coupled with extensive characterization is standard in the semiconductor industry

for understanding the failure mechanism and root causes from a mechanical point of view. In addition, this study developed an image processing technique with a homogenization model to reflect the local BEOL film layers on the silicon die (Si-die) to understand the regional stress distribution.

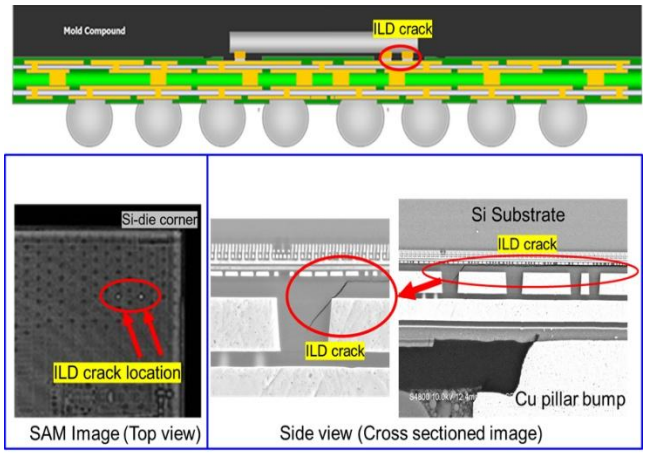


Figure 1: ILD crack location under the temperature cycle test , SAM image (left) and cross sectioned image (right)

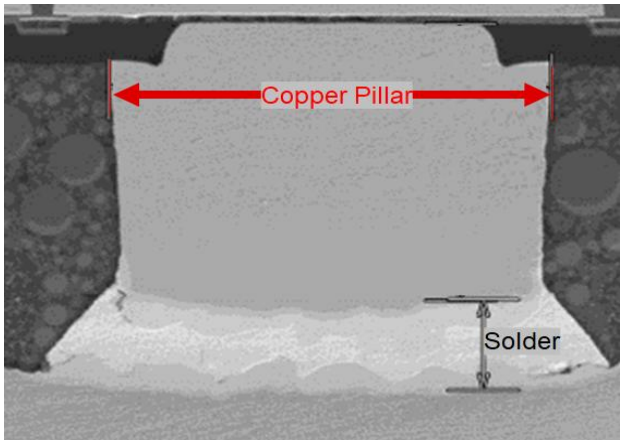


Figure 2: Cross sectioned image of Cu bump FC

## II. Material Formulation and Image Processing

An image processing technique was utilized to reflect the BEOL layers into the FEA-based thermo-mechanical simulations and help prevent the compression of FEA-based thermo-mechanical model sizes. First, the original BEOL layers and substrate drawing should be translated to the gray scale-based 8-bit color image files utilizing an image processing technique called light-intensity analysis (LIA), to reflect the local patterns into the FEA-based mechanical models. Figure 3 shows an example of the post-image processing technique with the light intensity values utilizing LIA. Light intensity values of 0 and 255 represent complete black and white colors, which means 100% copper trace and 0 copper trace regions, respectively. After LIA, the homogenization material model was utilized to reflect the regional BEOL layers and copper trace in the substrate using the following equation (1) [1] for the FEA-based thermo-mechanical simulation.

$$E_s = \Phi_{cu}E_{cu} + (1-\Phi_{cu})\,E_{BP},\ \alpha_s = \Phi_{cu}E_{BP} + (1-\Phi_{cu})\,\alpha_{BP} \quad (1)$$

Where $\varphi$ is the area fraction, $E$ is the Young's modulus, $\alpha$ is the CTE.

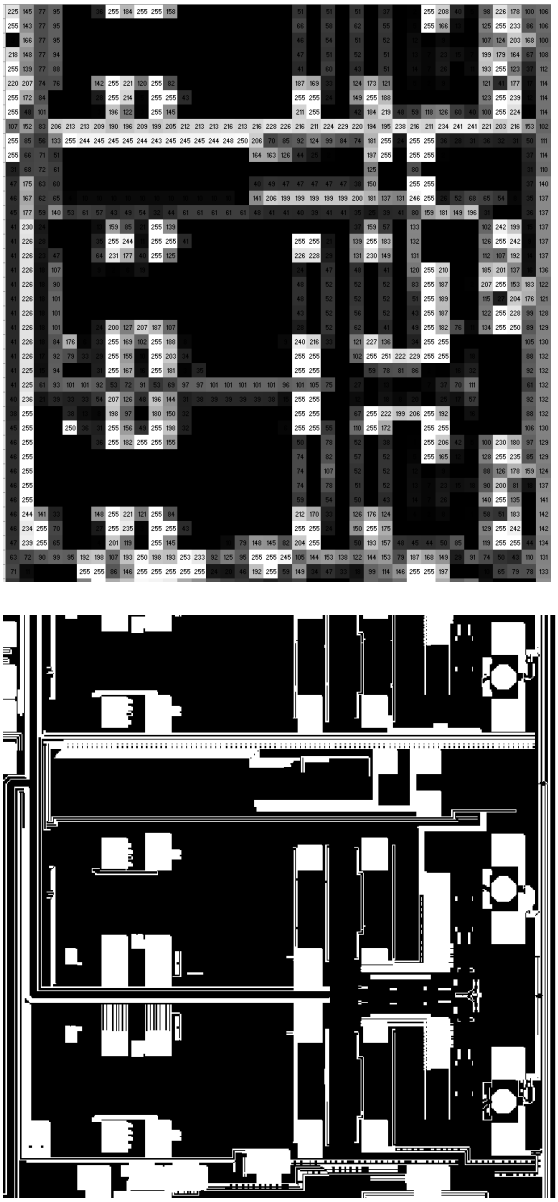

Figure 3: Example of metal density distribution post light-intensity-analysis (LIA)

For lead-free solder, rate-dependent plasticity, known as the Anand model based on the improvement of the Garofalo model, was characterized for this modeling technique [2]. This model has been widely used in the semiconductor industry to capture the rate-dependent plasticity of solder material under reliability testing [3]. Material constraints of Anand's viscoplastic constitutive model can be fitted to the strain rate and steady-state stress tests based on equations (2) and (3), and related strain hardening material parameters can be fitted based on stated equations (4) and (5). To estimate the remaining Anand's parameters, all the stress-strain data from the characterization is used to fit the following stress-strain relationship (6), [4], [5].

$$\frac{\mathrm{d}\varepsilon^p}{\mathrm{d}t} = A\exp\left(-\frac{Q}{RT}\right)\left[\sinh\left(\frac{\zeta\sigma}{s}\right)\right]^{1/m} \tag{2}$$

$$\sigma^* = \frac{\hat{s}}{\zeta}\left\{\frac{1}{A}\frac{\mathrm{d}\varepsilon^p}{\mathrm{d}t}\exp\left(\frac{Q}{RT}\right)\right\}^n \sinh^{-1}\left[\left\{\frac{1}{A}\frac{\mathrm{d}\varepsilon^p}{\mathrm{d}t}\exp\left(\frac{Q}{RT}\right)\right\}^m\right] \tag{3}$$

$$\frac{\mathrm{d}\sigma}{\mathrm{d}\varepsilon^p} = ch_0\left(1-\frac{\sigma}{\sigma^*}\right)^a, \qquad \sigma = cs \ , \ \sigma^* = cs^* \tag{4}$$

$$c \equiv \frac{1}{\zeta}\sinh^{-1}\left[\left\{\frac{1}{A}\frac{\mathrm{d}\varepsilon^p}{\mathrm{d}t}\exp\left(\frac{Q}{RT}\right)\right\}^m\right] \tag{5}$$

$$\sigma = \sigma^* - [(\sigma^* - cs_0)^{(1-a)} + (a-1)\{(ch_0)(\sigma^*)^{-a}\}\varepsilon_p]^{1/(1-a)} \tag{6}$$

Where $s_0$ is initial deformation resistance, Q/R is activation energy / Boltzmann's constant, A is the pre-exponential factor, ξ is the multiplier of stress, m is strain rate sensitivity of stress, $h_0$ is hardening/softening constant, Ŝ is the coefficient for deformation resistance saturation, n is strain rate sensitivity of saturation, a is strain rate sensitivity of hardening or softening. Anand parameters of solder bumps are listed in TABLE I.

TABLE I. ANAND PARAMETERS OF SOLDER MATERIAL FOR FC BUMP

| | | |
|---|---|---|
| Initial Deformation Resistance | $s_0$ (MPa) | 3.18E+06 |
| Activation energy/Boltzmann's constant | Q/R (/K) | 5.92E+03 |
| Pre-exponential factor | A ($s^{-1}$) | 3.50E-02 |
| Multiplier of stress | ξ | 1.51E+00 |
| Strain rate sensitivity of stress | m | 3.68E-01 |
| hardening/softening constant | $h_0$(MPa) | 5.08E+10 |
| coefficient for deformation resistance saturation | Ŝ (MPa) | 7.93E+06 |
| strain rate sensitivity of saturation | n | 2.56E-02 |
| strain rate sensitivity of hardening or softening | a | 2.67E+00 |

In addition, the thermomechanical properties of organic material representative of mold compound and substrate materials are sensitive to temperature and strain rate. These are considered to be thermo-rheologically simple viscoelastic materials. The generalized Maxwell model-based viscoelastic behavior was used to input parameters to capture the rate-dependent elastic behavior. The viscoelastic behavior of the generalized Maxwell model kth element can be obtained, and total stress is given by summing the solutions of (8) up to k=n. The parameters in the equation below are calculated from the dynamic viscoelastic experiment. The experiment used the dynamic material response by evaluating dynamic mechanical analysis (DMA) with frequency/temperature sweeps. This analysis was conducted to estimate the rate-dependent elastic properties with the Prony series [6], [7], thus a strain was given,

$$\frac{d\varepsilon_k}{dt} = \frac{1}{G_k}\frac{d\sigma_k}{dt} + \frac{\sigma_k}{\eta_k} \tag{7}$$

$$\sigma = \varepsilon_0 G(t) = \varepsilon_0 G_\infty + \varepsilon_0 \sum_{k=1}^{n} G_k exp(-t/\tau_k) \tag{8}$$

$$\varepsilon = \varepsilon_0 e^{i\omega t} \tag{9}$$

$$\sigma(t) = \left\{G_\infty \varepsilon_0 + \sum_{k=1}^{n} G_k \varepsilon_0 \frac{i\omega\tau_k}{1+i\omega\tau_k}\right\}\exp(i\omega t) \tag{10}$$

$$G'(\omega) = G_\infty + \sum_{k=1}^{n} G_k \frac{\omega^2 {\tau_k}^2}{1+\omega^2 {\tau_k}^2} \tag{11}$$

$$G''(\omega) = \sum_{k=1}^{n} G_k \frac{\omega\tau_k}{1+\omega^2 {\tau_k}^2} \tag{12}$$

where $G'(\omega)$ is dynamic storage elastic modulus, and $G''(\omega)$ is dynamic loss elastic modulus. Frequency dispersion of specific temperatures is given by using the time-temperature-superposition (TTS) to create the rate-dependent properties at the frequency or time domain from the experimental results of G∞, Gk, and τk by using the least square method. In ANSYS, G∞ was automatically calculated from other input parameters. TABLE II lists the viscoelastic parameters for the substrate at room temperature with the 15 Prony series based on the DMA test result. Fig.4 shows an example of a rate-dependent property post-TTS from the DMA data, called master curve, for a mold

compound to estimate an appropriate generalized Maxwell model-based viscoelastic parameter with different Prony series. At least 15 Prony numbers would be necessary to obtain a smooth master curve [8]. TABLE II lists the example of the generalized Maxwell model-based viscoelastic parameter for the substrate.

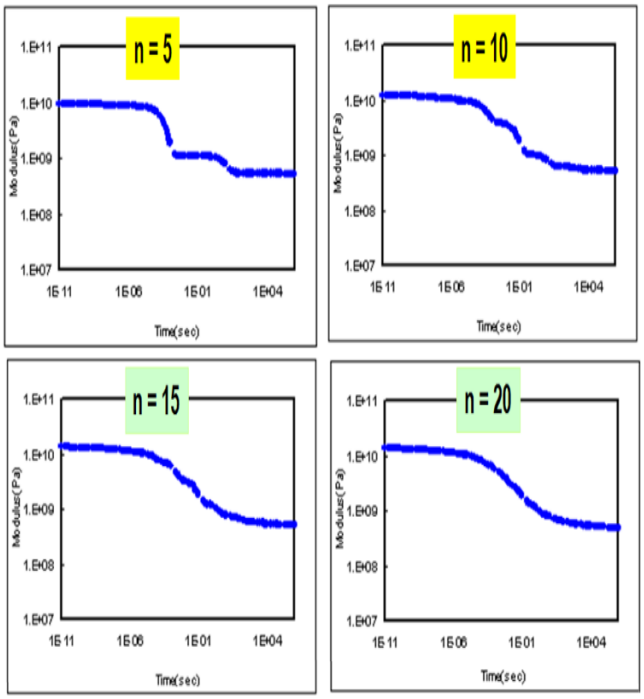


Figure 4. Estimation of generalized Maxwell model based viscoelastic parameters with different Prony series

TABLE II. THE GENERALIZED MAXWELL MODEL-BASED VISCOELASTIC PARAMETERS OF SUBSTRATE

| | k=1 | k=2 | k=3 | k=4 | k=5 |
|---|---|---|---|---|---|
| $G_k$ | 3.60E-02 | 1.47E-02 | 2.18E-02 | 2.84E-02 | 3.22E-02 |
| $\tau_k$ | 4.27E-03 | 5.33E-02 | 6.64E-01 | 8.28E+00 | 1.03E+02 |
| | k=6 | k=7 | k=8 | k=9 | k=10 |
| $G_k$ | 4.75E-02 | 6.05E-02 | 4.81E-02 | 5.73E-02 | 5.94E-02 |
| $\tau_k$ | 1.29E+03 | 1.60E+04 | 2.00E+05 | 2.49E+06 | 3.11E+07 |
| | k=11 | k=12 | k=13 | k=14 | k=15 |
| $G_k$ | 5.14E-02 | 3.36E-02 | 2.24E-02 | 9.99E-03 | 2.38E-02 |
| $\tau_k$ | 3.88E+08 | 4.83E+09 | 6.03E+10 | 7.51E+11 | 9.37E+12 |

## III. SIMULATIONS AND MODELING

FEA-based thermo-mechanical simulations were performed to understand the root cause of the stress distribution at the local regions attributed to the ILD crack risk. Figure 5 shows the metal density distribution of BEOL of the metal top layer and indicates the ILD crack location at the top view post temperature cycle (TC) test. The ILD crack was observed in area A under the Cu bump, and the exact failure location did not indicate the corner most bump. This image is divided into four regions (area A, B, C, D) and confirmed a vast metal density transition at area A, which observed an ILD crack post-TC. For areas A, C, and D, the high-low-high metal density transition was observed at the Si-die corner regions. Area A especially has a pronounced tendency to transition to this metal density. On the other hand, area B has the opposite metal density transition, low-high-low. Figure6 shows the minimum distance between the metal density transition, with the lowest number at area A and the highest at Area B, to understand the root cause of this ILD crack risk. Figure7 shows the Cu bump density of the entire Si die. Areas A and B have lower bump densities than areas C and D. To understand more details and root causes for this ILD crack risk, two kinds of FEA-based thermo-mechanical simulation were performed to clarify the individual impact for the ILD crack risk, called die-level and package-level models. The die-level model was performed to understand the effects of the BEOL film patterns, utilizing the combination of image processing technique and homogenization material model. The package-level model was also performed to understand the package-level geometry and material BOM set effect (e.g., FC bump layout, substrate material properties, Si die dimensions, etc.) The FEA-based thermo-mechanical simulation calculates the elastic strain energy density in ANSYS as a failure-sensitive parameter (FSP) to evaluate ILD crack risk. Figure8 shows the definition of the FSP, derived based on the combination of die-level and package-level models, which extracted the strain energy density of the ILD layer where the crack is encountered under the TC loading. FEA-based thermo-mechanical simulation results utilizing this FSP are consistent with the failure mode trend and location. The study also performed a solder bump type FC model to compare the ILD crack risk with the Cu bump FC.

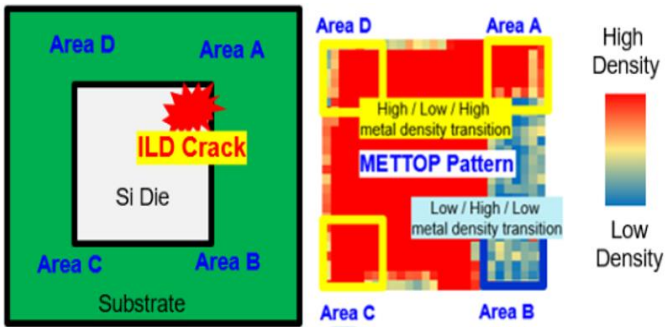


Figure 5. Failure location of ILD crack and metal density of top metal layer

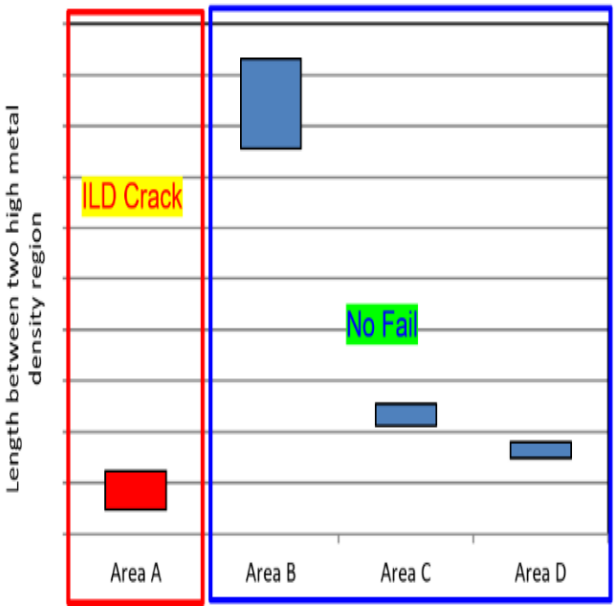


Figure 6. The minimum distance at the metal density transition regions for the top metal layer

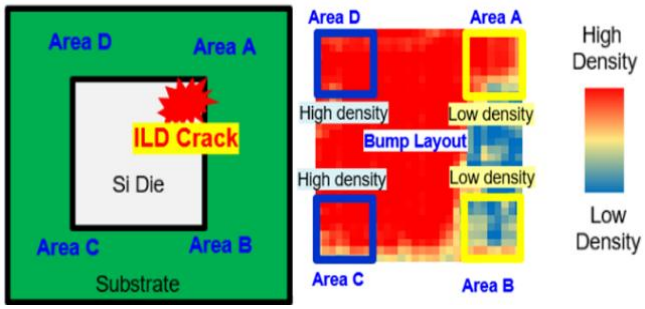


Figure 7. Failure location of ILD crack and Cu bump density of the entire die

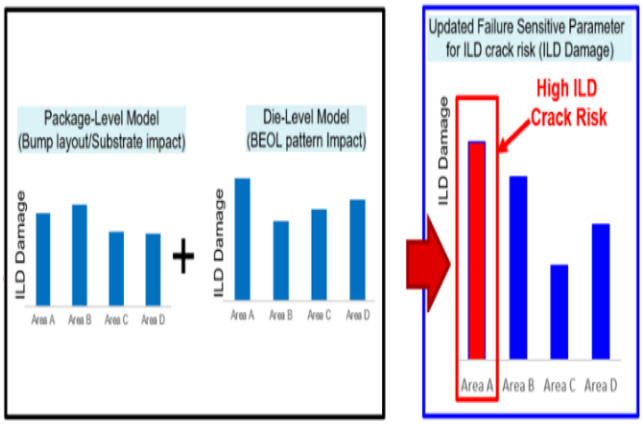


Figure 8. The failure-sensitive-parameter (FSP) to evaluate ILD crack risk

## IV. Interfacial Crack / Delamination Evaluation Between Dissimilar Materials

Stress singularity associated with oscillation at the tip of interfacial cracks/delamination between dissimilar materials can be seen (13) and (14) [9]. Figure 9 shows the coordinate system at the tip of the interfacial crack/delamination between dissimilar materials.

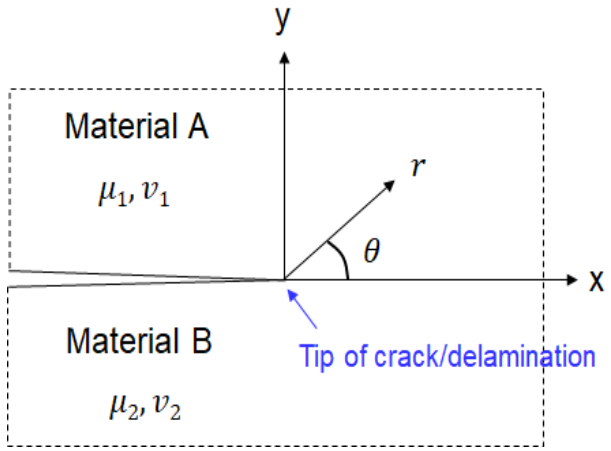


Figure 9. Coordinate system at the tip of the interfacial crack/delamination

$$\sigma_y + i\tau_{xy} = \frac{K_1 + iK_2}{\sqrt{2\pi r}}\left(\frac{r}{l}\right)^{i\varepsilon} \tag{13}$$

$$\delta_y + i\delta_x = \frac{K_1 + iK_2}{2(1+2i\varepsilon)\cosh(\varepsilon\pi)}\left[\frac{k_1+1}{\mu_1} + \frac{k_2+1}{\mu_2}\right]\sqrt{\frac{r}{2\pi}}\left(\frac{r}{l}\right)^{i\varepsilon} \tag{14}$$

$$\varepsilon = \frac{1}{2}\ln\left[\left(\frac{k_1}{\mu_1}+\frac{1}{\mu_2}\right)\Big/\left(\frac{k_2}{\mu_2}+\frac{1}{\mu_1}\right)\right] \tag{15}$$

$$C = 2\cosh(\varepsilon\pi)\Big/\left[\left(\frac{k_1+1}{\mu_1}+\frac{k2+1}{\mu_2}\right)\right] \tag{16}$$

$$Q = \varepsilon\ln\left(\frac{r}{l}\right) \tag{17}$$

$$K_1 = C\lim_{r\to 0}[\delta_y(cosQ + 2\varepsilon\ sinQ) + \delta_x(sinQ - 2\varepsilon\ cosQ]/\sqrt{r/2\pi} \tag{18}$$

$$K_2 = C \lim_{r\to 0}[\delta_x(cosQ + 2\varepsilon\, sinQ) - \delta_y(sinQ - 2\varepsilon\, cosQ]/\sqrt{r/2\pi} \quad (19)$$

$$G = \frac{1}{16cosh^2(\varepsilon\pi)}\left[\frac{k_1+1}{\mu_1} + \frac{k_2+1}{\mu_2}\right](K_1{}^2 + K_2{}^2) \quad (20)$$

Where $\mu_j$ and $\upsilon_j$ are the shear modulus and Poisson's ratio. Young's modulus can be estimated by $E_j$=2(1+$\upsilon_j$) $\mu_j$. $\sigma_y$ and $\tau_{xy}$ are the normal stress component and shear stress, $\delta_x$ and $\delta_y$ are the relative displacements.

$k_j$ = 3-4 $\upsilon_j$ for plane strain. ε is the strength of the oscillatory singularity of the stresses and displacements. The bimetal parameter $r$ is the distance from the tip of delamination and $l$ is the characteristic length. Stress intensity factors $K_1$ and $K_2$ can be calculated using the equations of (18) and (19). Energy release rate G was utilized to evaluate the ILD crack risk as a failure sensitive parameter (FSP) to evaluate the ILD crack risk, which is calculated by the stress intensity factors, $K_1$ and $K_2$ based on the displacement interpolation method described (20). Figure 10 shows an example of FEA-based thermo-mechanical models between cu and solder bump FC utilizing the local modeling technique after evaluating the global modeling technique, shown in figure 8.

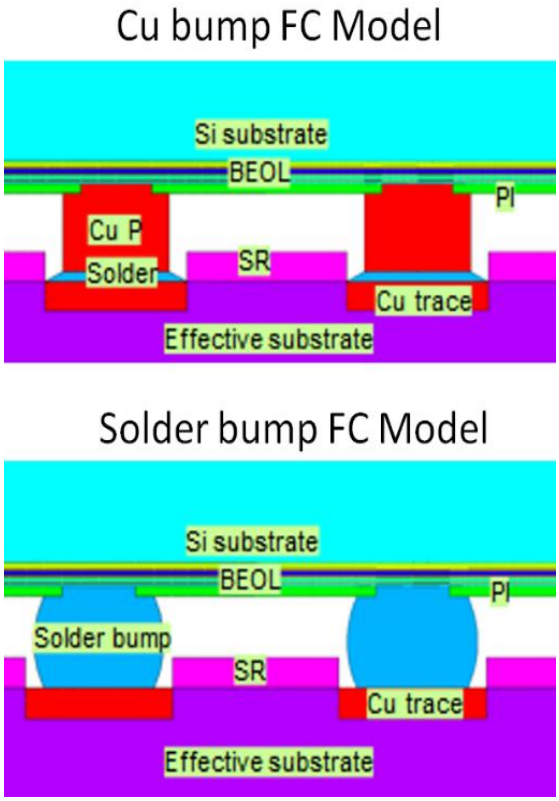


Figure 10. Example of Cu-bump and Solder-bump flip-chip (FC) model

## IV. Description of TC Test Vehicle

As depicted in Figure 1, the package platform type investigated in the study was an FC-CSP. The outlines of this package are as follows:

- 14x14mm body size FC-CSP
- 4ML (1/2/1 build-up stack) with 200um cored substrate

Five test vehicles were evaluated based on the FEA-based thermo-mechanical simulation results. Table III lists the details and differences of the test vehicles (TV). The main differences are top metal (METTOP) thickness, substrate BOM set, and metal density transition, which directly impact the coefficient of thermal expansion (CTE). TV2 was built to evaluate the impact of the metal density transition, which means filling the metal in the high metal density transition region partially at area A, where the ILD crack was observed post-TC. TV3 was built to evaluate the substrate CTE impact on the ILD crack risk. The relative differences in temperature-dependent CTE between reference and low CTE substrate utilizing thermal-mechanical-analysis (TMA) are listed in table IV. The lone difference between TV4 and TV5 is the METTOP thickness on the Si die and solder bump FC, respectively, compared to TV1.

TABLE III. Evaluated Test Vehicle

| Test vehicle | METTOP thickness | Substrate BOM set | Metal density transition | FC Bump Type |
|---|---|---|---|---|
| TV1 | Refrence | Refrence | Refrence | Cu Pillar |
| TV2 | Refrence | Refrence | New (filled metal) | Cu Pillar |
| TV3 | Refrence | Low CTE | New (filled metal) | Cu Pillar |
| TV4 | 1.4x | Refrence | New (filled metal) | Cu Pillar |
| TV5 | Refrence | Refrence | New (filled metal) | Solder Bump |

TABLE IV. Relative Comparison of CTE between Reference and Low-CTE Substratee

| | CTE with TMA | | | | |
|---|---|---|---|---|---|
| | 0-50°C | 50-100°C | 100-150°C | 150-200°C | 200-250°C |
| Reference substrate | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Low CTE substrate | 0.85 | 0.87 | 0.93 | 0.83 | 0.99 |

| | Modulus with DMA | | | | |
|---|---|---|---|---|---|
| | 0-50°C | 50-100°C | 100-150°C | 150-200°C | 200-250°C |
| Reference substrate | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Low CTE substrate | 1.07 | 1.06 | 1.05 | 1.06 | 1.14 |

## V. Empirical Test and Simulation Result

Table V lists the empirical test results with a failure rate under the TC loading and FEA-based thermo-mechanical simulation results, which extracted FSP relative to the evaluated ILD crack risk between the five test vehicles. Metal density transition, low CTE substrate, thicker metal of the top layer, and solder bump FC improve the ILD crack risk. The low CTE substrate and thicker metal of the top layer were the critical parameters to help reduce the ILD crack risk. In addition, FEA-based thermo-mechanical simulation indicated a similar trend to these empirical test results, and thermo-mechanical simulation expects that the combination of the thicker METTOP and low CTE substrate mitigates the ILD crack risk drastically. The risk level from using the low CTE material and thicker top layer metal would be similar to switching to solder bump type FC devices. This result helps the development of future devices while keeping a fine pitch for the 1st level of interconnection.

TABLE V. Empirical Test Result under the TC Loading

| Test vehicle | METTOP thickness | Substrate BOM set | Metal density transition | FC Bump Type | TC Test Result | FSP (Ratio) |
|---|---|---|---|---|---|---|
| TV1 | Refrence | Refrence | Refrence | Cu Pillar | Fail (6/80) | 1.00 |
| TV2 | Refrence | Refrence | New (filled metal) | Cu Pillar | Fail (3/80) | 0.94 |
| TV3 | Refrence | Low CTE | New (filled metal) | Cu Pillar | Passed | 0.70 |
| TV4 | 1.4x | Refrence | New (filled metal) | Cu Pillar | Passed | 0.92 |
| TV5 | Refrence | Refrence | New (filled metal) | Solder Bump | Passed | 0.51 |

## VI. Passivation Film Crack Evaluation

Based on the preliminary study regarding the ILD crack risk mitigation, although a thicker METTOP helps mitigate ILD crack risk, other failure modes are expected to be generated due to the intricate shape of the BEOL films caused by the thick METTOP. This study demonstrates and focuses on the passivation film crack risk with different METTOP thickness, metal spacing, and passivation slope angles. Utilizing a design of experiment (DOE) approach, feasibility of the ranges were defined by performing FEA-based thermo-mechanical modeling to clarify the contribution factor. Figure 11 shows an example of the passivation film crack risk model, stress contour map, and stress vector analysis. Figures 12 and 13 show the factorial estimation and contribution ratio from the DOE analysis. According to the contribution ratio of the individual and interaction factors, these three factors affect the passivation film crack risk. Since the passivation films are well-known as a brittle material, the first principal stress was used as an FSP to evaluate the passivation film crack risk.

TABLE V. Material properties for the Passivation film and Si substrate

| | Modulus (GPA) | CTE (ppm/C) |
|---|---|---|
| Si | 131 | 2.61 |
| Passivation film 1 | 166 | 1.4 |
| Passivation film 2 | 140 | 1.6 |

TABLE VI. DOE range for METTOP thickness, Metal Spacing, Passivation film slope angle

| | DOE Range | | |
|---|---|---|---|
| METTOP thickness | X1.0 | X1.4 | X2.2 |
| Metal Spacing | X1.0 | X1.7 | X2.5 |
| Passivation film slope angle | X0.9 | X1.0 | X1.1 |

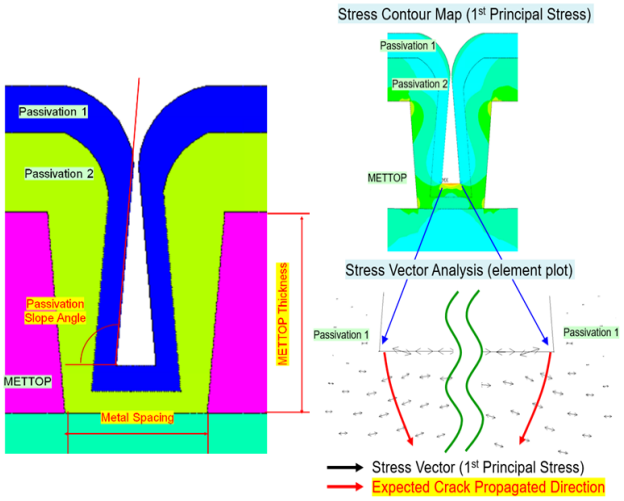


Figure 11. Example of passivation flm crack model and stress contour map and stress vector analysis.

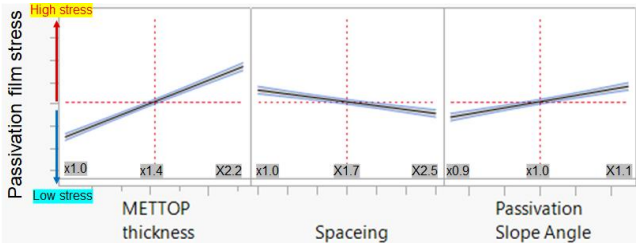


Figure 12. Factorial estimation from the DOE analysis

| Source | DF | Sum of Squares | Mean Square | F Ratio | Prob > F | Contribution Ratio |
|---|---|---|---|---|---|---|
| METTOP thickness | 1 | 470795 | 470795 | 640 | <.0001* | 67.73 |
| Spacing | 1 | 48967 | 48967 | 67 | <.0001* | 6.95 |
| Passivation Slope Angle | 1 | 84802 | 84802 | 115 | <.0001* | 12.11 |
| METTOP thickness*Spacing | 1 | 71957 | 71957 | 98 | <.0001* | 10.26 |
| METTOP thickness*Passivation Slope Angle | 1 | 592 | 592 | 1 | 0.3806 | . |
| Spacing*Passivation Slope Angle | 1 | 2028 | 2028 | 3 | 0.1125 | 0.19 |
| Model | 6 | 664504 | 110751 | 150 | <.0001* | . |
| Error | 20 | 14720 | 736 | | | 2.76 |

Figure 13. Contribution ratio from the DOE analysis.

## VII. Empirical Test of Passivation Film Crack

Table VII lists the empirical test results between five test vehicles with different METTOP thickness and metal spacing. These empirical test results show that the wider metal spacing is expected to help improve the passivation film crack risk despite the thick METTOP. These empirical test trends are consistent with the FEA-based thermo-mechanical modeling result with DOE analysis. In addition, the cross-sectional image of the passivation film crack for TV A is shown in figure 14. Since this crack growth direction is consistent with the FEA-based thermo-mechanical modeling result based on the vector analysis, these thermo-mechanical modeling results are reliable compared to the empirical test results. Although the passivation slope angle was not evaluated due to the major change in manufacturing process parameters for these five test vehicles, the passivation slope angle is also expected to affect the passivation film crack risk. This combination helps the development of future devices while keeping lower ILD and passivation film crack risks with enough margins.

TABLE VII. Empirical Test Result under the TC TestThe TC Test

| Test Vehicle | METTOP thickness | Metal spacing | Test Result | FSP (Ratio) |
|---|---|---|---|---|
| TV A | x2.2 | X1.00 | observed crack | 1.00 |
| TV B | x2.2 | X1.75 | no crack | 0.79 |
| TV C | x2.2 | X2.50 | no crack | 0.74 |
| TV D | x1.4 | X1.00 | no crack | 0.61 |
| TV E | x1.0 | X1.00 | no crack | 0.33 |

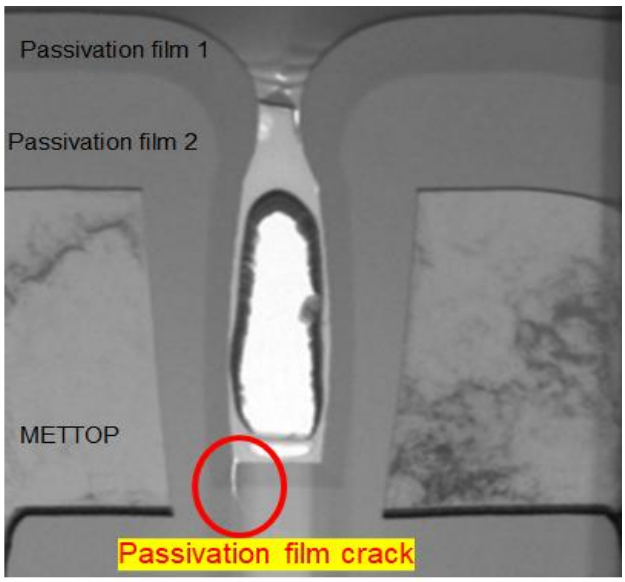


Figure 14. Example of Passivation film crack

## VIII. Conclusion

Based on the combination of the empirical tests and FEA-based thermo-mechanical simulation results, the investigation revealed the root causes of this ILD crack risk under the TC loading. An image processing technique was developed to reflect the local BEOL layer patterns into the FEA-based thermo-mechanical simulations. This approach helps prevent the compression of FEA-based thermo-mechanical model sizes and provides highly accurate results. In the study, the metal density transition, the thicker top metal layer, and the low CTE substrate are the critical parameters to mitigate ILD crack risk. These findings allow for a fine pitch interconnect without changing the FC type and show the guideline principle for successfully downsizing future FC-CSP platform devices. In addition to utilizing a thicker METTOP, combining the wider metal spacing and the lower passivation slope angle is expected to help reduce the ILD and passivation film crack risks with enough margin.

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