Modeling Analysis of Passivation and TEOS Cracking in BEOL Metal Trace Design

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Abstract

As flip chip packaging technologies advance, silicon-level failure highlights the importance for robust design evaluation methodologies early in the development cycle. To support this need, we have developed a multi-scale finite element analysis (FEA) framework that includes both 3D and 2D multi-scale simulations, to capture stress distributions at critical failure locations. These models demonstrated comparable stress trends, validating their effectiveness in identifying high-risk regions. To further investigate micro-crack propagation risks at submicron scales, a 2D fracture mechanics model is introduced. This model enables detailed analysis of how key design parameters, such as aluminum pad (AP) spacing and BEOL metal trace spacing, influence failure susceptibility. Notably, these parameters exhibit opposing effects on two different failure modes, underscoring the importance of trade-off analysis. This paper presents a simulation-driven framework for assessing chip-level failure risks during the early stages of silicon-level design. Rather than prescribing specific design solutions, this study emphasizes the use of developed modeling framework to guide early-stage design exploration on silicon-level failure risk. The modeling framework provides a foundation for integrating modeling-driven insights into silicon-level design and process development, ensuring robust chip design to avoid failures downstream in packages.

Key words

Finite Element Analysis (FEA), Modeling, Passivation, TEOS, BEOL, Cracking

I. Introduction

As semiconductor technology nodes continue to advance, back-end-of-line (BEOL) integrity has become an increasingly critical concern in flip chip packaging. Common failure modes include low-k (LK) or extreme low-k (ELK) delamination due to thermal mismatch between chip and package during chip attach or after assembly and have been widely studied [1][2]. In addition, under-bump metallization (UBM) and aluminum pad (AP) delamination are known to occur under thermal cycling conditions [3]. However, cracking at the die passivation and tetraethyl orthosilicate (TEOS) layers may also occur due to additional failure mechanisms even in the absence of common failure modes, and may propagate into BEOL metal layers, ultimately leading to electrical failure at the chip level. As such, mitigating these cracking risks is essential for achieving robust chip design.

Despite their significance, there is limited fundamental research on die passivation and TEOS cracking. Experimental investigations into these failure modes are often constrained by the high cost and long cycle times associated with wafer fabrication. To address this gap, we present a modeling-based approach to characterize two BEOL failure modes: cracking at the silicon nitride/silicon oxide interface, and cracking within the TEOS layer.

In this study, we develop a suite of finite element analysis (FEA) models to understand two failure modes to support early-stage design analysis. First, a 3D multi-scale global-submodel approach is used to evaluate stress distribution at critical failure locations. To improve computational efficiency while maintaining predictive accuracy, a corresponding 2D multi-scale model is developed and validated against the 3D results. Comparable stress distribution predication is achieved between 3D model and 2D model. To better quantify the cracking risk, a fracture mechanics model is developed to assess micro-crack propagation risks at submicron scales. Since the 3D model and 2D model show comparable stress prediction, a 2D

fracture mechanics model is introduced for modeling efficiency.

This modeling framework enables quantitative evaluation of key design variables, such as AP spacing and BEOL metal trace spacing, and their influence on cracking susceptibility. The simulation results reveal that these parameters affect the two failure modes in opposite effects ways, highlighting the need for trade-off analysis. Rather than prescribing specific design solutions, this study emphasizes the value of simulation framework in guiding early design exploration and identifying potential failure risks. The modeling framework presented here provides a foundation for integrating modeling-driven insights into silicon-level design, ensuring robust chip design to avoid failure risks downstream in packages

II. FEA Model Development

To investigate the mechanical integrity of BEOL structures in flip chip packages, a multi-scale finite element analysis (FEA) framework was developed to simulate test packages. The modeling approach was designed to evaluate stress distributions and fracture risks associated with two failure modes: (1) cracking at the silicon nitride/silicon oxide interface, and (2) cracking within the TEOS dielectric layer. The methodology integrates global-to-local stress modeling with fracture mechanics to enable both macro- and micro-scale simulation analysis.

A. Three-Dimensional (3D) Multi-scale Model

A 3D global-submodeling technique was first employed to capture the overall thermo-mechanical response of the package during temperature loading. The global model includes key package components such as the die, molding compound, and substrate, and simulates the temperature loading profiles representative of reliability tests. A submodel was constructed around the critical BEOL region which is susceptible to cracking to simulate localized stress distribution.

Given the significant scale disparity between the package-level geometry (millimeter scale) and the BEOL features (sub-micrometer scale), a multi-scale modeling approach was developed. As illustrated in Fig. 1, the global model uses a coarse mesh at the package level, which transitions smoothly to a fine mesh in the BEOL submodel. The mesh size varies from hundreds of micrometers near the package edge to sub-micrometer resolution in the vicinity of the aluminum pad (AP) and thick top metal layers. This meshing strategy ensures accurate stress resolution at critical interfaces while maintaining computational efficiency.

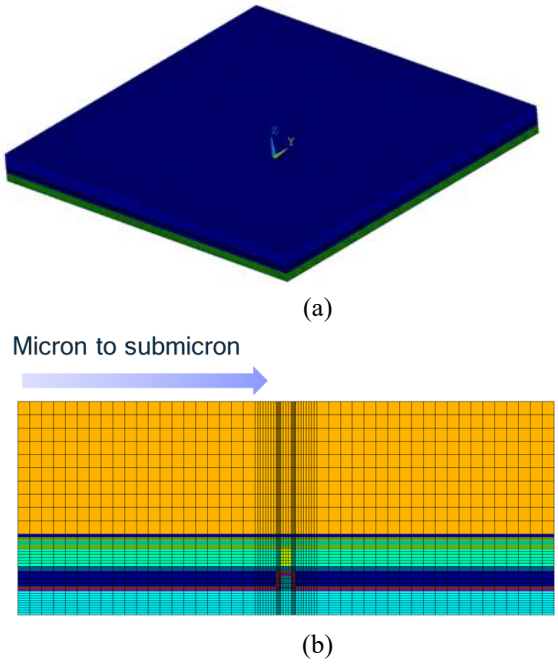


Fig. 1 (a) 3D Multi-scale FEA model and (b) local mesh

B. Two-Dimensional (2D) Multi-scale Model

To improve computational efficiency while maintaining accuracy, a 2D multi-scale model was also developed as shown in Fig.2. This model simplifies the geometry while preserving the essential material stack-up and boundary conditions. Comparative analysis between the 3D and 2D models showed good agreement in stress predictions at the failure locations, validating the use of the 2D model for this study.

A fracture mechanics model was then developed to analyze the material fracture propagation risk where stress singularity could become an issue in extreme small-scale structures. The fracture model focuses on two critical regions: the silicon nitride/silicon oxide interface and the TEOS dielectric layer as shown in Fig.3. Parametric studies were then conducted to analyze the influence of key design variables at the failure locations.

In the fracture mechanics model, both crack types were explicitly modeled to quantify the influence of design parameters on cracking risks. A 2D BEOL crack model was developed under plain strain conditions as illustrated in Fig.3. To accurately capture the stress and strain fields near the crack tip, a highly refined mesh with nanometer-scale resolution is applied in the local region.

Unlike conventional stress-based analysis, fracture mechanics does not rely on stress values to assess crack risk due to the singular nature of the stress field at the crack tip and the mesh dependency of stress magnitudes. Instead, the energy release rate is used as the primary metric.

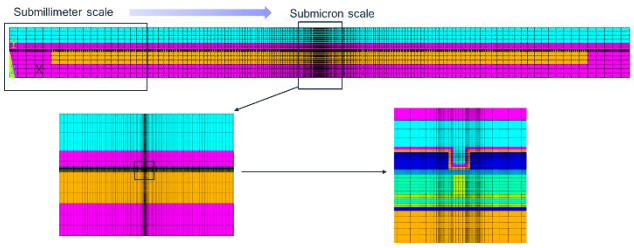
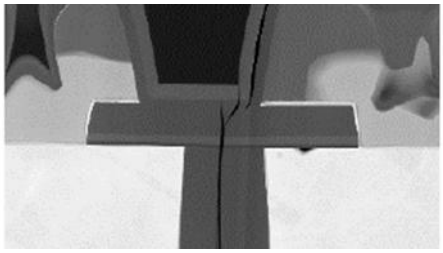


Fig. 2 2D Global model and local FEA mesh



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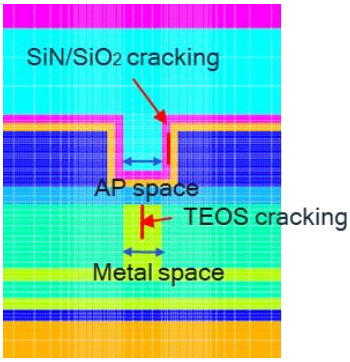


(b)

Fig. 3. (a) Cracks in the BEOL and (b) Fracture model

C. *Energy Release Rate*

In fracture mechanics, energy release rate serves as the fundamental driving force for crack propagation. The energy release rate, defined as the reduction in potential energy per unit area of crack growth, provides a mesh-independent and physically meaningful measure of the driving force for crack propagation. When the energy release rate exceeds the material's critical energy release rate, which is the threshold value of energy required to extend a crack by a unit area, the crack will propagate. This criterion is particularly relevant for brittle materials, where fracture occurs with minimal plastic deformation.

To compute the energy release rate in finite element analysis, several numerical techniques have been developed in finite element method, such as J-Integral and virtual crack closure technique (VCCT). The J-Integral provides a path-independent measure of the energy release rate around a crack tip, while VCCT estimates the energy required to close a crack by virtually reversing the crack opening process. These methods enable accurate and mesh-independent quantification of fracture driving forces in complex BEOL structures. Both methods are applicable within the framework of linear elastic fracture mechanics and are well suited for evaluating crack growth in brittle material.

For a crack in 2D domain, the J-integral is formulated as [4] [5]

$$J = \int_{\Gamma} W dx_2 - n_i \sigma_{ij} \frac{\partial u_i}{\partial x_1} ds \quad (1)$$

where Γ is any contour path around the crack tip starting from the bottom crack surface to top crack surface, W is the strain energy density, n_i is the normal vector normal to the path pointing outward, x_1 is the x coordinate variable, u_i is the displacement component, σ_{ij} is the stress component, and ds is an infinitesimal increment along the path. The schematic of domain to calculate J-integral is shown in Fig. 4.

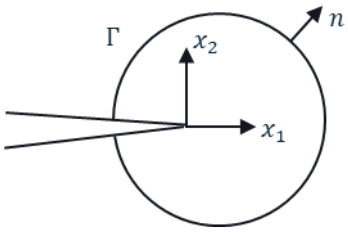


Fig. 4. J-Integral computation schematic

In numerical calculation, a practical approach is to convert path integral into domain integral. By Gaussian integration theory, the contour path integral can be converted into integral on an area domain enclosed by the contour around the crack tip as

$$J = \iint_A \left(\sigma_{ij} \frac{\partial u_i}{\partial x_1} - W\delta_{1i}\right) \frac{\partial q}{\partial x_i} dA \quad (2)$$

where δ_{1i} is the Kronecker delta and q is a weight function.

The VCCT method assumes that the energy to separate a surface is equal to the energy needed to close the same surface. In VCCT method, the energy release rate is defined as [6]

$$G_I = -\frac{1}{2\Delta a} R_Y \Delta v \quad (4)$$

$$G_{II} = -\frac{1}{2\Delta a} R_X \Delta u \quad (5)$$

where G_I and G_{II} are defined as mode I and mode II energy release rate, respectively, Δu and Δv are relative displacement between the top and bottom nodes of the crack face in local coordinates x and y, respectively, R_X and R_Y are reaction force at the crack tip, and Δa is the crack extension. The schematic of VCCT method is shown in Fig. 5. The total energy release rate is the sum of the two components.

To validate the accuracy of the fracture mechanics model, both the J-Integral method and the Virtual Crack Closure Technique (VCCT) were employed to compute the energy release rate. These two independent approaches showed comparable results, confirming the robustness of the

simulation framework. For consistency and clarity, the results presented in the simulation section are based on the J-Integral method, which offers a path-independent and numerically stable formulation for evaluating crack driving forces in brittle materials.

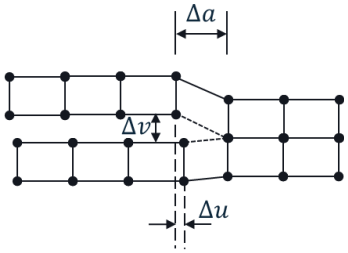


Fig. 5. VCCT method diagram

D. Design Parametric Evaluation

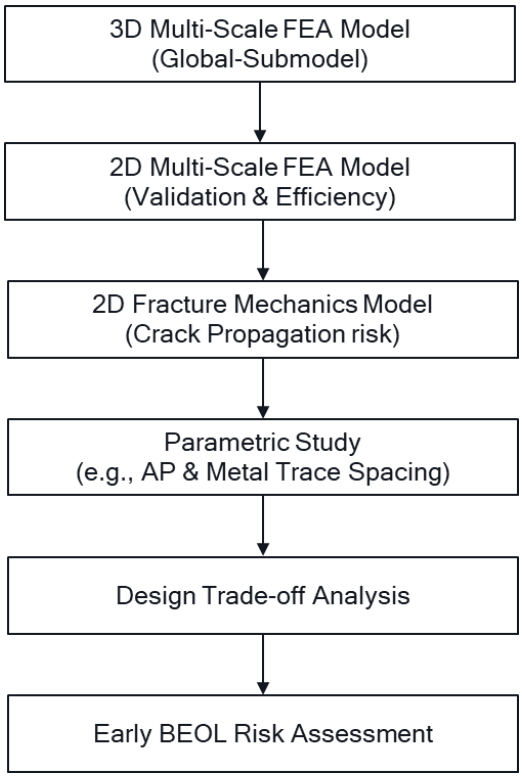
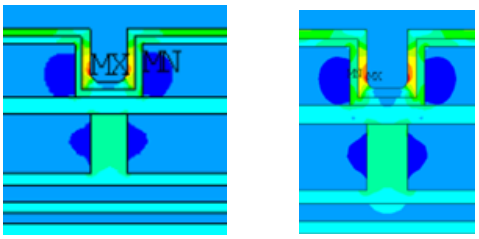


Fig. 6. Flowchart of using multi-scale FEA model set for early-stage design analysis

A flowchart of the developed multi-scale FEA modeling to support early-stage chip design analysis is given in Fig. 6. Starting from 3D model, the stress distribution is first predicted. A 2D model is then developed to validate the model accuracy. A 2D fracture mechanics model is further developed for crack propagation risk. Using the 2D fracture models, parametric studies can be conducted to investigate the influence of key design variables with satisfactory model efficiency and accuracy. Specifically, the spacing of aluminum pads (AP) and BEOL metal traces are varied to assess their impact on stress concentration and fracture risk. This modeling approach provides a framework for early-stage design evaluation for micro-scaling cracking risk, enabling designers and process engineers to assess BEOL risks prior to physical prototyping or wafer fabrication.

III. Simulation Results

Thermo-mechanical stress is induced due to the mismatch in material properties across the BEOL stack. Finite element simulations reveal that high stress concentrations occur at the silicon nitride layer as shown in Fig. 7. Additionally, regions confined by top-layer thick metal traces show elevated stress, indicating potential locations for cracking depending on the local material and interface toughness. Both 3D and 2D models show similar stress contours in the vicinity of the failure locations.



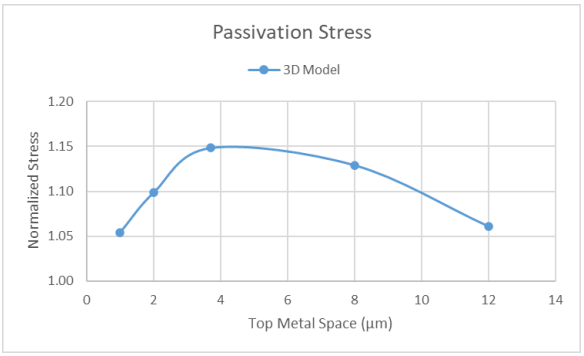
(a) (b)

Fig. 7. Stress contour in the local region (a) 3D model stress contour and (b) 2D model stress contour

Figure 8 represents the normalized stress in passivation layer as a function of top metal spacing. The stress values are normalized against a baseline with solid thick metal coverage. The results from both 3D and 2D models show consistent trends, further supporting the use of the 2D model for efficient parametric studies.

Interestingly, the peak stress in the passivation layer exhibits a non-monotonic relationship with metal trace spacing. The stress increases initially and then decreases as the spacing continues to widen. Therefore, it is important to evaluate the impact of thick metal spacing on stress at both failure-prone regions for a comprehensive understanding of stress-induced cracking risk.

To gain deep insight into the cracking risk, a fracture mechanics approach was employed to quantify the energy release rate associated with two critical failure modes: interfacial cracking between silicon nitride and silicon oxide, and bulk cracking within the TEOS material confined by top metal traces. The energy release rate is normalized against the baseline case where both aluminum pad (AP) spacing and thick metal trace spacing were set to 2 μm.



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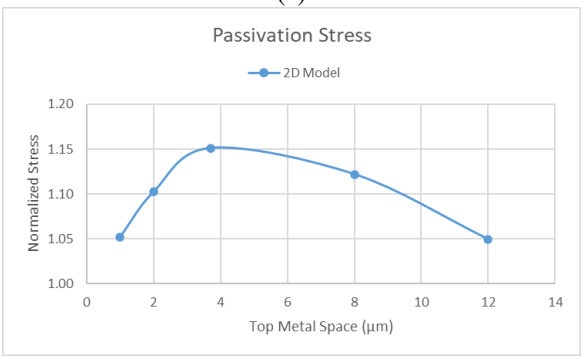

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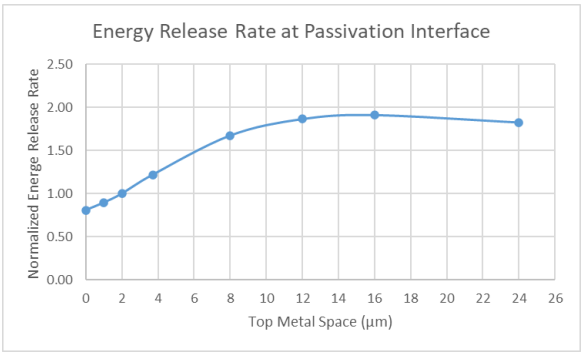
Fig. 8. Stress variation as a function of thick metal space (a) 3D Model and (b)2D Model



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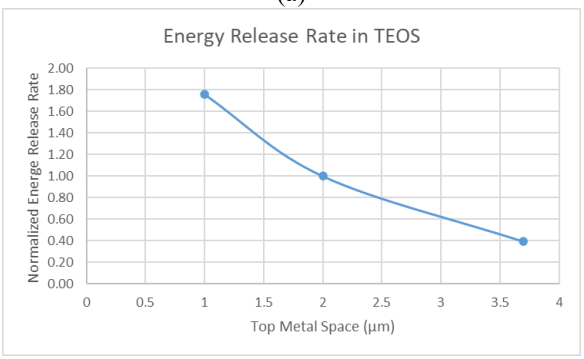

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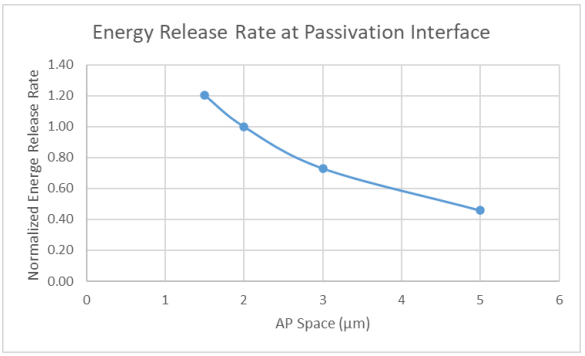
Fig. 9. Energy release rate as function of top metal space (a) die passivation cracking (b) TEOS cracking



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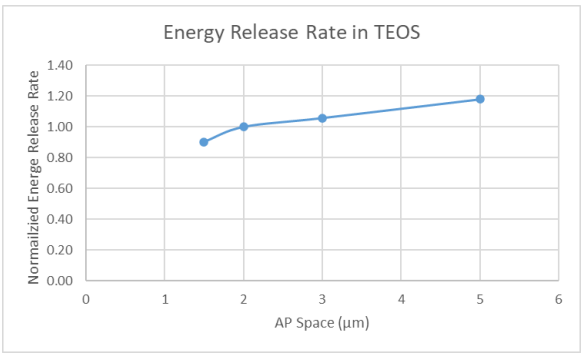

(b)

Fig. 10. Energy release rate as a function of AP space (a) die passivation cracking (b) TEOS cracking

As shown in Fig. 9 (a), the normalized energy release rate at the silicon nitride/silicon oxide interface increases with metal spacing up to a certain point, after which it gradually decreases. The trend indicates that a larger metal spacing beneath the die passivation layer can initially increase the silicon nitride/silicon oxide cracking propagation risk but may reduce the risk with further widened spacing. However, as shown in Fig. 9(b), the energy release rate within the TEOS material confined by metal space decreases consistently with increasing metal spacing, showing opposite trend. It indicates that wider thick metal spacing helps reduce stress in the TEOS material, thereby reducing the cracking risk of TEOS materials.

These opposing trends indicate that an optimized top metal spacing is essential to mitigate cracking risks at both the passivation interface and within the TEOS dielectric, ensuring robust mechanical reliability in BEOL structures.

In addition to metal trace spacing, the AP spacing also plays a significant role in influencing fracture behavior within the BEOL structure. As shown in Fig. 10(a), the energy release rate at the silicon nitride/silicon oxide interface decreases significantly with increasing AP spacing. This trend suggests that a wider AP spacing beneath the die passivation layer can effectively reduce the risk of silicon nitride/silicon oxide cracking.

In contrast, Fig. 10(b) illustrates that the energy release rate within the TEOS material increases with larger AP spacing. This indicates that while increasing AP spacing may benefit the passivation interface, it can simultaneously elevate the cracking risk in the TEOS region confined by metal traces.
The results revealed that these design parameters affect the two failure modes in opposite ways. These opposing effects reinforce the importance of trade-off analysis in layout optimization. An appropriate balance in AP spacing is necessary to mitigate failure risks across both critical regions.
It is important to note that the specific dimensions of AP and metal trace spacing may vary depending on the BEOL architecture and material systems used in different product designs. The results presented here are intended as an illustrative study to demonstrate the influence of design variables on cracking risk, rather than to prescribe specific design rules.

IV. Conclusions

The study provides a simulation modeling-based framework for evaluating BEOL-level failure risk in flip chip packages, focusing on two critical failure modes: die passivation cracking and TEOS layer cracking. A multi-scale finite element analysis (FEA) approach was developed to assess stress distributions and fracture risks under thermal loading conditions. The modeling framework incorporates both 3D and 2D simulations, along with a 2D fracture mechanics model, to enable efficient and accurate analysis of design-dependent failure risks.
The results demonstrate that key design parameters, specifically aluminum pad (AP) spacing and thick metal trace spacing, have opposing effects on the two failure modes. A larger metal trace spacing beneath the die passivation increases the energy release rate at the silicon nitride/silicon oxide interface, thereby elevating the risk of passivation cracking. However, it simultaneously reduces the energy release rate within the TEOS layer, mitigating the risk of TEOS cracking. Conversely, increasing AP spacing reduces the risk of passivation cracking but increases the risk of TEOS cracking. It is important to note that the dimensions of AP spacing and metal trace spacing may vary depending on product architecture and material systems.
These findings underscore the importance of trade-off analysis in BEOL layout optimization. The modeling methodology presented here provides a valuable framework for early-stage design evaluation. By enabling simulation-based predictive assessment of failure risks, this approach supports the development of robust and reliable chip designs. This study also recommends that semiconductor foundries conduct analogous assessments during the early phases of future technology node development, to facilitate a more systematic approach to identifying and balancing competing failure mechanisms.

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