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System Modeling for Advanced AI Superconducting Hardware

IMAPS ATW
Sep 23, 2025

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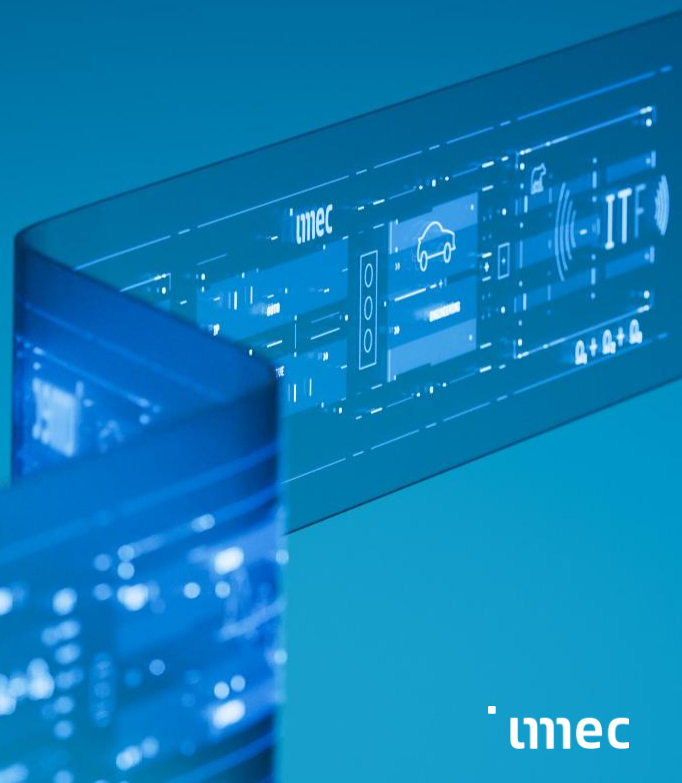

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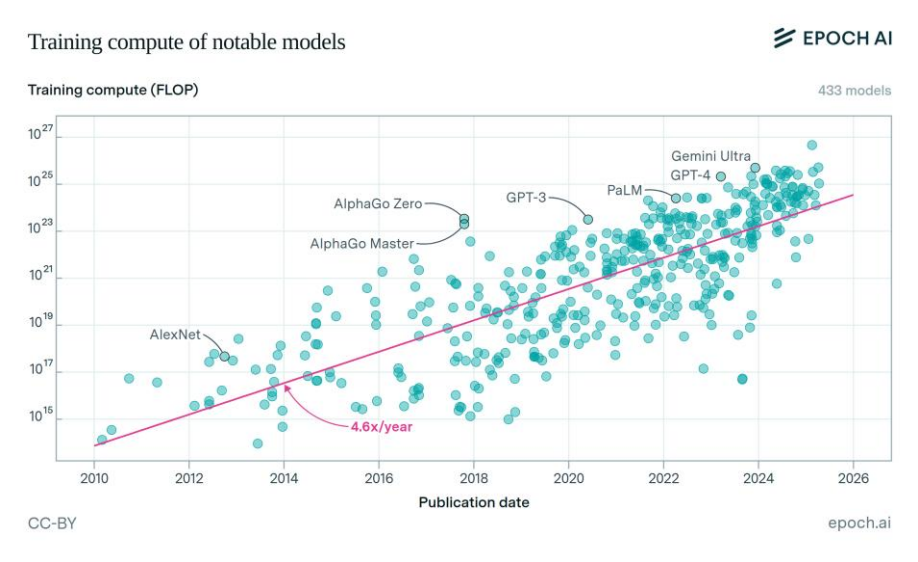
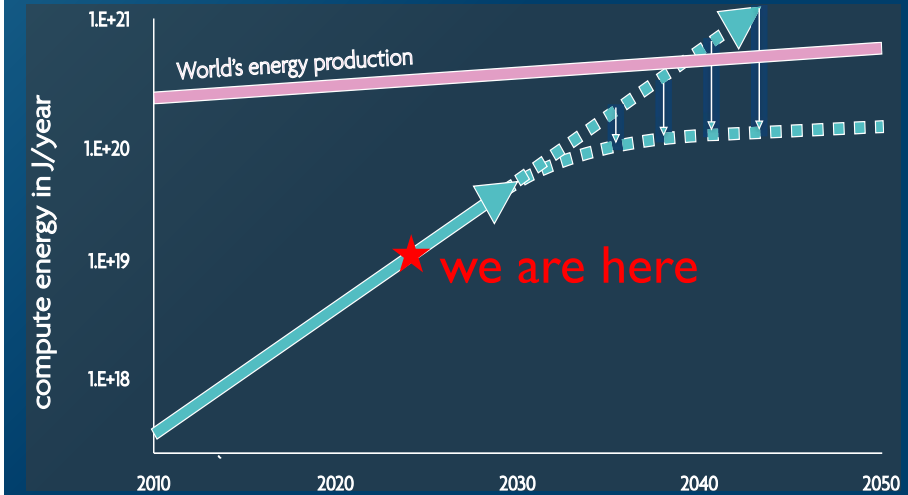
Outline

- Motivation for cryogenic computing (Superconducting Digital)
- Introduction to superconductivity
- SCD technology innovations and capabilities at imec
- Superconducting circuits and system modeling

Demand for computing is soaring





AI compute growing:
4.6X per year

By 2040 ***50%*** of world's electrical power will be used for computing

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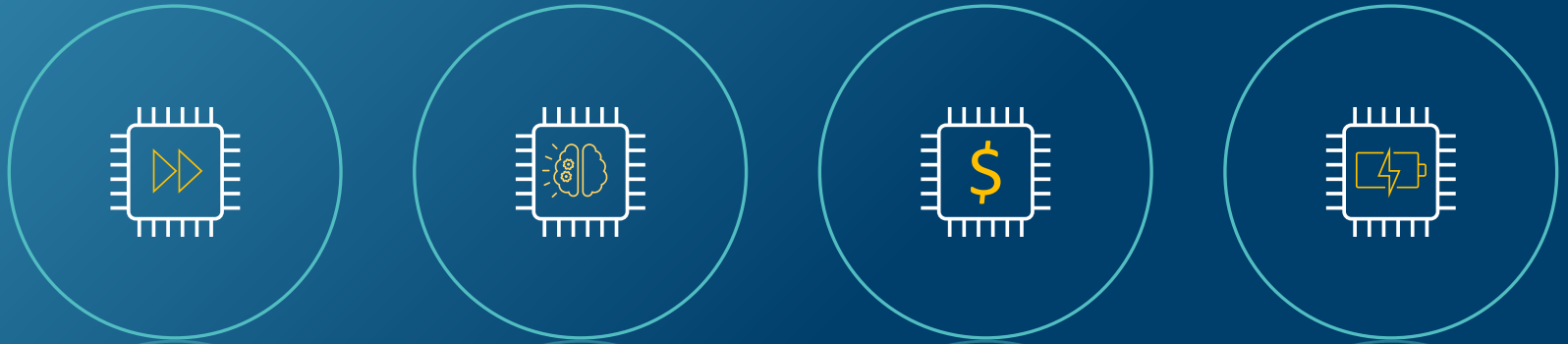
Enabling a comprehensive solution for SCALING

Superconducting Digital Technology



1000X BANDWIDTH

1000X COMPUTE DENSITY

AI @10% TCO

100X ENERGY EFFICIENCY

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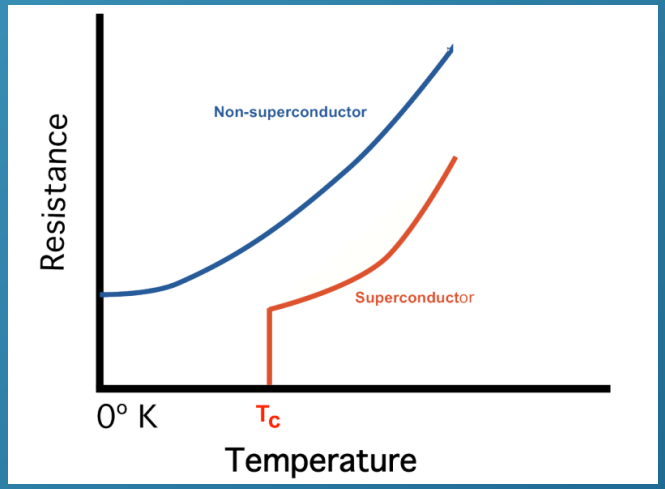
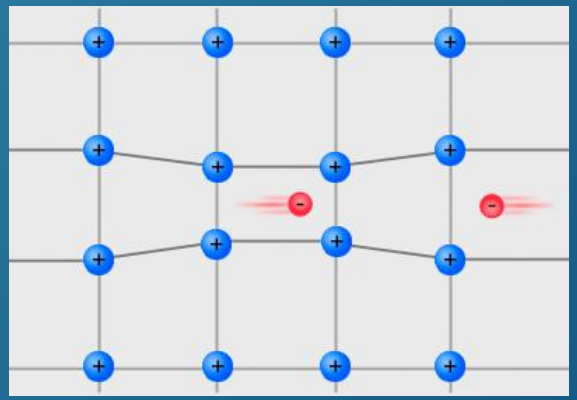
What is superconductivity

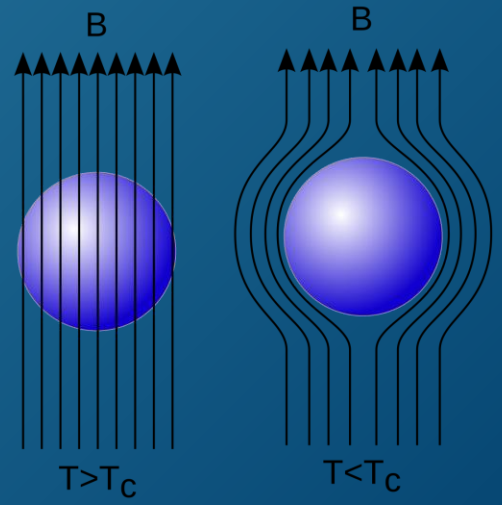
A perfect, zero resistance electrical conductor



Zero resistance, T<Tc



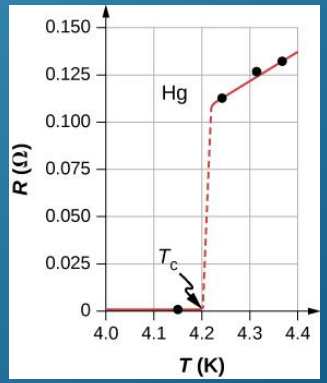
Cooper pairs carry suppercurrent



Perfect diamagnet

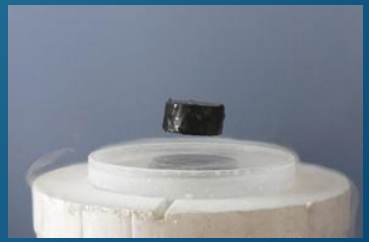
Physics of superconducting digital devices

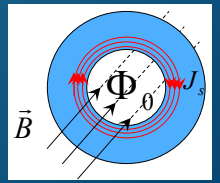
Zero resistance wires



- THz bandwidth interconnects
- Optical like interconnects with no amplification

Meissner effect

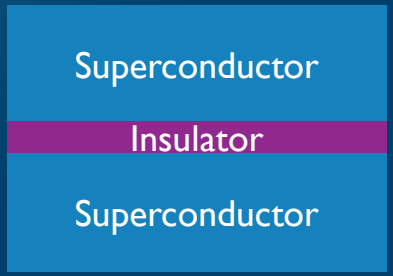


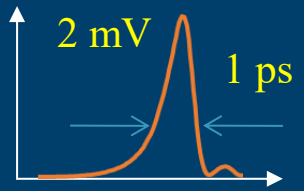


$$\Phi_0 = \frac{h}{2e} \approx 2\ \text{mApH}$$

- Quantum accurate digital bits
- Large noise margin
- Fundamental limit for energy

Josephson junction





E = 0.2 aJ

- Fast, low energy logic and memory

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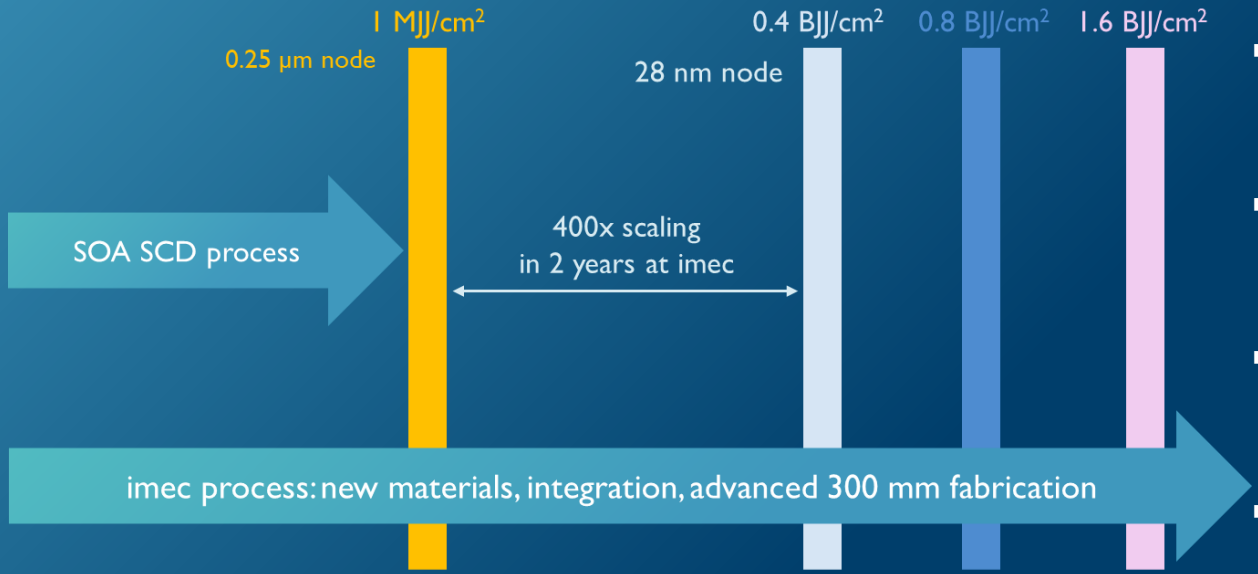
New material and fabrication flow

State-of-the-art Nb technology		imec NbTiN technology
200°C budget	Process compatibility	420°C budget
250 nm feature size	Device density	50 nm feature size
200 mm wafers	Process scalability	300 mm wafers
T_C ~ 9 K	Material properties	T_C > 12 K
Low L_{kinetic}	Routing density & EDA	High L_{kinetic}

Key innovations: make SCD practical

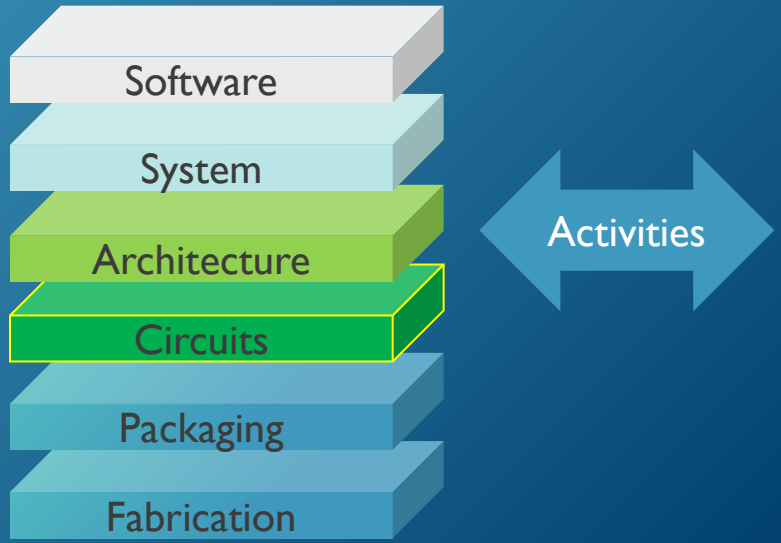
Re-starting Moore's law – for compute at scale!



- 28 nm fabrication stack with new materials (300 mm)
- Device Scaling → 2X density / node
- Power Scaling → AC power distribution with capacitors
- Cold-DRAM & Josephson SRAM

System technology co-development

Application driven full stack system technology co-development



- Performance modeling
- EDA development
- Development of superconducting modules: compute, memory, power delivery
- Interface to room temperature
- Packaging
- PDK development
- Technology development & scaling
- Testing & characterization

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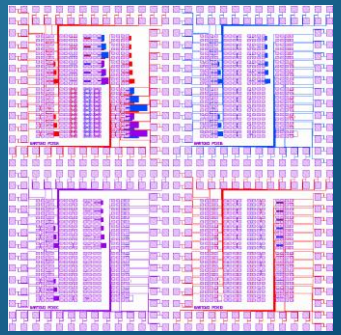
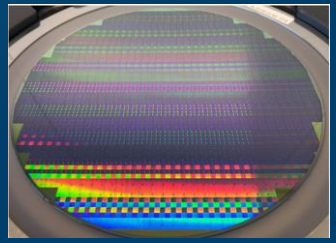
Imec capabilities

Personnel, Infrastructure and Funding

Team



Bartow



- **Design & Test**
- **4 K cryostat & test equipment**
- **New cryostat & lab building**

>129,000 sqft Cleanroom

imec, Leuven

imec, Florida
Regional talent

Supported by Osceola County, State of Florida, imec INVEST+, FSE, DOE, and LPS

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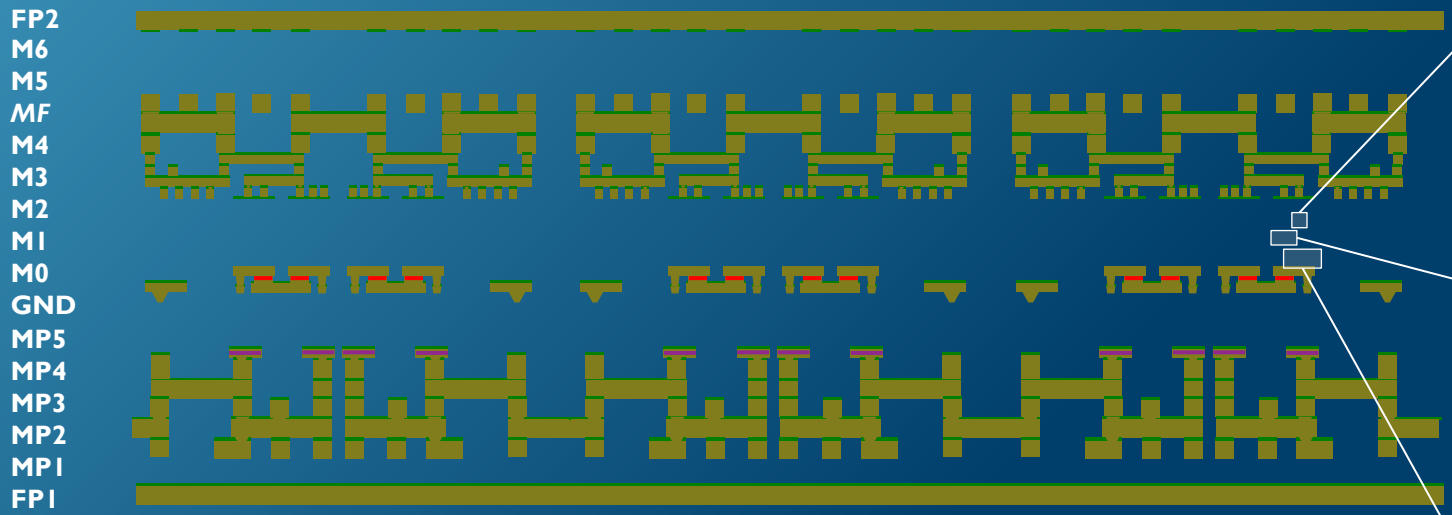
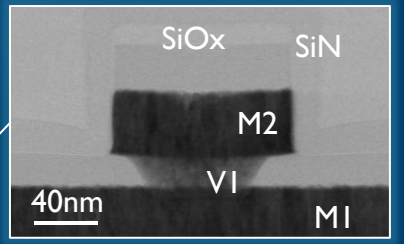
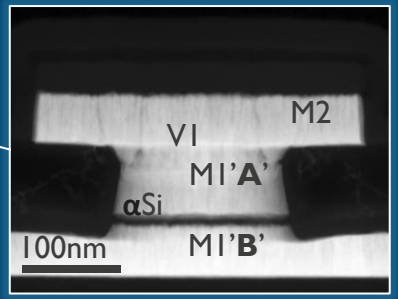
Superconducting Digital Technology

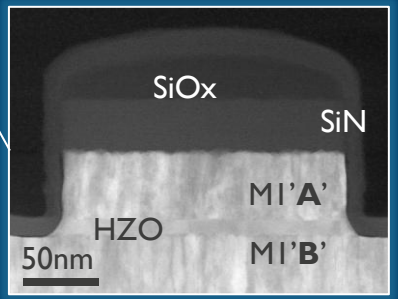
The Process Stack

Fabrication







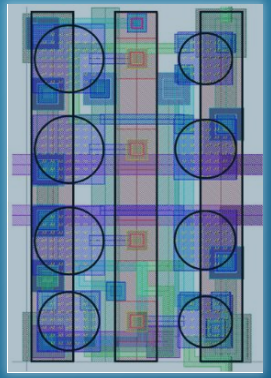


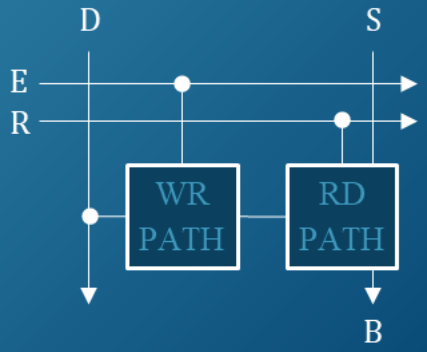
16ML stack vision to enable scalable superconducting digital technology

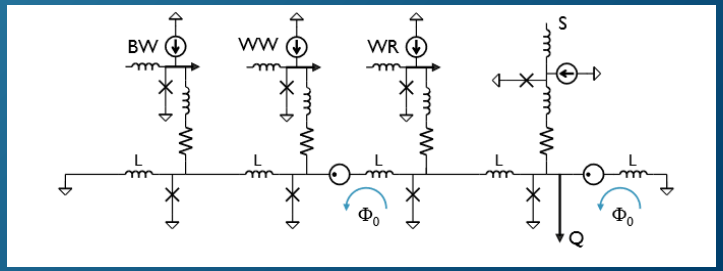
- Flux trapping layers
- Superconducting BEOL (wires & vias)
- Superconducting FEOL (Josephson Junction)
- Power Delivery Network (MIM capacitors, wires & vias)

SCD circuits and gate library

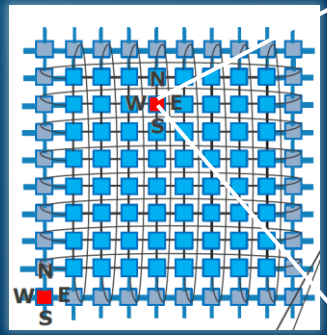
Inform system models and PDK development



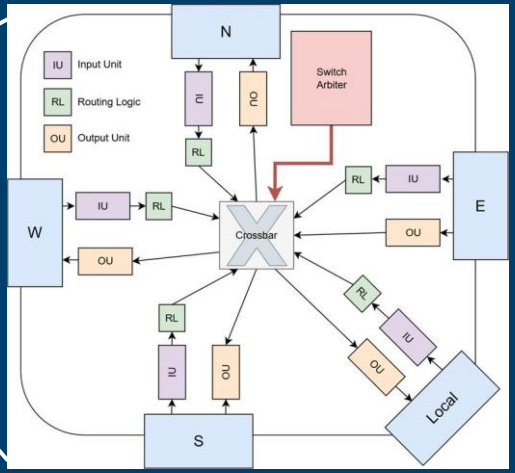




Josephson SRAM cell



SCD Network

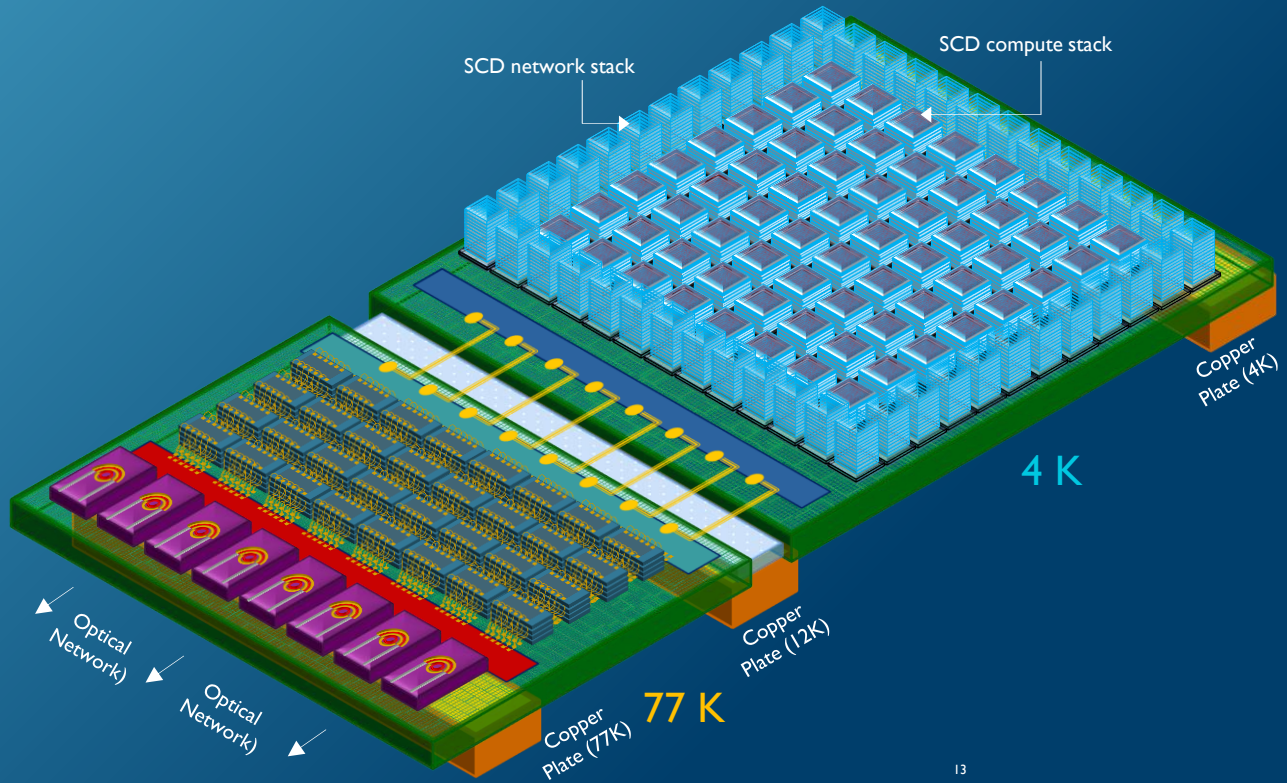


Circuits

Supported by FSE

Superconducting Digital Systems

Scale up (3D Integration) → Superconducting Blade



Superconducting interposer (4 K)

+ Superconducting compute stacks
+ Superconducting network stacks

Glass bridge / thermal break

+ 4 K–77 K link

Cryo-CMOS interposer (77 K)

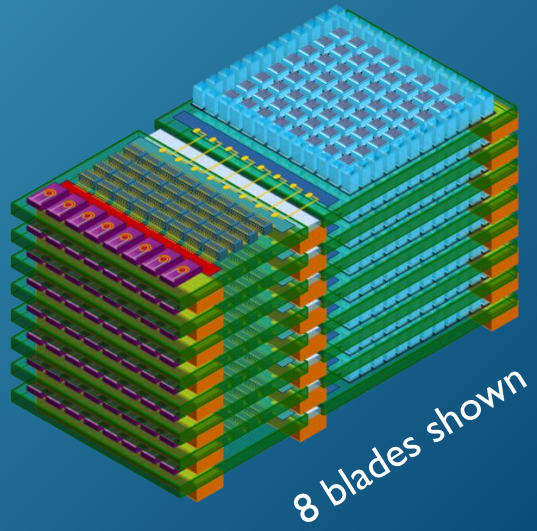
+ Cryo-DRAM

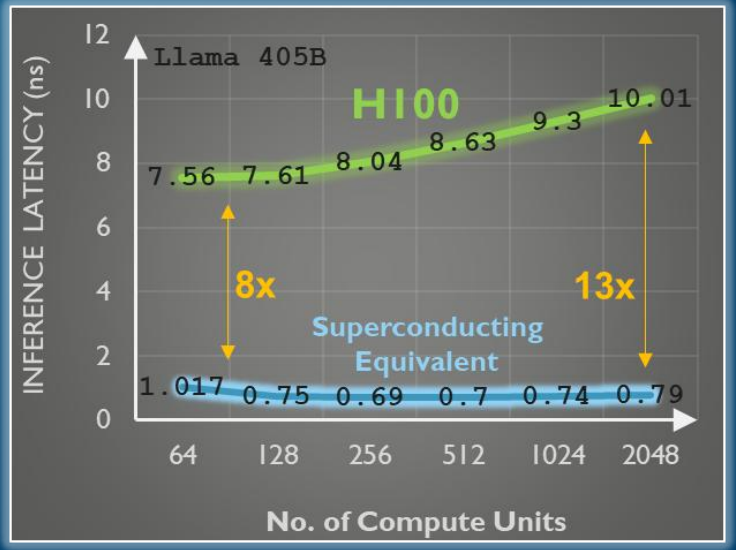
Cryo-optical modulators

SCD system modeling

System

Analytical Performance Modeling





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Summary

- SCD technology can perform exascale computing at 100x less power and 1000x integration density
- These gains are enabled by the physics of superconducting devices combined with the advanced process and packaging technologies
- Imec demonstrated sustainable scaling for SCD
- Imec performs system technology co-development of SCD technology

Thank You

Questions?

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