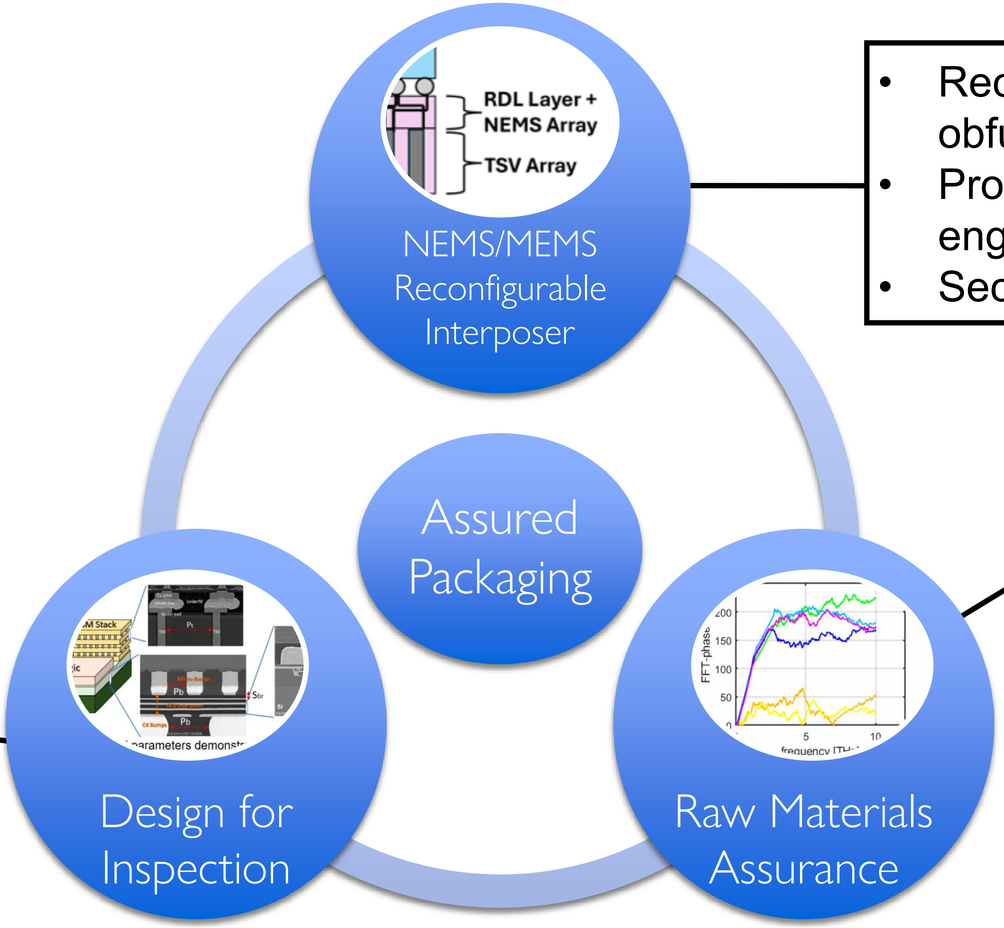
AI-Driven Non-Destructive Characterization for Advanced Packaging: Challenges, Frameworks, and Opportunities

Patrick Craig, Navid Asadi

Project Scope and Goal



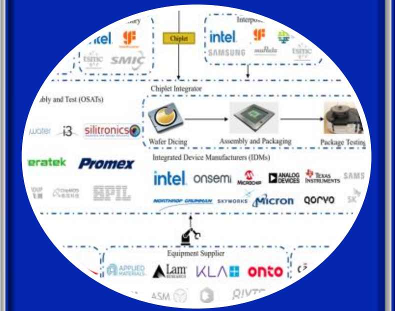
- Reconfigurable interposer for obfuscation
- Protects SoC IP from reverse engineering
- Secure interposer IP

- Optimizes packaging design for X-ray inspection
- Improves defect visibility and localization
- Provides inspection-aware design IP

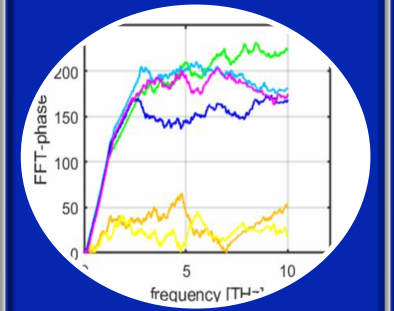
- Benchmarks material reliability for SoCs
- Uses microscopy/spectroscopy datasets
- Software outputs predictive reliability scores

Goal: Provide a multi-faceted approach to address assurance, reliability, and inspection challenges of advanced packaged SoCs.

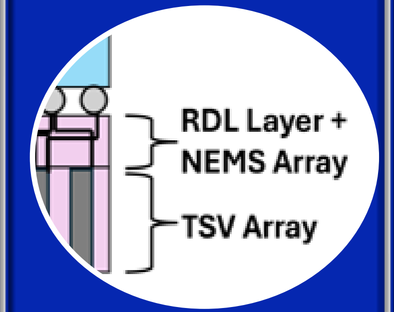
Presentation Overview



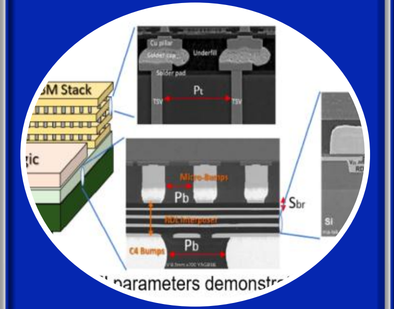
Vulnerabilities in the Advanced Packaging Supply Chain



Raw Materials Security Framework



NEMS/MEMS Reconfigurable Interposer



Design for Inspection

Security and Assurance Lab Capabilities

Future Work and Take-Aways

Topics of this Presentation

- What are the vulnerabilities in the microelectronics supply chain?
- How can analysis of raw materials, NEMs/MEMs interposer, and design for inspection help build trust?
- What future directions are being taken to reach total trust and increase inspection capabilities?

Advanced Packaging Supply Chain

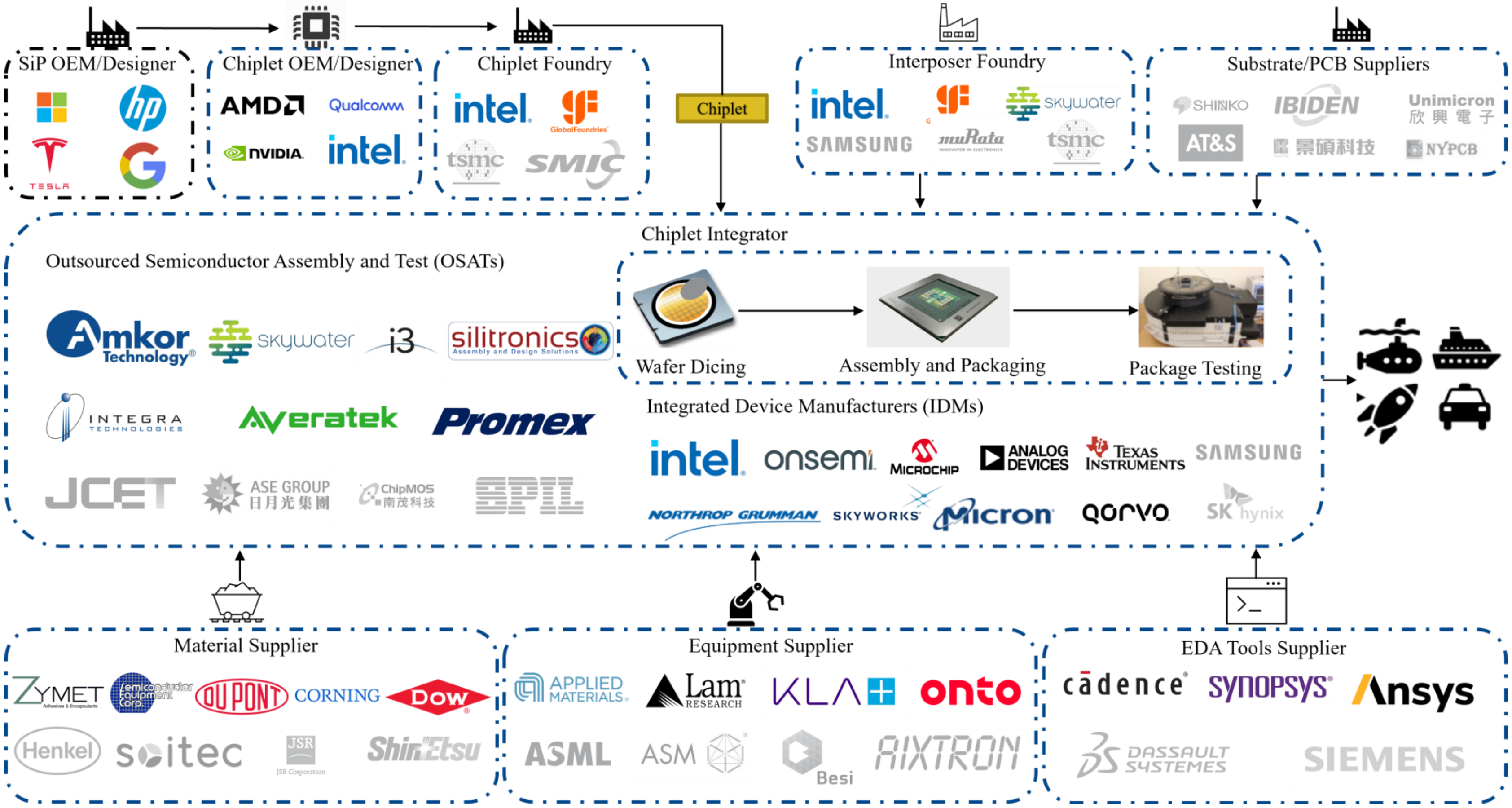
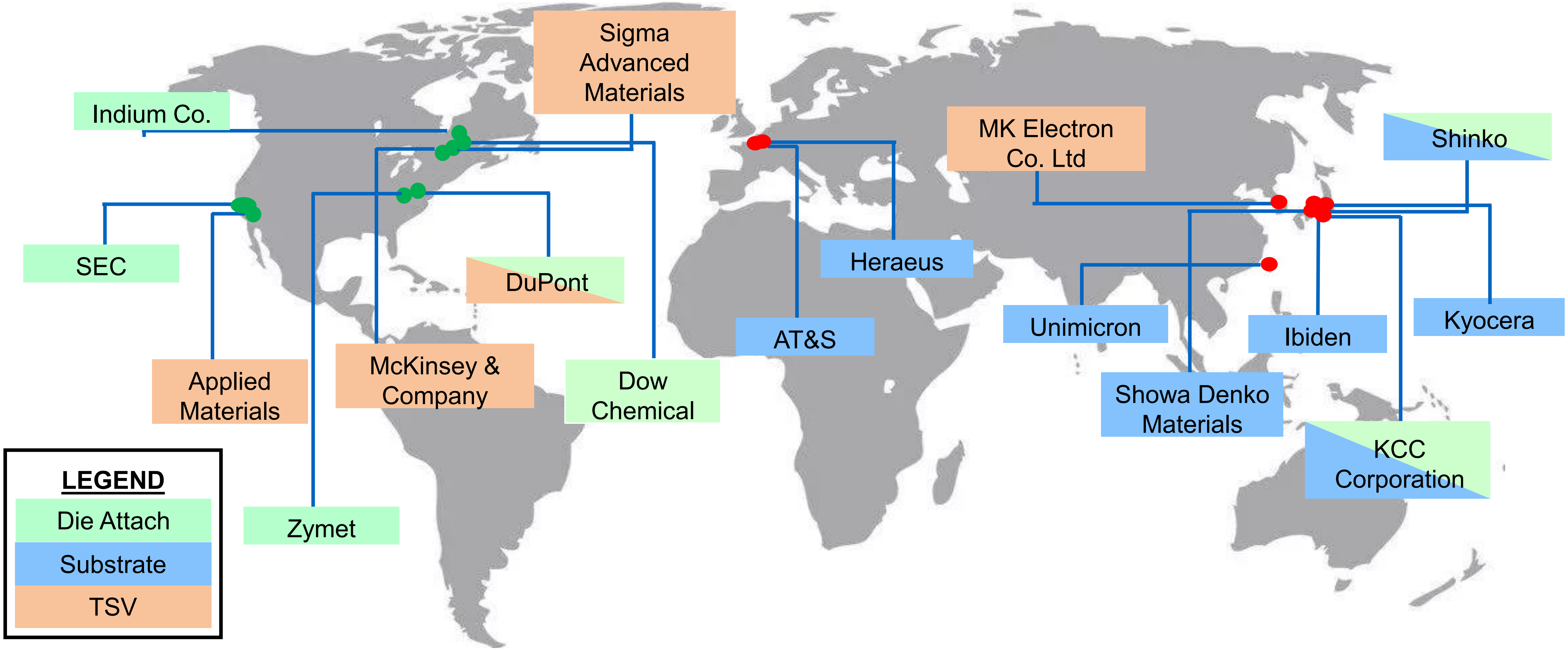


Figure 1: US-based advanced packaging supply chain

- ✓ End-to-End semiconductor ecosystem involves diverse stakeholders
- ✓ Defense, automotive, and aerospace drive demand for secure and reliable Packaging
- ✓ Foundries and OSATs enable wafer fabrication and advanced packaging
- ✓ Raw Materials vendors drive innovation in materials for packaging

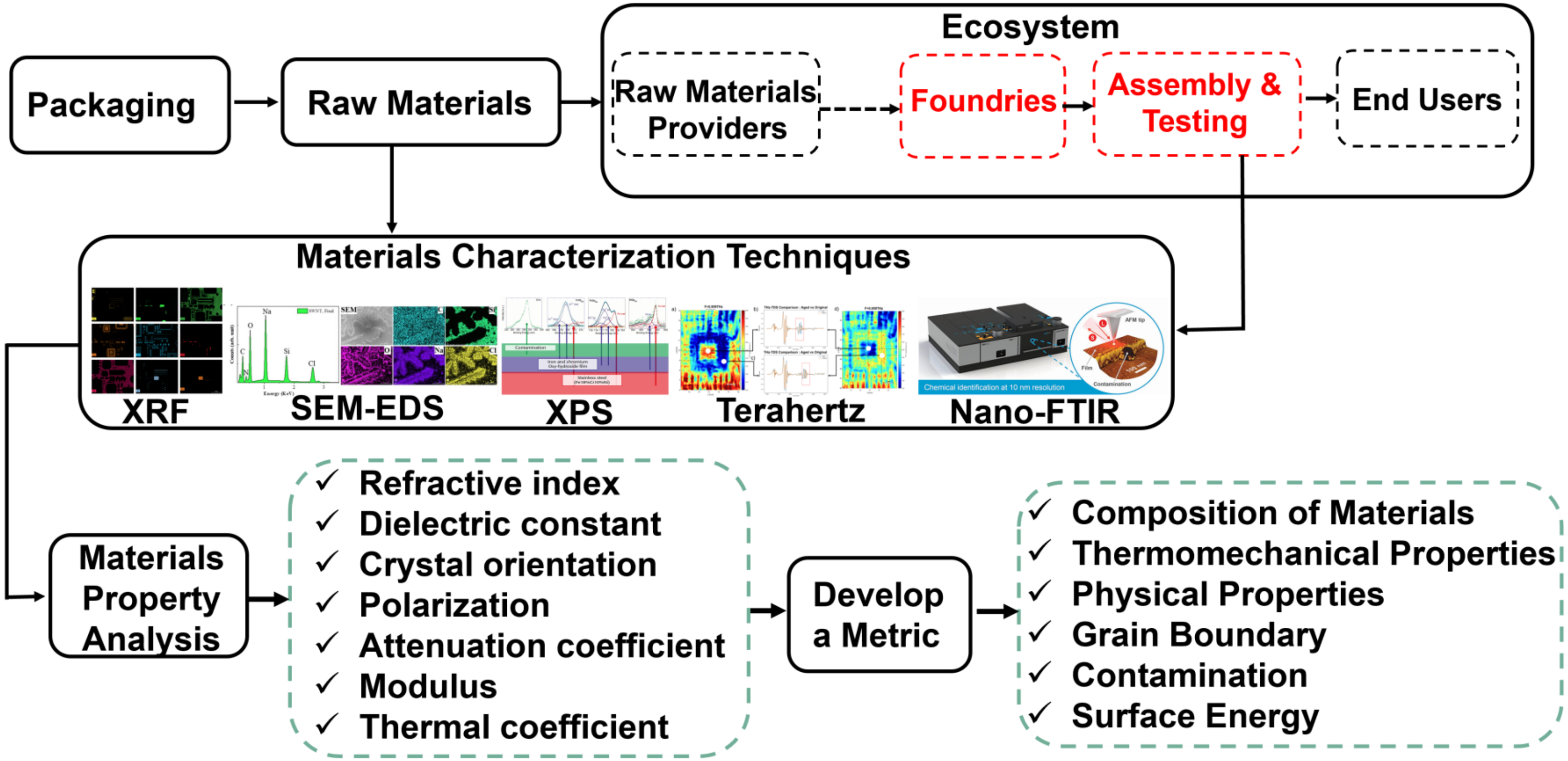
Heavy reliance on overseas fabs and third parties increases risk to the SoC supply chain and security.

Providers of Substrate, TSV & Die Attached Raw Materials



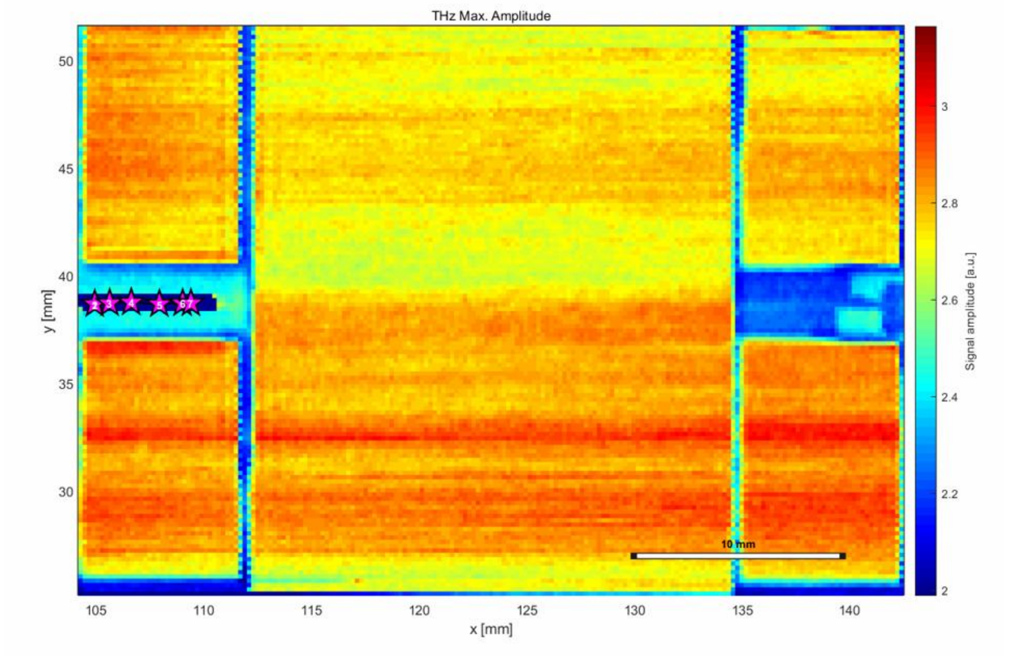
Reliance on global suppliers creates vulnerabilities and disruptions or quality issues risk product reliability and trust.

Framework for Advanced Packaging Raw Materials Assurance



- ✓ Packaging Material Integrity Depends on Raw Material Provenance
- ✓ Advanced Characterization Techniques Enable In-Depth Material Analysis
- ✓ Comprehensive Property Analysis Drives Material Qualification
- ✓ Toward a Quantitative Metric for Raw Material Quality Assessment

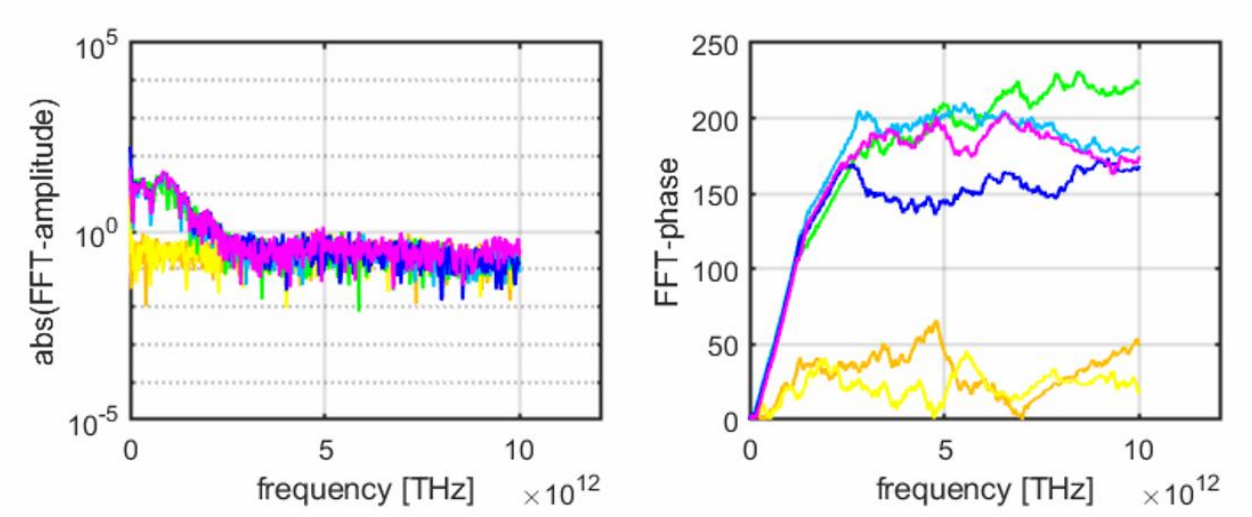
THz-TDS for Packaging Material Characterization



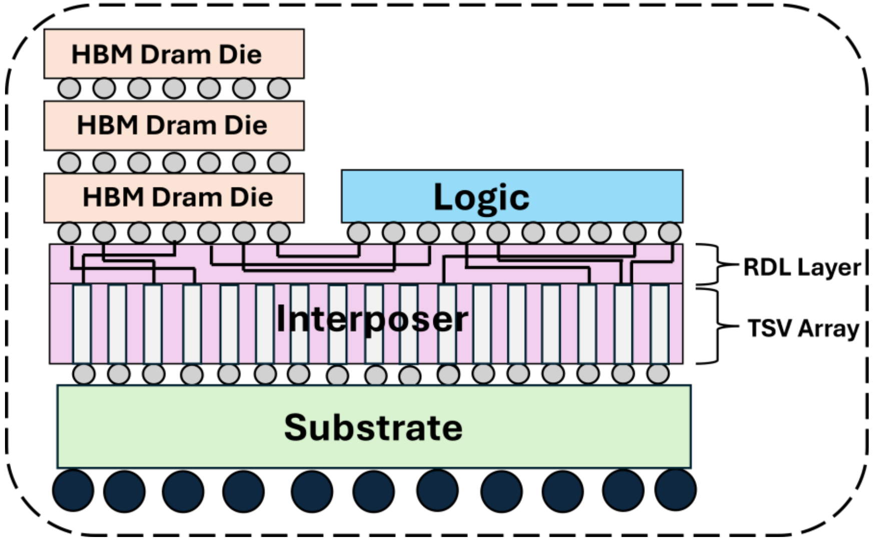
Experimental Results: NVIDIA P100

- ✓ Optimized THz frequencies provide targeted insights: different frequencies revealed structural details with distinct features (interfaces, anomalies)

- ✓ Need for non-destructive inspection tools to verify material integrity
- ✓ THz imaging provides a unique ability to probe dielectric properties and hidden structures without damaging packages

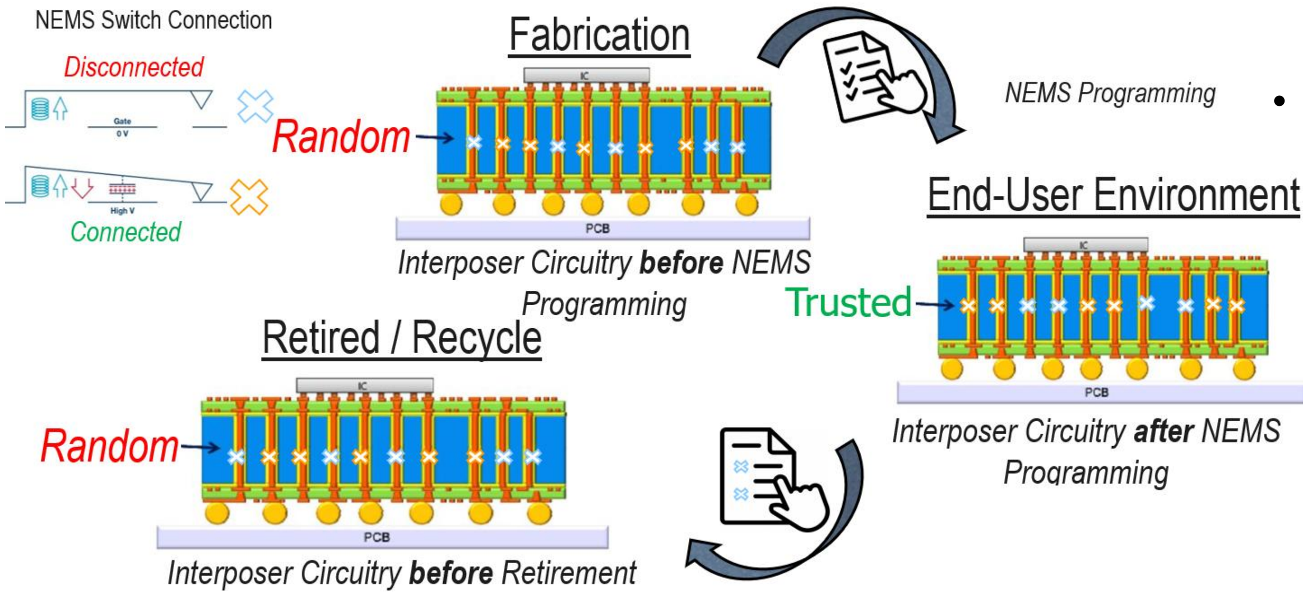


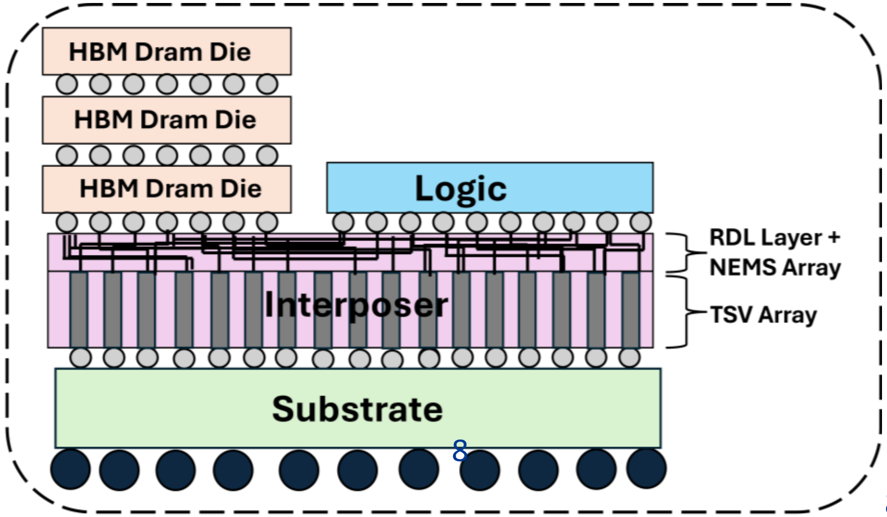
Reconfigurable NEMS



Potential Threats	Existing Package	NEMS Based Package
Reverse Engineering	☑☑☑	✗✗✗
Counterfeiting	☑☑☑	✗✗✗
Cloning	☑☑	✗✗
Tampering	☑☑☑	✗✗
Hardware Trojan	☑☑	✗✗

- Concealed golden design during interposer fabrication to prevent IP theft.
- Enabled two-level activation to block recycling and reverse engineering.

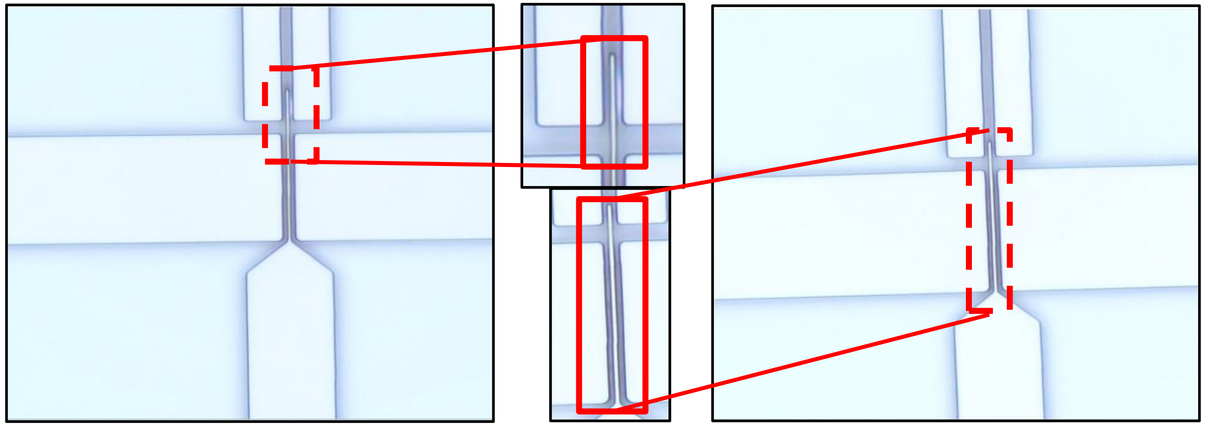




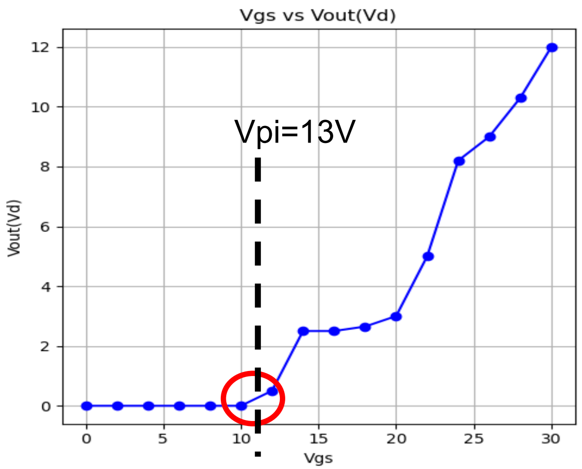
Prototype Testing Results

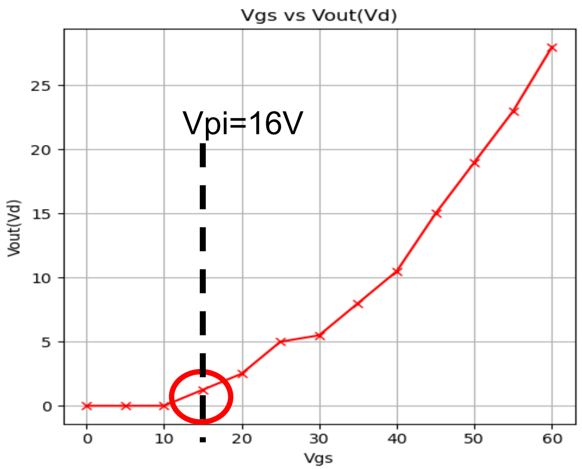
Physical Inspection and Visual Check
- KGD
- Cantilever release
- Material Texture

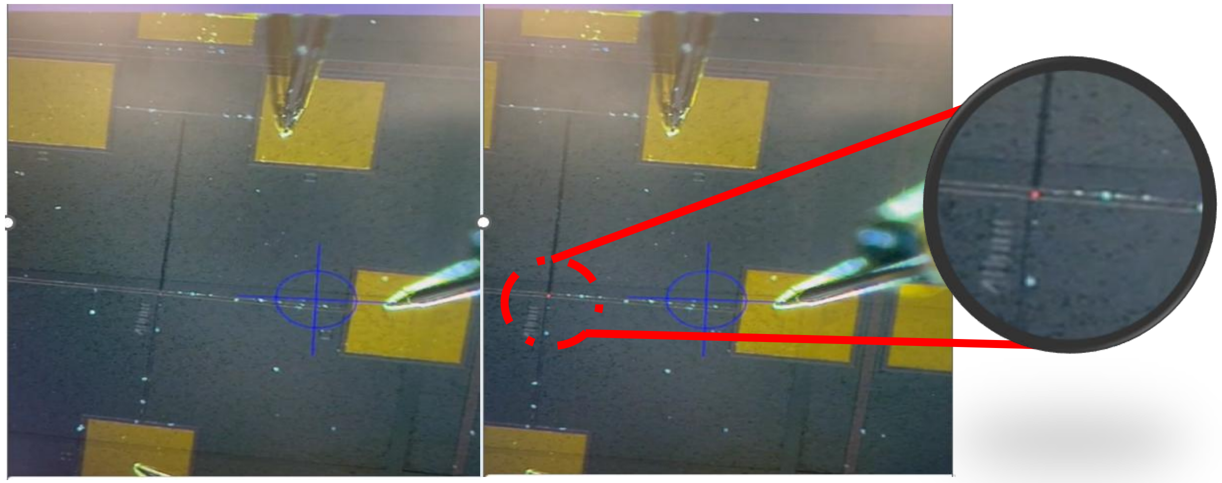
Electrical Characterization (very few)
- Vpi – 13V-16V
- Burn-in Test – 33V above until 60V
- Repeatability



Good and Bad die(Switches)







Burn-in Test for the NEMS switch

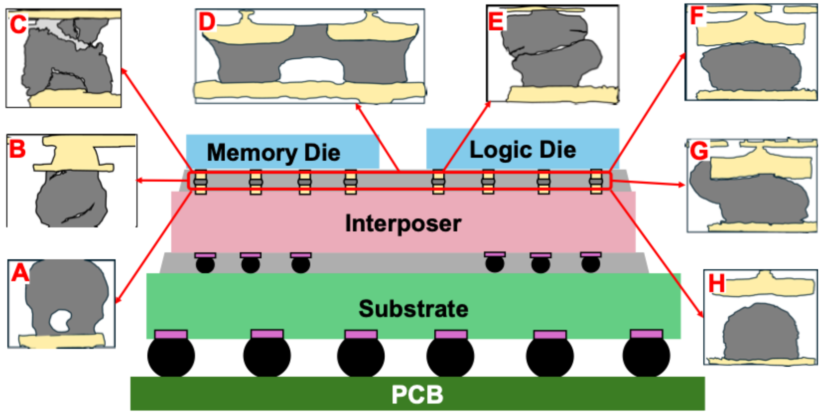
Inspection Challenges of 3D Packaging

Defect detection challenges in advanced packaging:
- Variety of defects (e.g., void, fatigue crack, bridging, etc.)
- Defects size vs. component size
- Complex stacked 3D structures

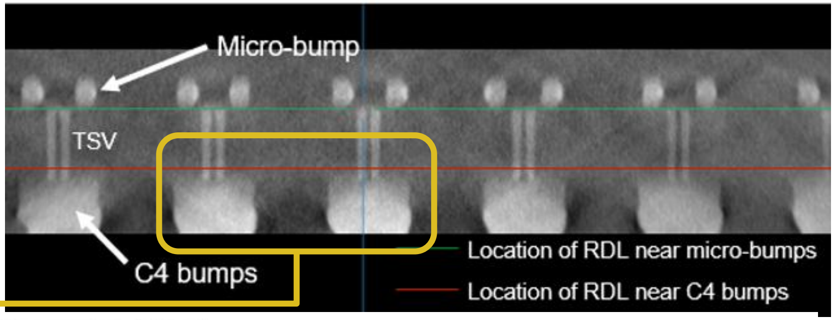
X-ray inspection challenges:
- Noise, blur and scatter in X-ray images
- Strict constraints of in-line inspection for yield

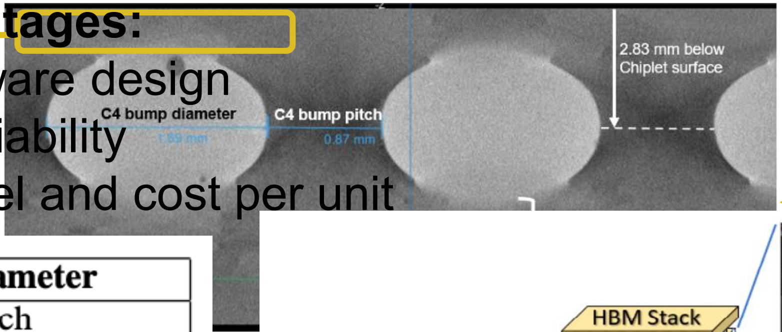
Parameters affecting X-ray inspection challenges:
- Design parameters (design specification + material composition)
- Imaging parameters

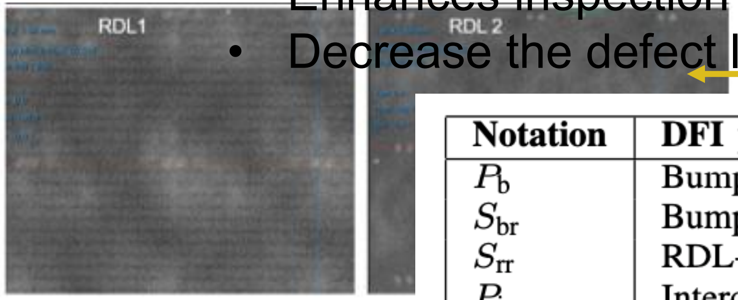
Design for Inspection (DFI) Advantages:
- Facilitates inspection-aware design
- Enhances inspection reliability
- Decrease the defect level and cost per unit



A 2.5D advanced package structure and possible defects in microbumps



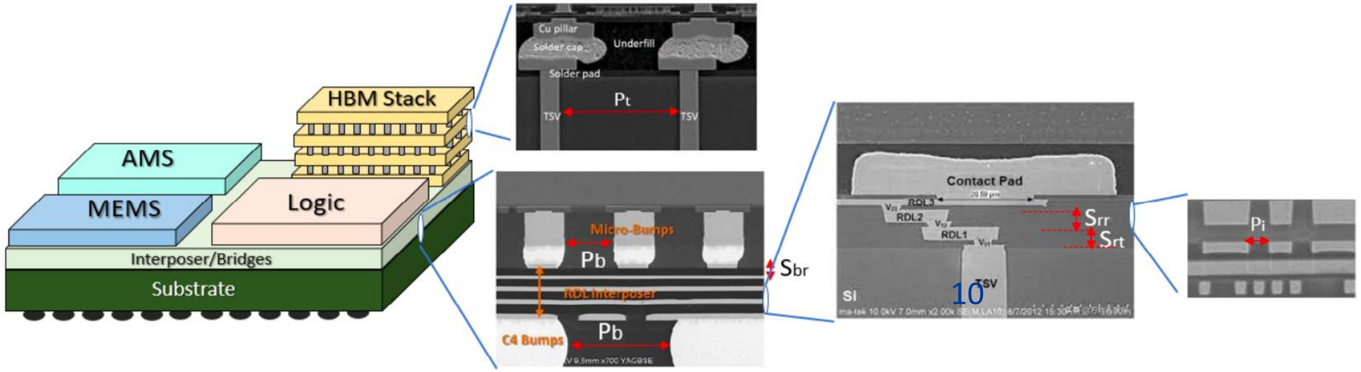




RDLs vertically abov

ros

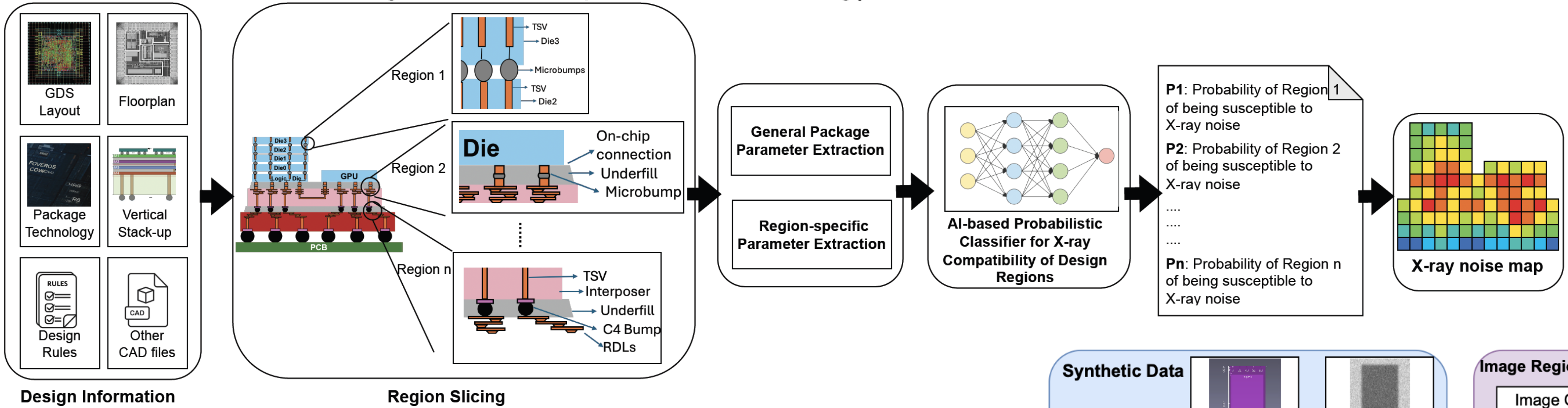
Notation	DFI parameter
P_b	Bump pitch
S_{br}	Bump-RDL spacing
S_{rr}	RDL-RDL spacing
P_i	Interconnect spacing
S_{rt}	RDL-TSV spacing
P_t	TSV pitch



DFI-based solutions for Inspection Challenges

Design-based inspection (DBI) for X-ray compatibility

- DBI tailors inspection processes to design-specific requirements
- Predict X-ray noise susceptibility of design regions
- *Commercialization: integration in inspection/ metrology tools*

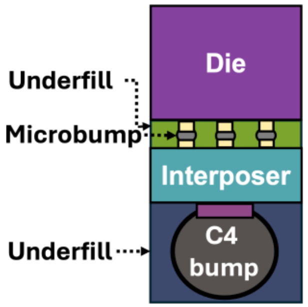


Experimental setup and case study analysis

- Experimental setup of framework and case study analysis

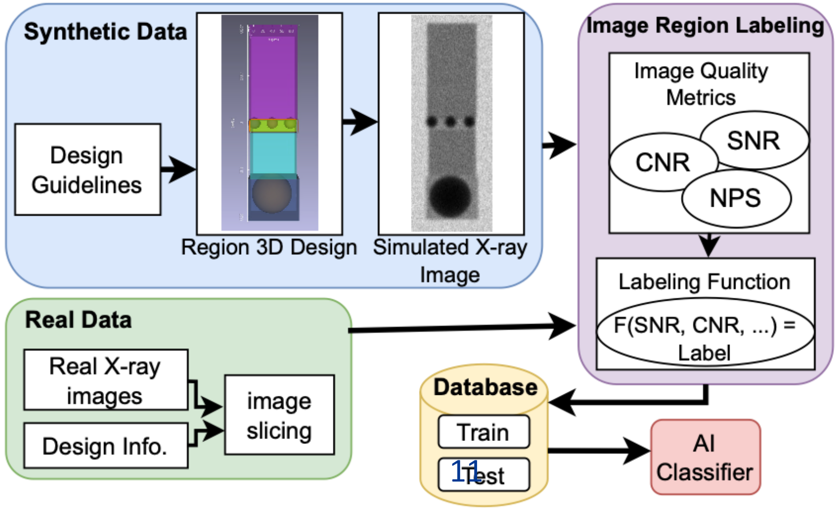
Random Forest prediction performance

AI model	Random Forest
Accuracy	75%
Logarithmic Loss	0.52
F1 score	0.74



Parameters	Range
Microbump pitch (μm)	[20, 40]
Microbump height (μm)	[12, 27]
Microbump underfill density (g/cm^3)	[1.8, 2]
Interposer thickness (μm)	[50, 100]

Case study design parameters and their range.



Experimental setup

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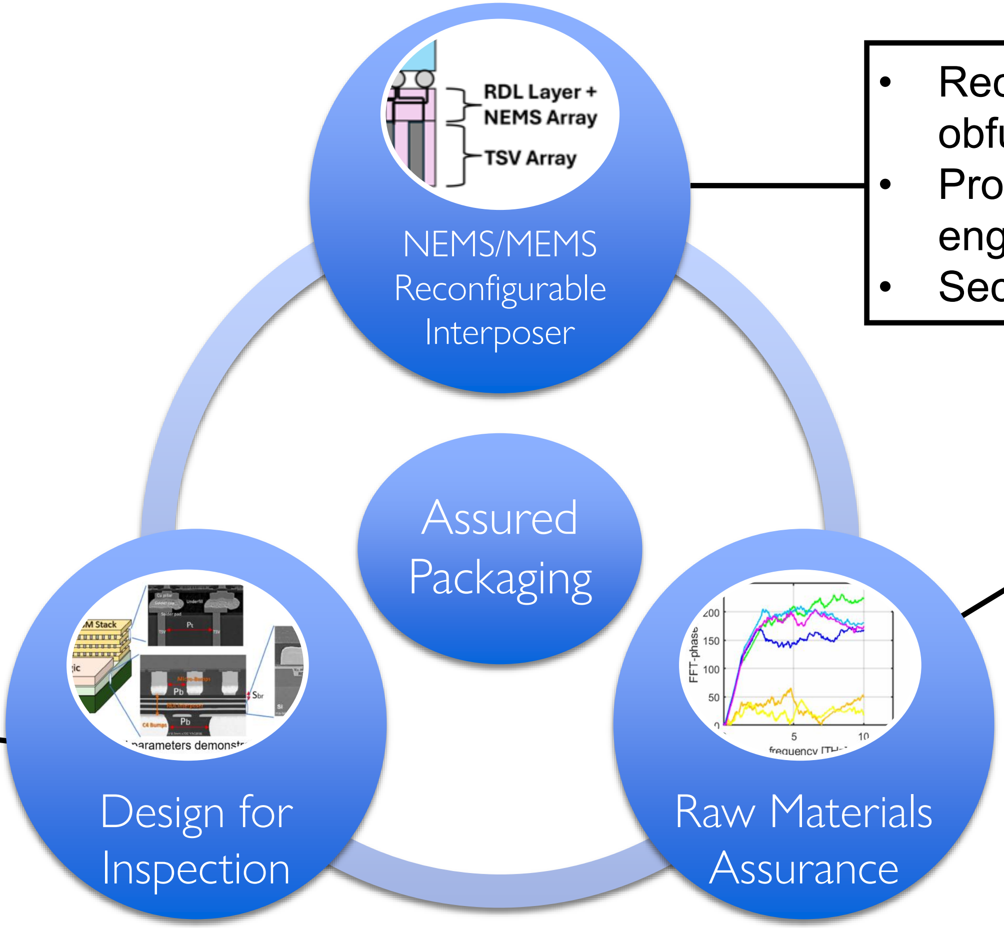

- Benchmarks material reliability for SoCs
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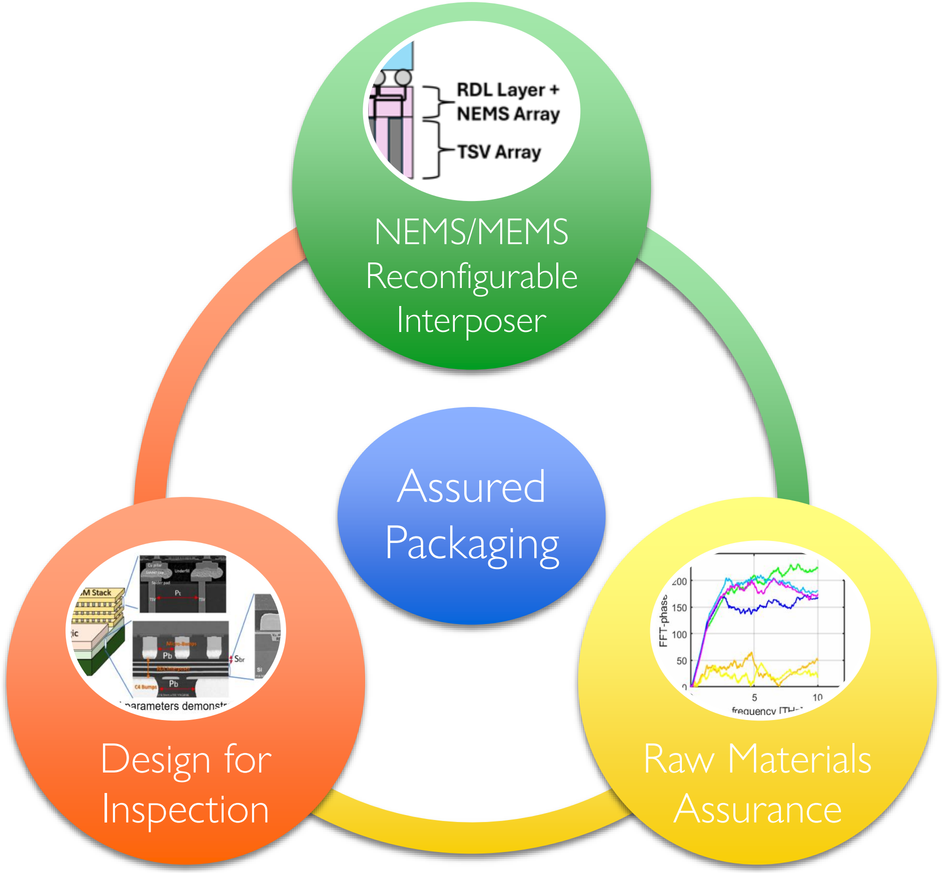
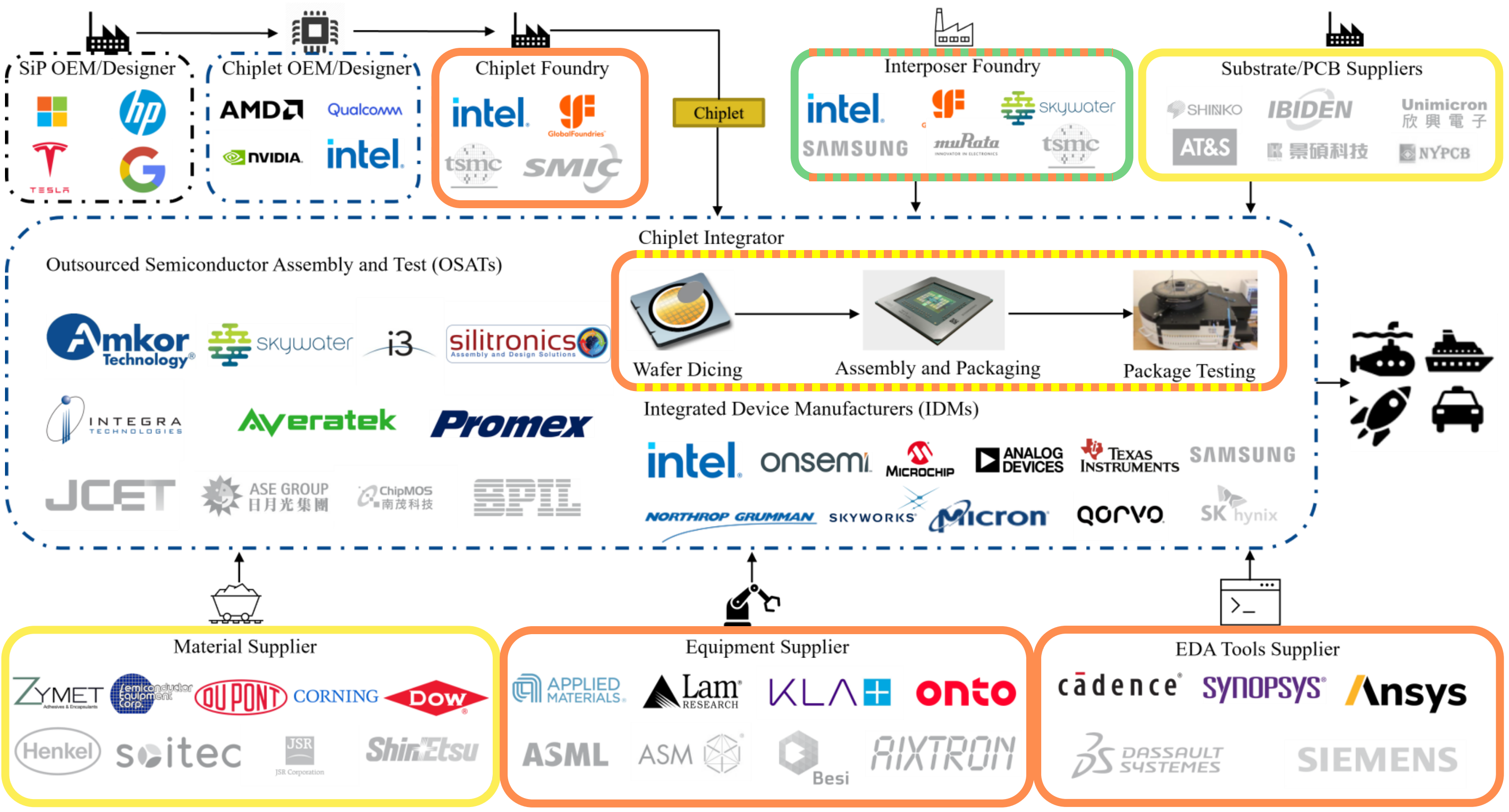
- Software outputs predictive reliability scores

Goal: Provide a multi-faceted approach to address assurance, reliability, and inspection challenges of advanced packaged SoCs.

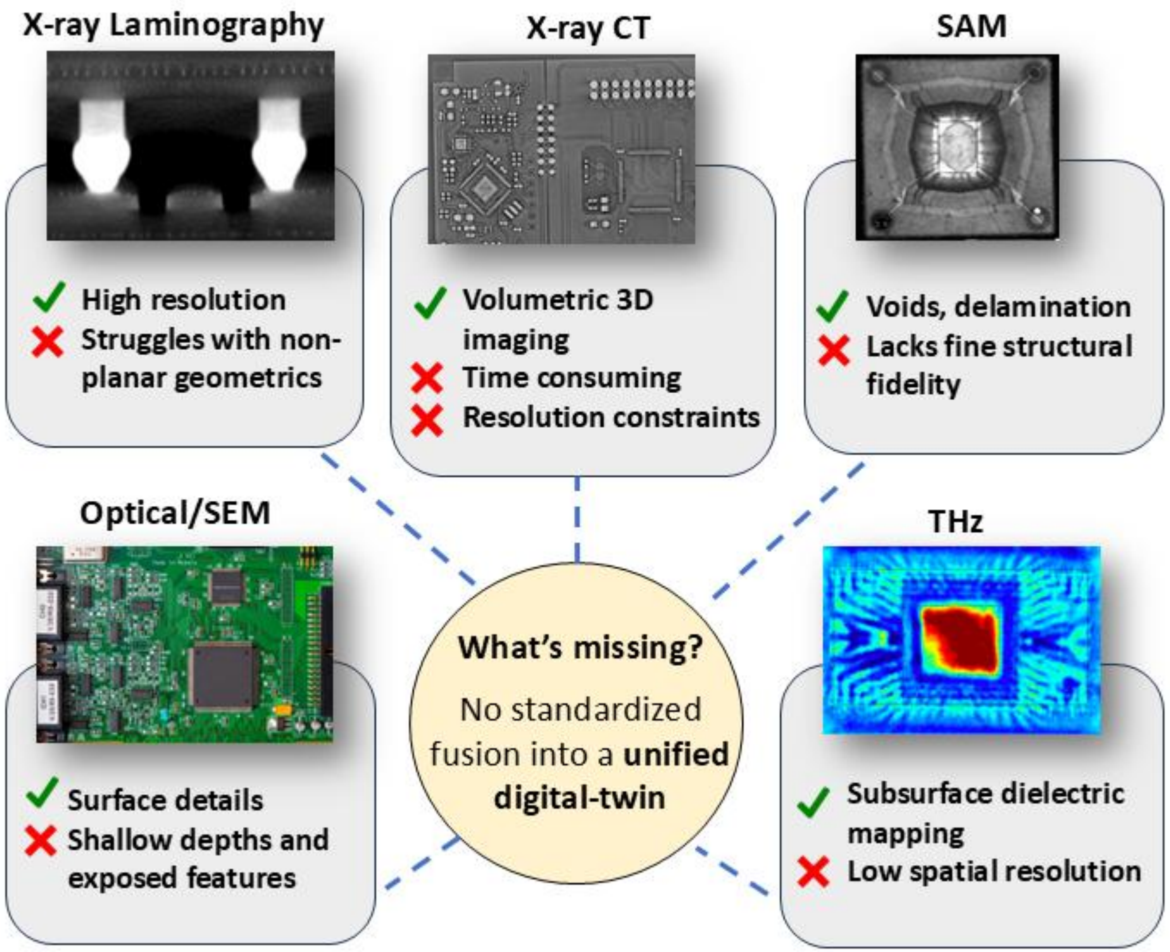
Future Application Domains of Key Areas



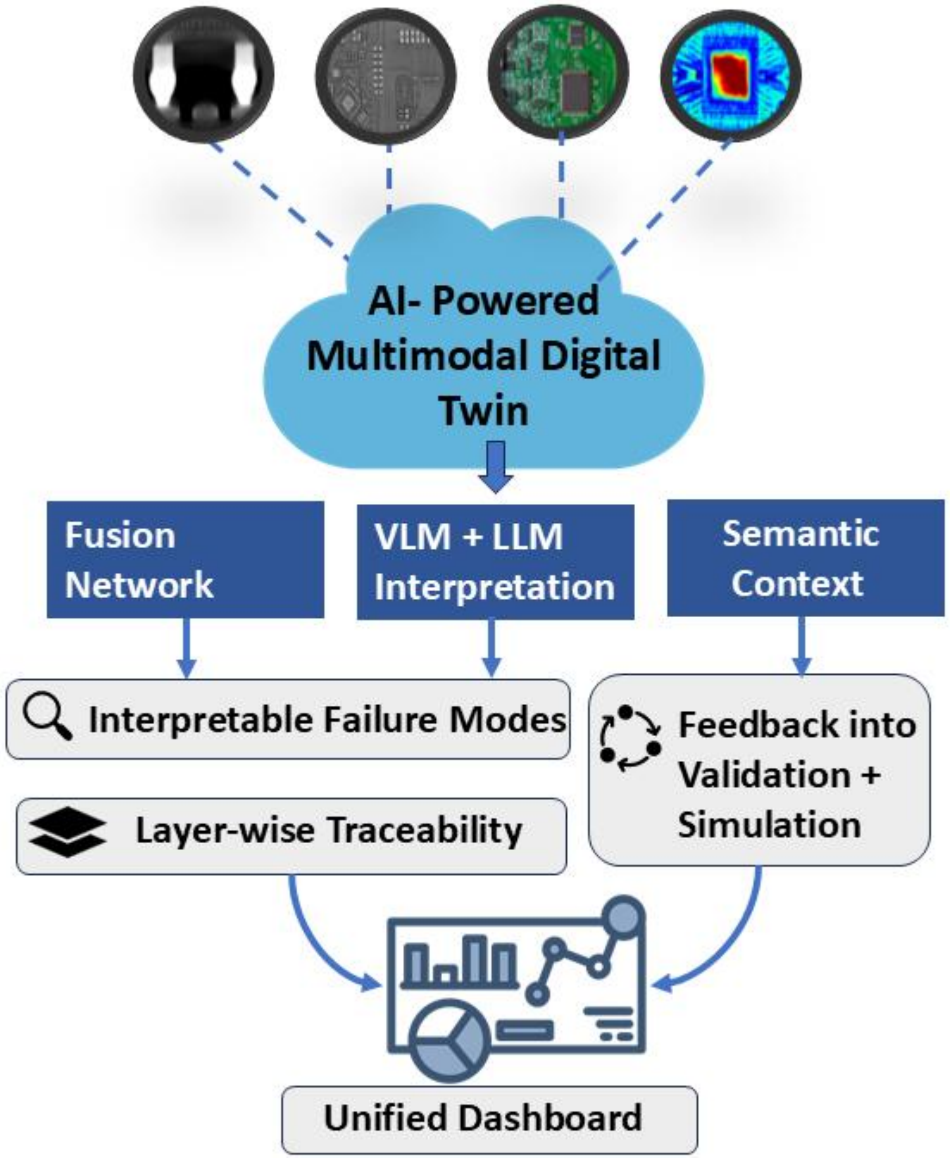


- Integration with existing workflows from target portions of the supply chain
- Further develop frameworks with additional microscopy techniques and tooling

Future Work: Multimodal Digital Twin

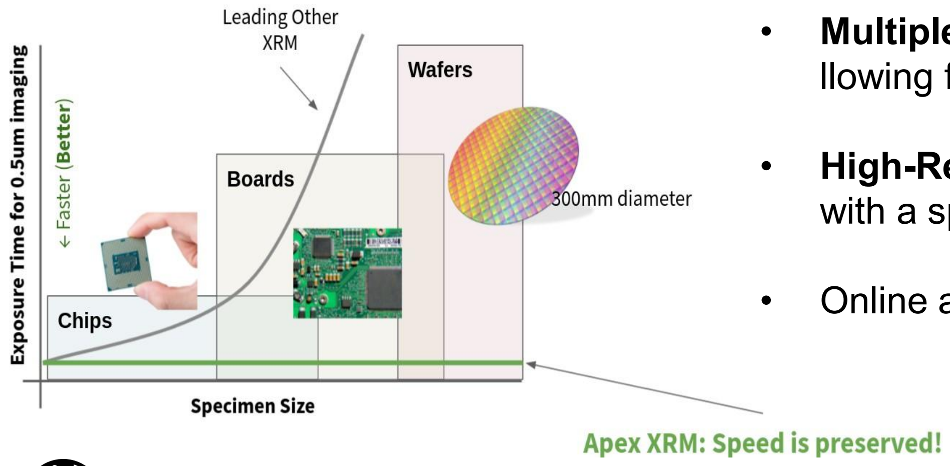


Limitations:
- Single Modality
- Isolated Tools
- Expert Dependent
- Manual Analysis

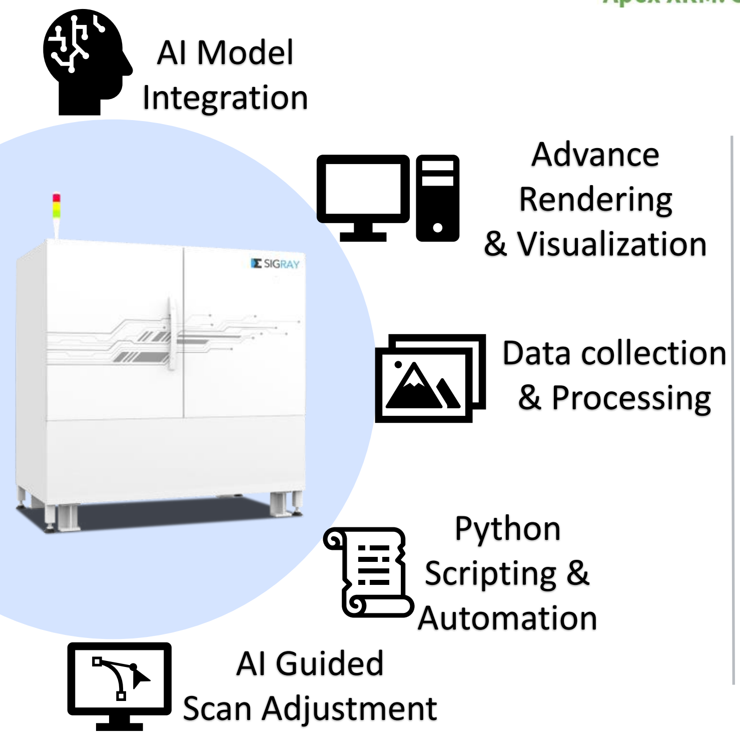


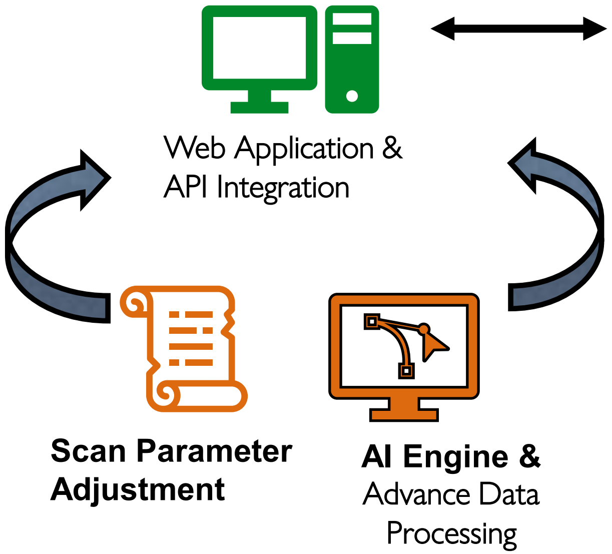
Physical Inspection: Security and Assurance Laboratory

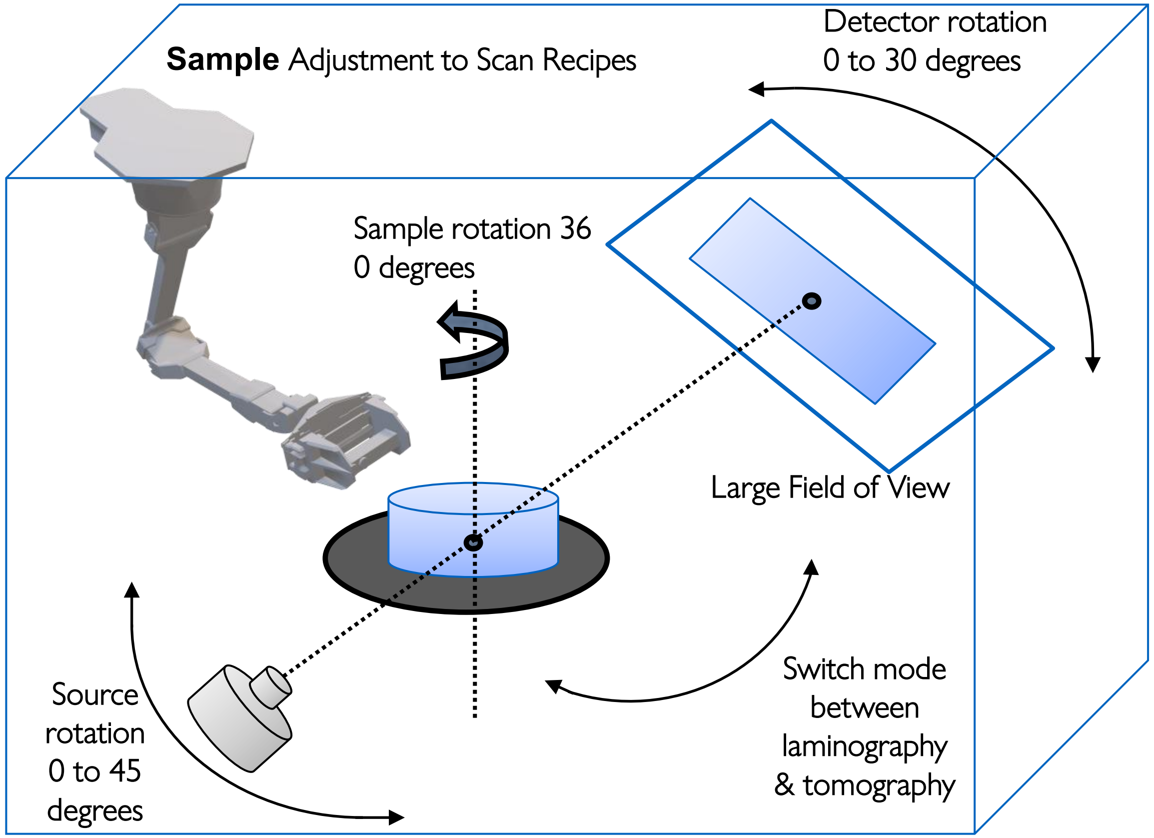
Sigray Apex Hybrid Imaging System



- **Multiple Scanning Geometries** – Supports both laminographic and tomographic X-ray scanning, a llowing for flexible imaging of complex structures.
- **High-Resolution and Fast Imaging** – Captures 3D images of samples up to 300 mm in diameter with a spatial resolution of 0.5 μm in under 15 minutes
- Online access to processing software and acquisition

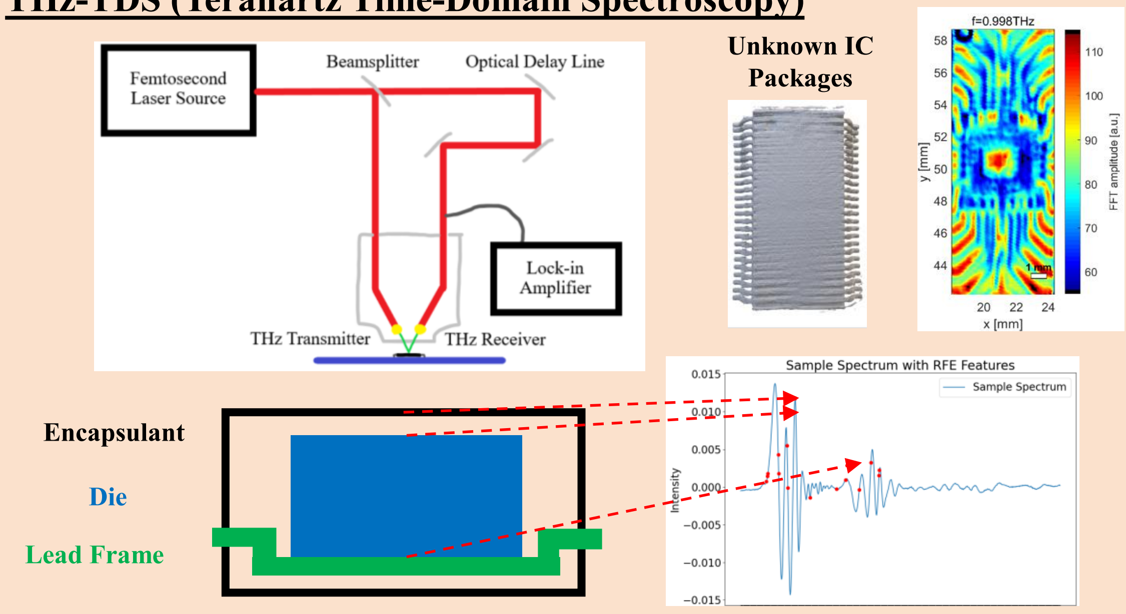




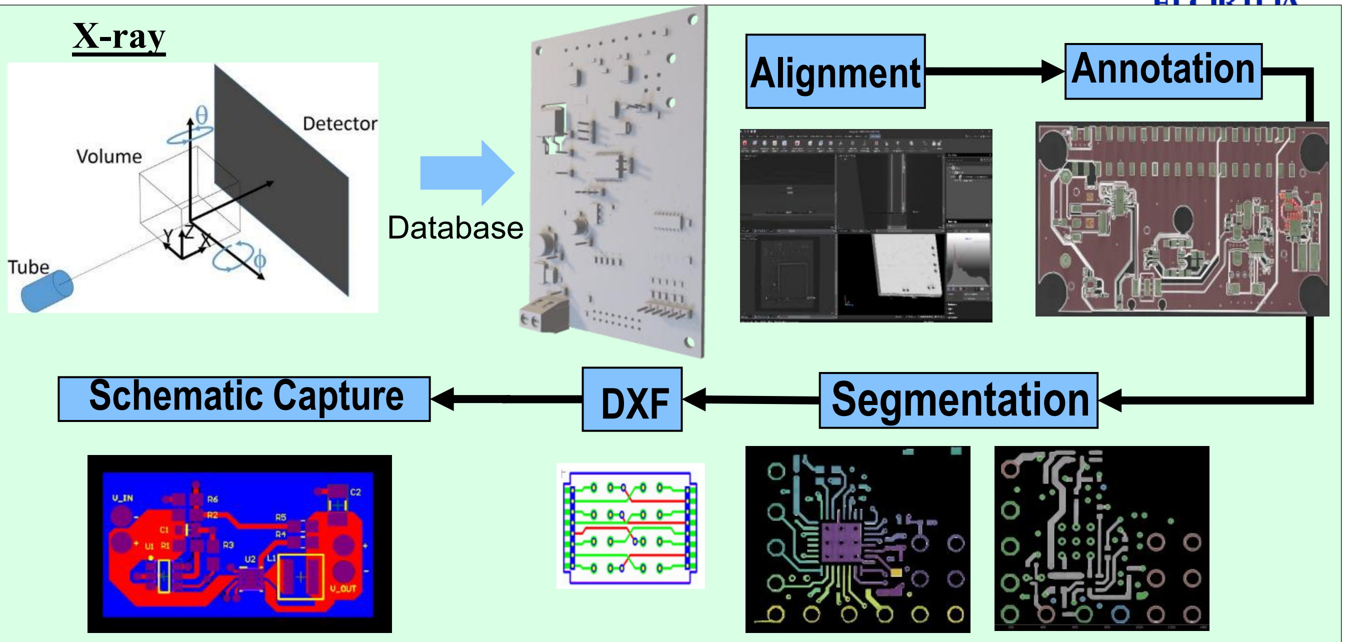


Non-Destructive Analysis Capabilities

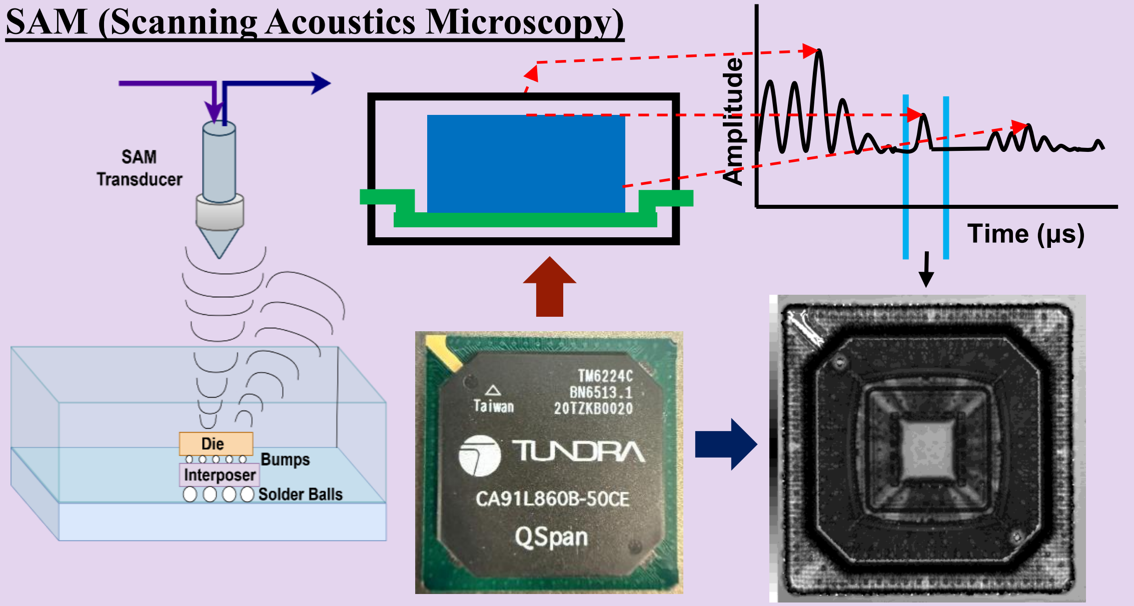
THz-TDS (Terahartz Time-Domain Spectroscopy)



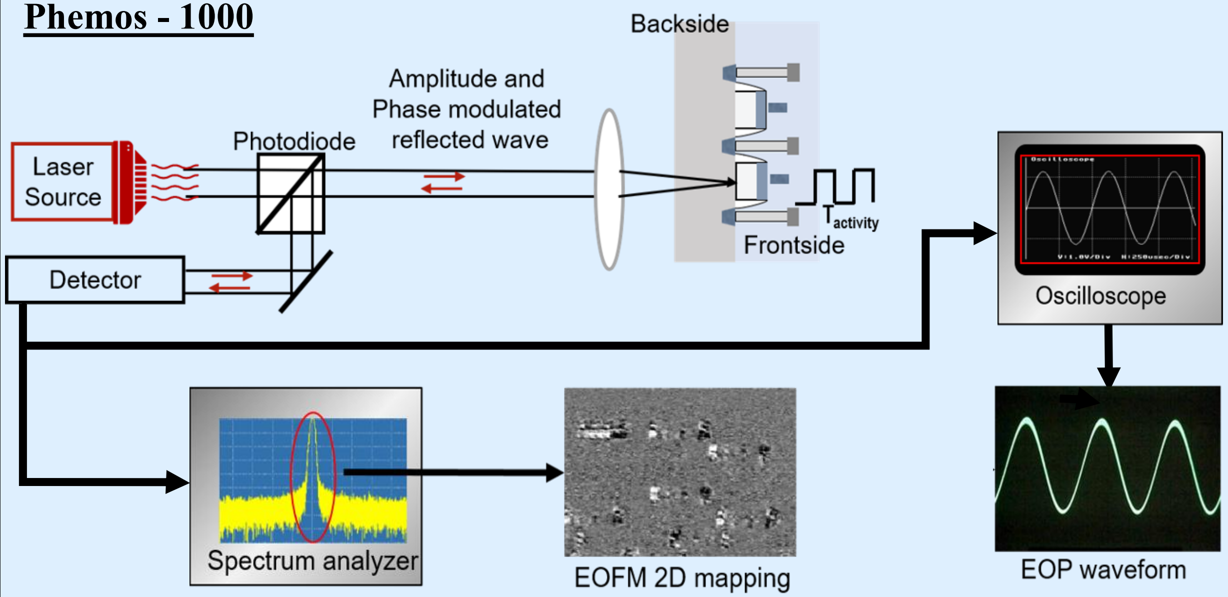
X-ray



SAM (Scanning Acoustics Microscopy)

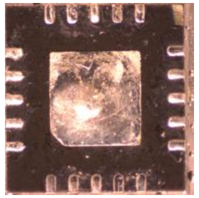


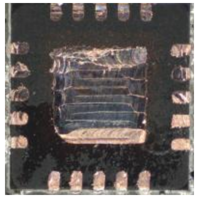
Phemos - 1000

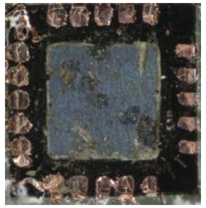


Destructive Analysis

Destructive Sample Preparation

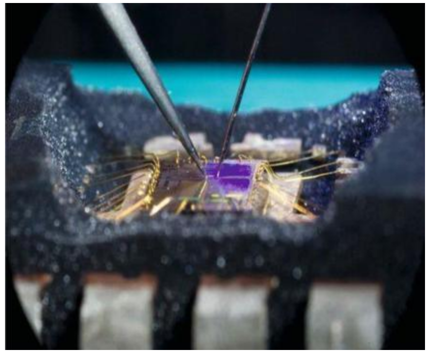

Backside Sample


Lead Frame

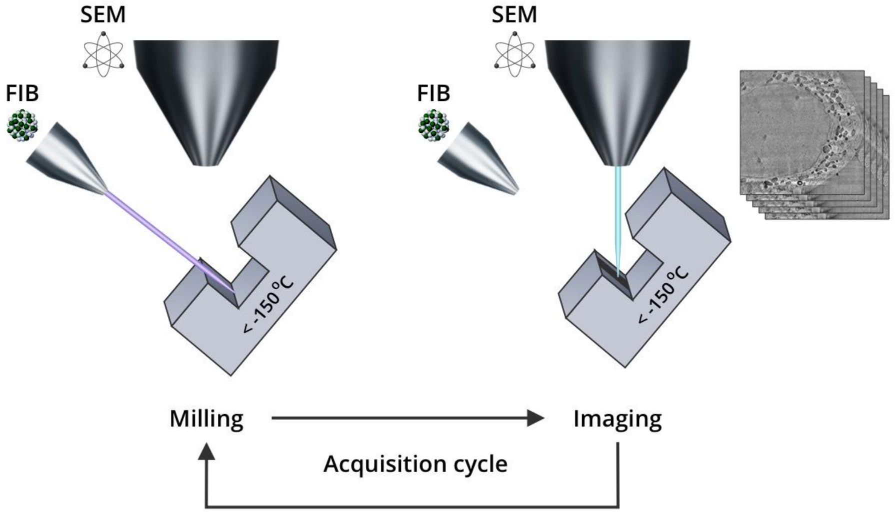

Exposed Die


Thinned Substrate

Advanced X-Prep


Wet Etching

Focused Ion Beam(FIB)



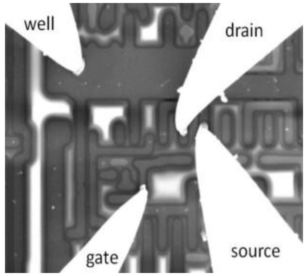
Scanning Electron Microscopy(SEM) with nano-probing

Low-res
SEM image

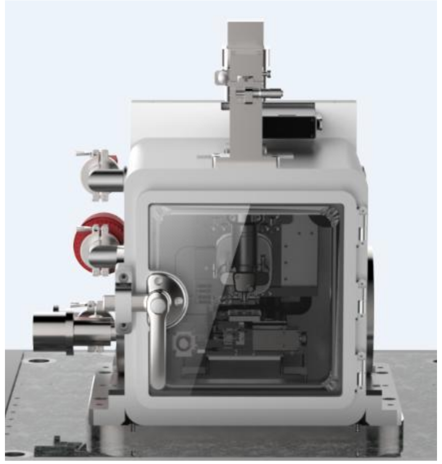
Synthesis of SEM
image with ML/AI

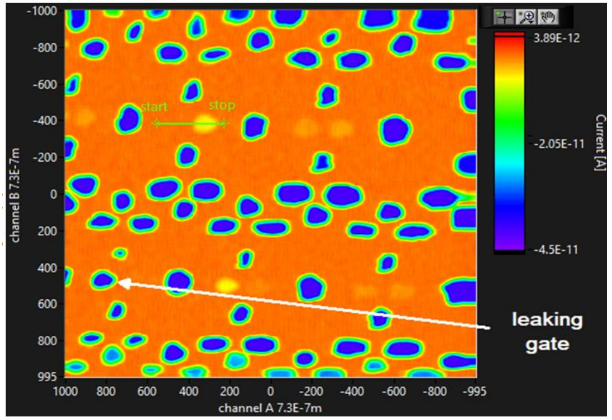
High-res
SEM image

Real time
nano probing



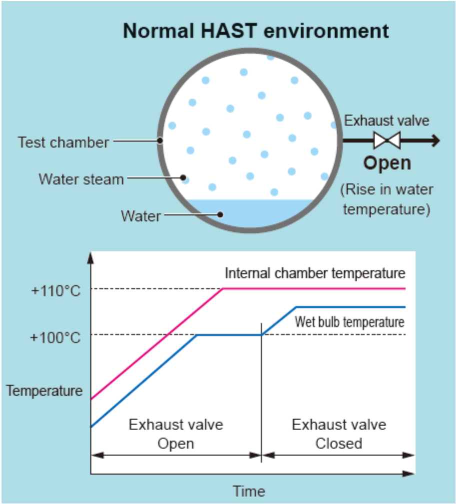
Atomic Forced Microscopy with sMIM

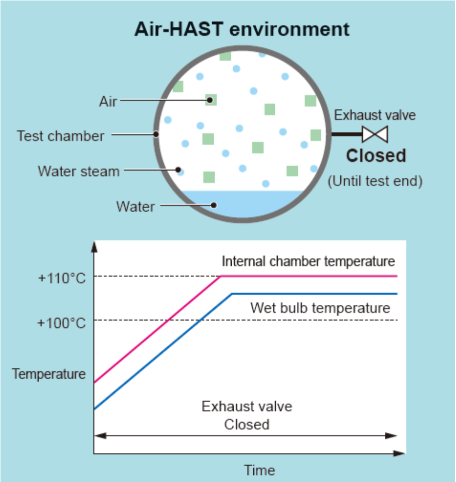




Reliability Testing Tools

HAST (Highly Accelerated Stress Test)





Temperature: **105°C to 142°C**

Humidity: **75 to 100%** RH

- ✓ Accelerates failure under **heat** and **humidity**
- ✓ Simulates **long-term aging** in short time

HOTL (High Operating Temperature Life test)

This is a **reliability stress test** conducted on electronic components (like ICs, transistors, or modules) where devices are:

- ✓ Operated under **elevated temperatures** (often 125°C or higher),
- ✓ Sometimes combined with **voltage or current bias**,
- ✓ Over an extended period (e.g., 1000 hours),
- ✓ To **accelerate aging and failure mechanisms**, such as:
  - ➢ Electromigration
  - ➢ Time-Dependent Dielectric Breakdown (TDDB)
  - ➢ Hot Carrier Injection (HCI)
  - ➢ Bias Temperature Instability (BTI)

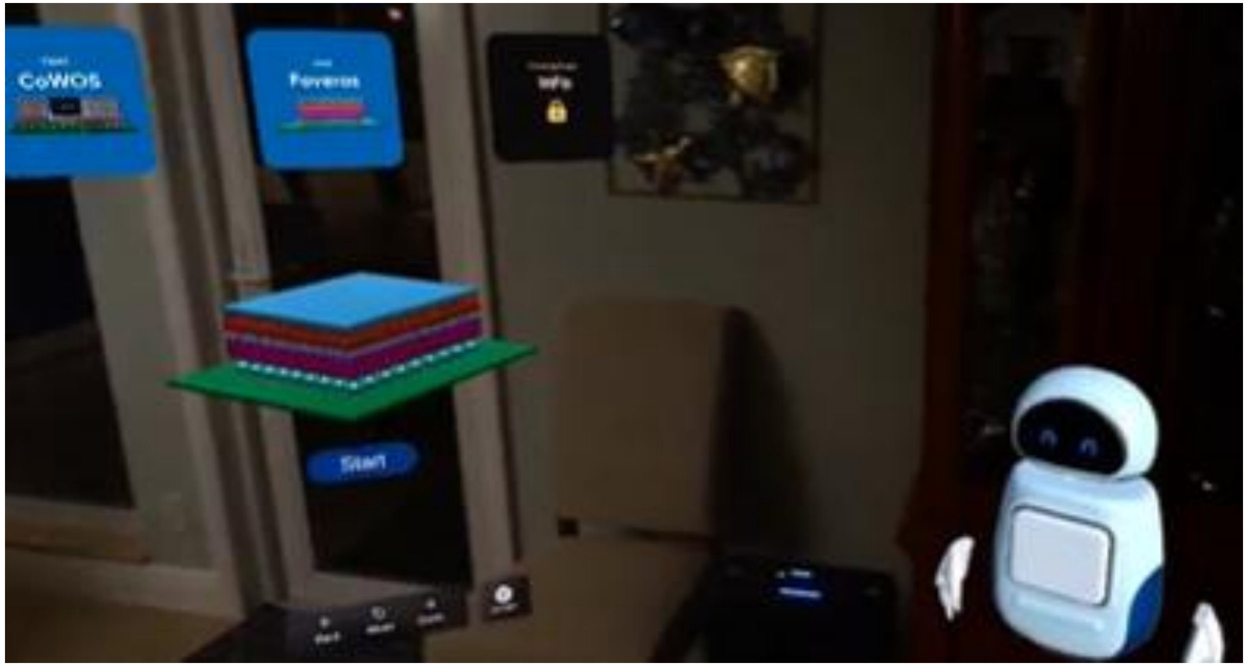
Shock/Drop Test System

- ✓ **Purpose:**
  - ➢ Simulates mechanical shock during accidental drops.
  - ➢ Evaluates the **mechanical reliability** of semiconductor packages, especially the **integrity of solder joints**
  - ➢ Helps predict field failure mechanisms like **interconnect cracking**, **die fracture**, or **package delamination**
- ✓ **Used for:** PCB assemblies, military/aerospace components.
- ✓ **Features:**
  - ➢ Controlled **drop height** (usually ~1 meter)
  - ➢ Half-sine, trapezoidal, or sawtooth waveform generation
  - ➢ High g-force capability (up to 100,000 g)
  - ➢ Includes **accelerometers** and **event detectors** to capture electrical opens or intermittent failures
  - ➢ Complies with MIL-STD and JEDEC standards

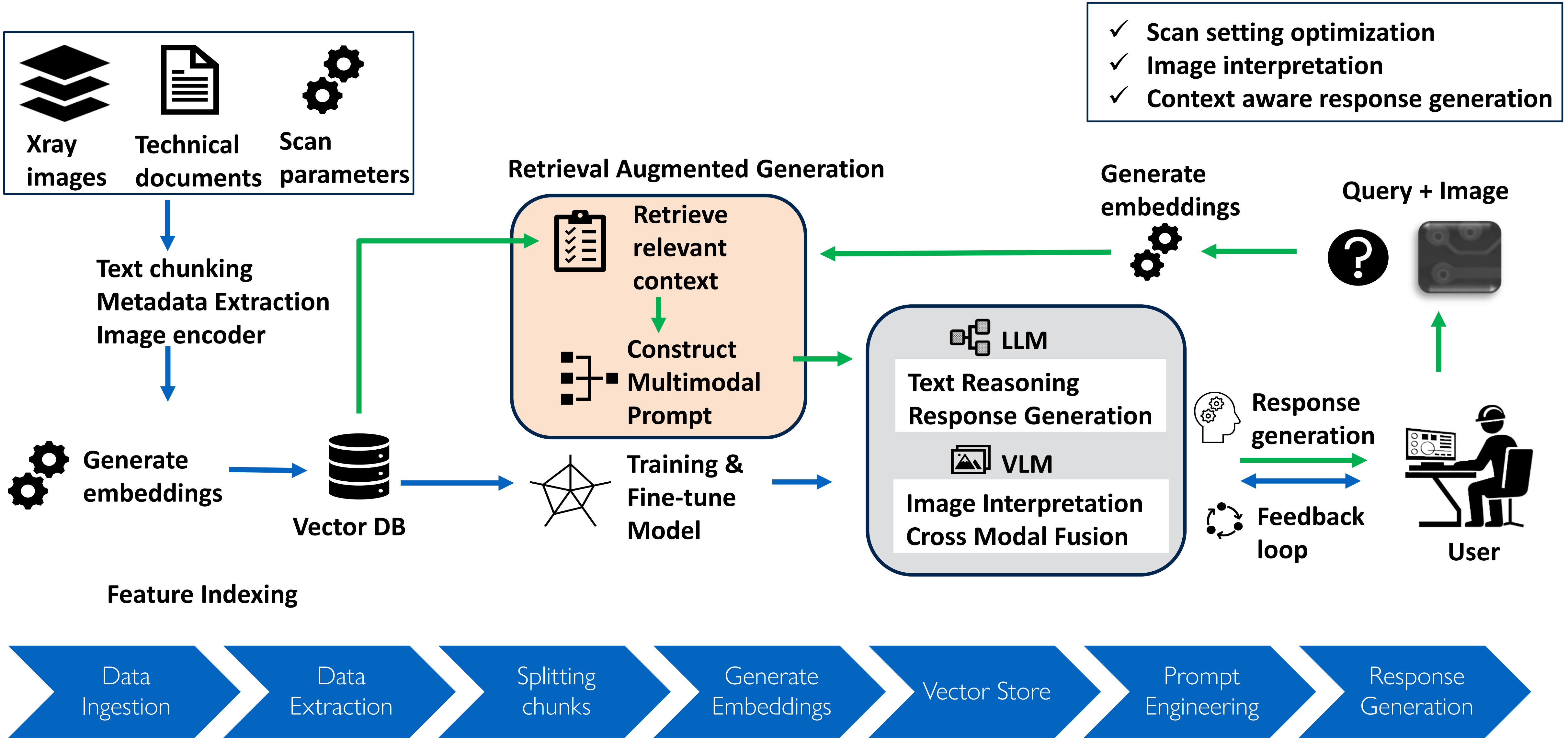
Virtual Reality Resources

Physical Assurance: X-ray tomography, optical imaging, Acoustic imaging, THz, Photon emission microscopy etc.

Advanced packaging: TSMC – CoWoS/InFo PoP, Intel Foveros, etc.



Future Work: Virtual Assistant for X-ray Inspection



Future Challenges of Assurance for Advanced Packaging

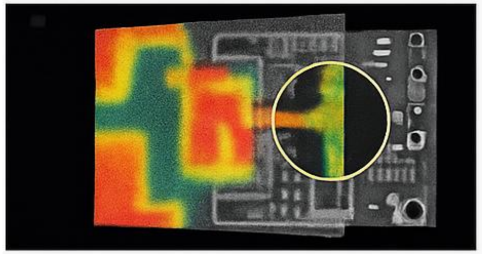
Key Challenges

Complex Inspection Process

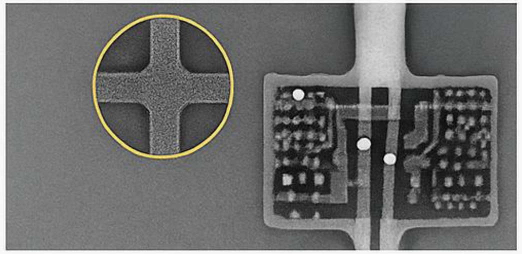
Reliable Inspection

Data Overload

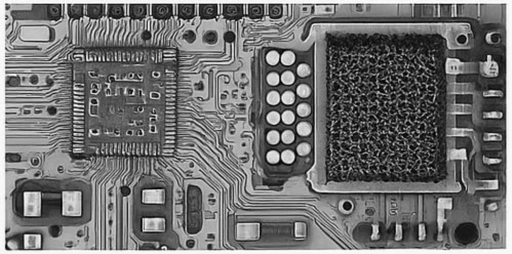
Dependence of Manual Inspection



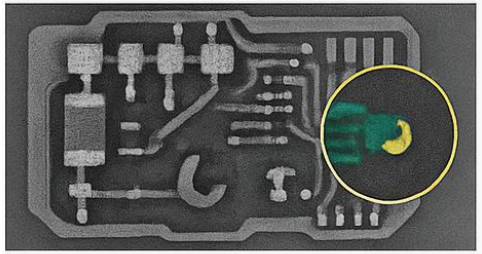
Multimodal imaging faces alignment issues and incomplete defect coverage



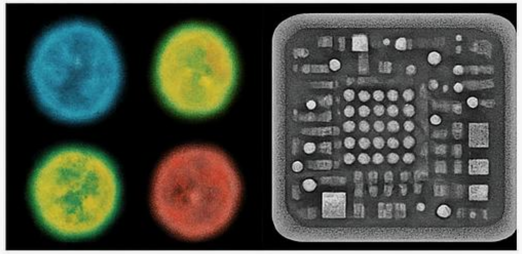
Meta-conductor materials still introduce scattering in dense areas



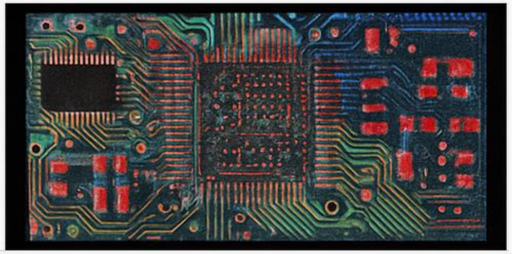
DFI is rarely applied early, limiting system transparency by design



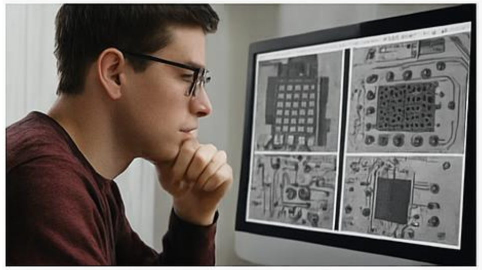
Mode switching may miss defects in complex or buried regions



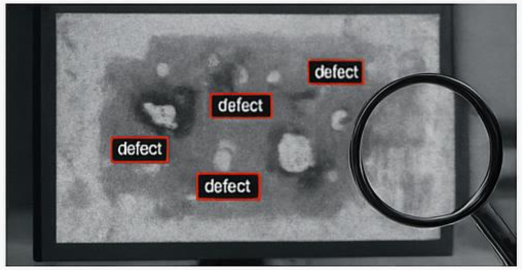
Material property variation causes imaging inconsistency



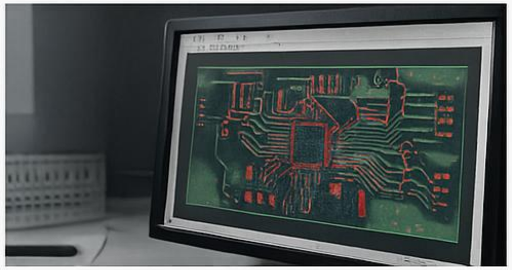
High-res multimodal scans generate excessive, hard-to-process data



Multimodal data interpretation still relies on expert review



AI models require manual labeling, especially for novel materials.



Poor design-inspection integration sustains manual effort

Advanced packaging assurance faces challenges of complex inspection, data overload, and reliance on manual interpretation, underscoring the need for more reliable and automated inspection frameworks.

Summary and Conclusion

- **What are the present vulnerabilities in the microelectronics supply chain?**
  - *Fabless & Globalized Supply Chain*: Heavy reliance on overseas fabs and third parties increases risk from geopolitical tensions and disruptions.
  - *Security & Bottlenecks*: Cross-border processes potentially expose IP, while regional concentration creates critical chokepoints.
- **How can analysis of raw materials, NEMs/MEMs interposers, and design for inspection help build trust?**
  - *Raw Materials Security Framework:* Ensures quality and authenticity from the source. Aims to forecast reliability.
  - *NEMs/MEMs Interposer:* Enhances device trust through precise integration.
  - *Design for Inspection:* Enables better inspection of heterogeneously integrated SoCs.
- **What future directions are being taken to reach total trust and increase inspection capabilities?**
  - *AI-Driven Inspection*: Enhancing detection and verification through intelligent automation.
  - *Multimodal Digital Twins*: Creating comprehensive virtual models for continuous monitoring and trust validation.

Questions?

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