Heterogeneous Integration in Florida Enabling High Bandwidth Subsystems

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The Good News: Chip Evolutions "Simplified" Our Lives

- In September 2000:
  - A good computer - Pentium 4 / 128 MB RAM / 40 GB Storage - cost about $3500.
  - If you wanted to check e-mail wirelessly, you had a Blackberry – cost about $700 + $40/month.
  - To talk on 2G cell phone, you paid by the minute and/or by the text. No camera. No data.
  - A 36" TV cost about $2000. A Garmin GPS navigation device cost about $1000.
  - A 3.3 MP camera was about $1000. A MiniDV digital camcorder was also about $1000.
- In September 2025:
  - iPhone 17 Pro Max (A19 / 12 GB RAM / 256 GB Storage) – cost $1200 + $50/month
  - Including…5G phone, text, data, GPS, a 48 MP camera, and studio quality camera (1080p + 4K Dolby)
- Reflect on how innovations in chips simplify and centralize so many functions into one technology hub

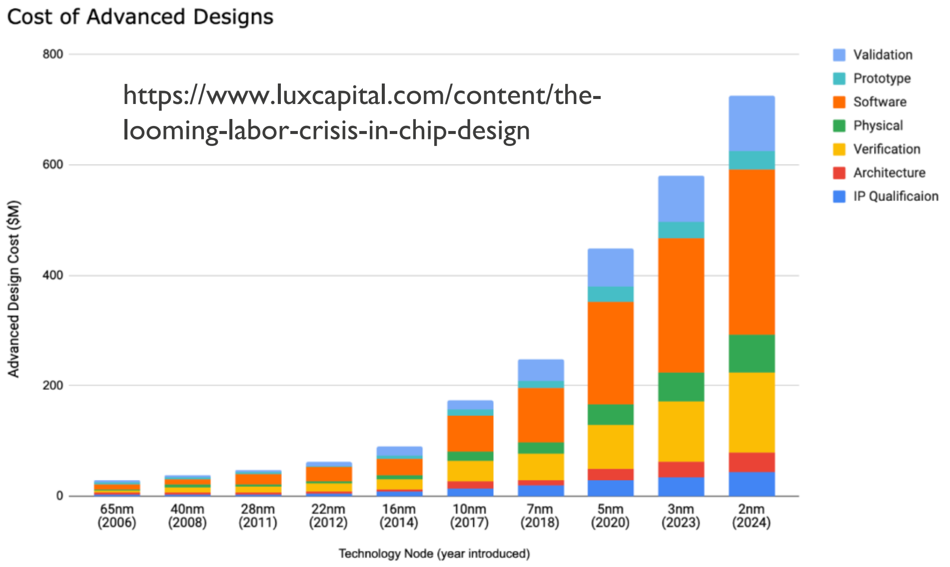







The Bad News: The Huge Bill for Chasing Moore's Law

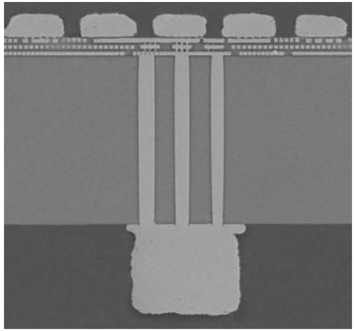
- More functionality on one platform requires huge resources to manage the system complexity. This increases the barrier of entry for new innovations.
- To build a modern semiconductor fab, it requires tens of billions of dollars. This level of investment is only possible by huge involvement at the level of nation-states.
- More daunting, simply creating a design to feed these new fabs requires investment of 100's of millions of dollars per design
- Do we really want nation states and oligarch led cartels to dictate the future of technology?
- Many movies were made about how this might turn out for society. None of them paint a positive picture of the future.

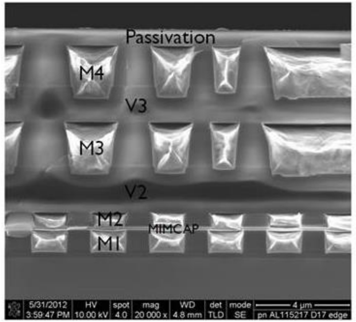


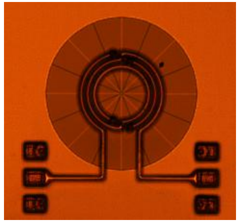
Design by Dario Soatto combining data from International Business Strategies.

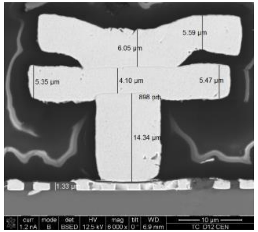
Silicon Interposers for Heterogeneous Integration

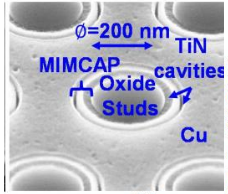
- New High Bandwidth Solutions Start as Low-Volume, High Mix
- Required Modules for Any Interposer:
  - Thru Silicon Vias (TSV) – 25-year history of advancements at imec
  - BEOL Metallization – Damascene Cu process is common
  - Interconnect – UBM with micro-bumps
- Differentiators for High Bandwidth Capability:
  - Fine Pitch Digital Interconnect (1 um L/S)
  - Embedded Passives
    - 2D MIMCAPs (for plane decoupling)
    - 2D Shielded high Q inductors (L~3 nH; Q~40)
    - 2.5 D MIMCAPs (additional decoupling)
  - Low Loss RDL layers (10 um L/S)
    - BCB material layers up to 25 um thick
    - Minimizes loss at high frequencies











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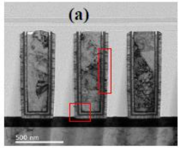


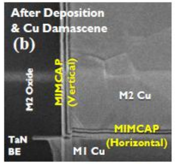
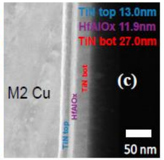
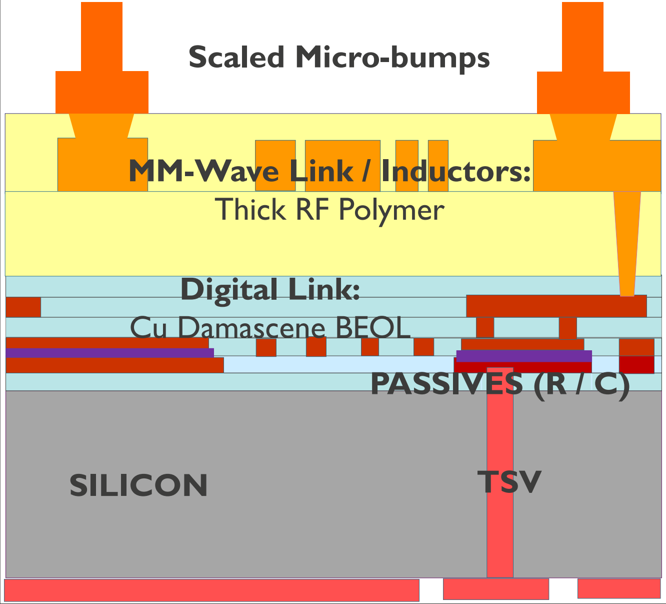


Fig. 4. TEMs for 2.5D Mimcap: (a) Mimcap pillars, (b) general zoom-in of the partial bottom and sidewall (c) zoom-in of the vertical sidewall with key parameters measured shown. The following 2D Mimcap is assumed with the same parameters. The 2.5D Mimcap also has oxide stud height, radius, and pitch of 1 um, 0.1 um and 0.45 um respectively (not shown here).



imec Interposer for High Bandwidth Applications

FIVE KEY TECHNOLOGY MODULES



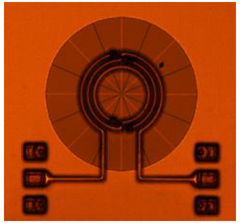
High Frequency Chip Interconnects

MM-Wave Connections
Density: 10um / 10um
BW ~ 300 GHz

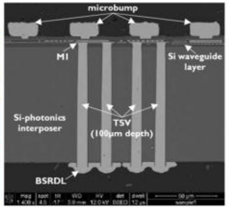
Digital Connections
Density: 1um / 1um
BW ~ 3 GHz

Integrated Passives

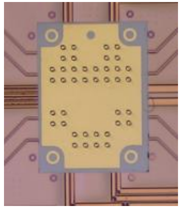
Wafer Thinning and Stacking



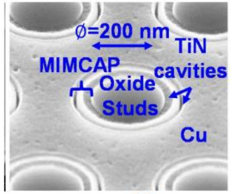
High Q inductor



High Aspect Ratio TSV



III-V Chiplet



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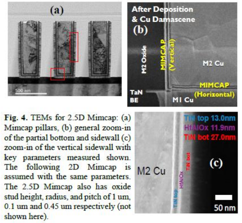

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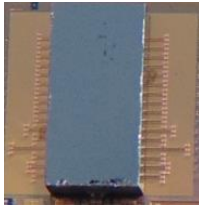
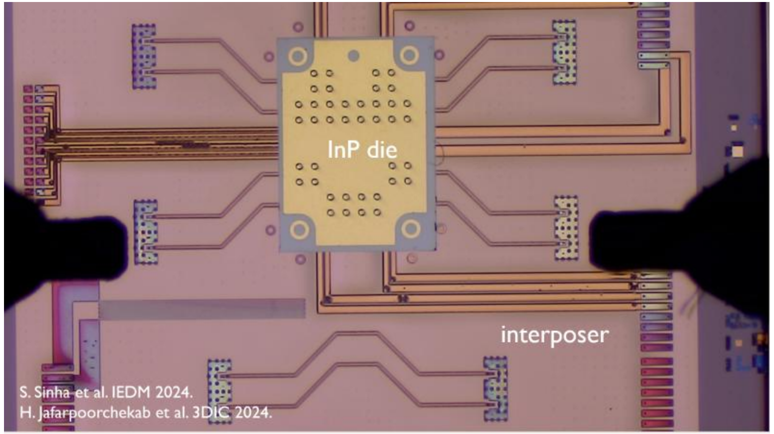
High Density MIMCAP



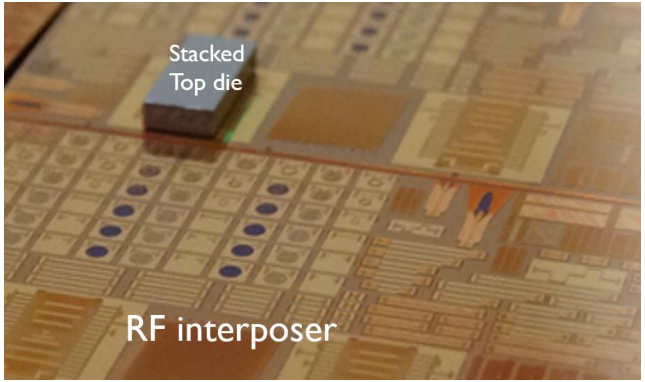
CMOS Chiplet

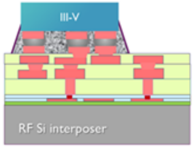
- **IEEE VLSI 2021:** H.Lin et. al., 91.5%-Efficiency Fully Integrated Voltage Regulator with 86fF/µm^2-High-Density 2.5D MIM Capacitor
- **IEEE ECTC 2022 :** X. Sun et. al., *Cost-effective RF interposer platform on low-resistivity Si enabling heterogeneous integration opportunities*
- **IEEE VLSI 2022 :** R. Chen et. al., Backside PDN and 2.5D MIMCAP to Double Boost 2D and 3D ICs IR-Drop beyond 2nm Node
- **IEEE IEDM 2024 :** S. Sinha et. al., *Hetero-integration of InP Chiplets on a 300 mm RF Silicon Interposer for mm-wave Applications*
- **IEEE ECTC 2025 :** X. Sun et. al., *RF Si interposer platform for chiplets based heterogenous systems*

Key Published Results from imec Heterogeneous Integration



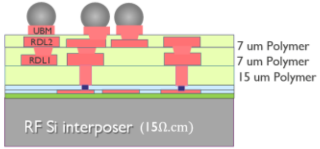
Performance Shines Brighter As Frequency Increases



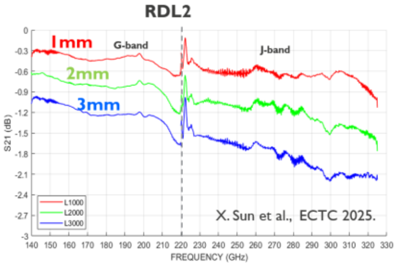


Technology / Material	HDI PCB	IC Substrate + mSAP	RF-Interposer
Routing Layers	6 – 8	4 – 8	2 – 4
Trace / Space	50 um / 50 µm	10 µm / 10 µm	5 µm / 5 µm
Layer thickness	50 – 250 µm	10 – 30 µm	5 - 20µm
Bump pitch	200 um	80 – 120 µm	20 - 40 µm
Flip-chip Freq.	170 GHz	300 GHz	500 GHz
Flip-chip area	600 x 600 µm²	300 x 300 µm²	150 x 150 µm²
Flip-chip Loss @ 150 GHz	1 dB	0.5 dB	0.2 dB
Line Loss @ 150 GHz	0.3 dB/mm	0.4-0.5 dB/mm	0.3 dB/mm

- ✓ Excellent RF interconnect performance
- ✓ Fine pitch flip-chip (< 40 µm)
- ✓ Denser low loss interconnect
- ✓ Enable small antenna array pitch at 140 GHz and above
- ✓ Small Cu surface roughness
- ✓ Integrated decoupling MIMCAP in addition to on-chip decoupling
- ✓ Integrated high Q passives and matching network



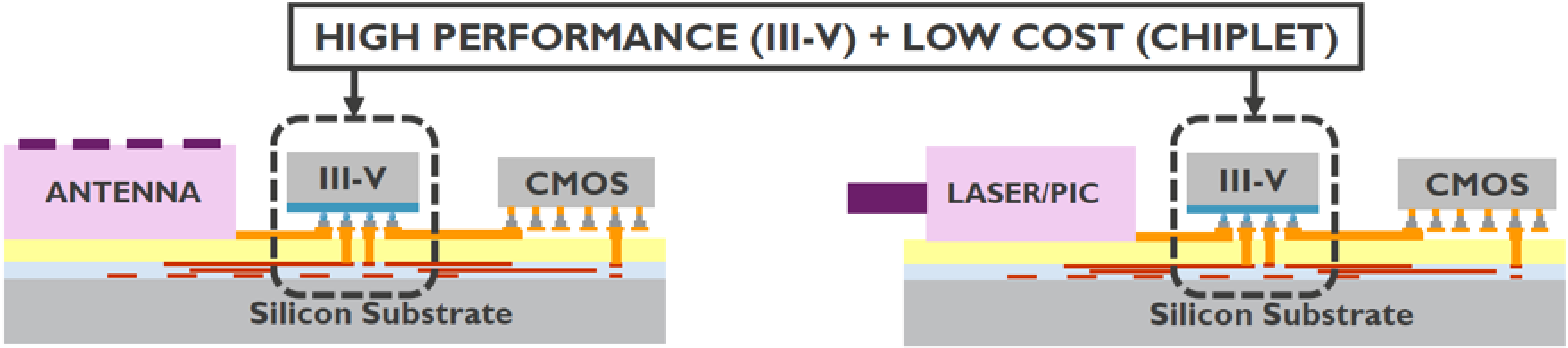
Loss @Freq	140GHz	220GHz	320GHz
imec RDL1	0.32 dB/mm	0.6 dB/mm	0.9 dB/mm
imec RDL2	0.23 dB/mm	0.5 dB/mm	0.78 dB/mm
Glass interposer [1]	0.78 dB/mm @ 80 GHz (Glass interposer)		
Epoxy mold compound [2]	250 µm interconnect length: 1.8 dB@240GHz; 4dB @300 GHz		



RF Si interposer demonstrates < 1dB/mm loss over 300GHz bandwidth

1: "Die-Embedded Glass Interposer with Minimum Warpage for 5G/6G Applications", 2023 ECTC, Georgia Institute of Technology
2: "A Low-Loss DC-to-300 GHz InP/Si Interconnection Based on Wafer Level Packaging Using Chip-first/Facedown Process", Microwave Symposium - IMS 2024

Target Applications for imec Interposer Heterogeneous Integration



WIRELESS (Communication/Radar)

CMOS : Beamformer

III-V : Power Amplifier

Antenna

Phased Array Pitch ~ 1mm

2D Scalable Array with III-V

Low Loss mm-wave distribution

Thermal Management

WIRELINE (Datacenter/HPC/Optical)

CMOS : DAC/ADC

III-V : Driver / TIA

Laser/PIC

Very Wide bandwidth interconnects

DC – 300 GHz and beyond

High Speed digital ADC / DAC

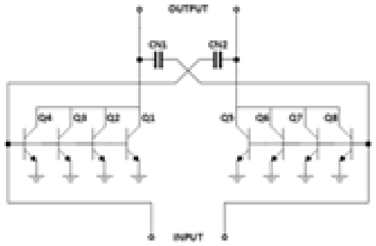
Photonic Components

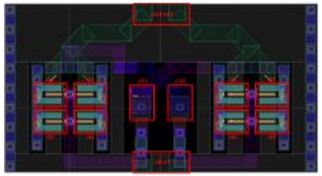
The Goal: Heterogeneous Integration In Florida

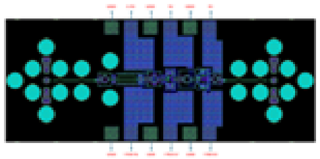
- imec RF interposer technology being stood up at NeoCity fab
- Building up Florida based design capabilities with help from NSF and imec HQ
- Goal: A Transceiver Subsystem at D-Band (140 GHz)
- Gaps to Fill: Need design, fabrication, and packaging capabilities at Neocity
    - Currently: Module design underway
        - III-V power amplifier taped out in July 2025 (Teledyne 250 nm InP)
        - Advanced CMOS (GF 22 nm FDX+) tape out scheduled for January 2026
    - Next Step (pending funding): Co-design with interposer
        - Design interposer based on emerging NeoCity fab capabilities
        - Package, test, and validate local capability
    - Then…work with OEM partner to realize US fabricated transceiver design
        - D-Band applications are in early stages now
        - Will be nicely positioned to address early demand at this point

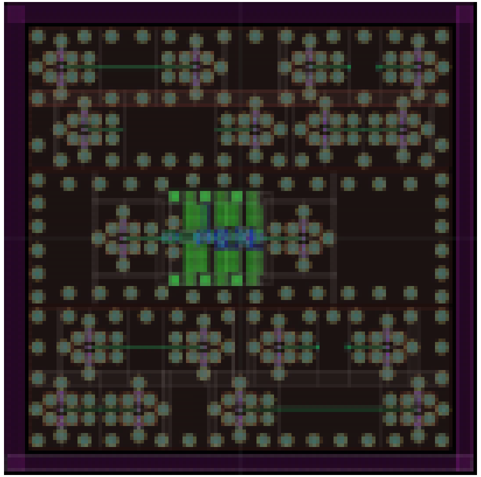
Power Amplifier (PA) Design

- Florida based design capability in III-V semiconductors is now online at FSE.
- Meysam Asghari – PhD from University in Florida.
- Two-stage common emitter design in 250 nm Teledyne Indium Phosphide (InP).
- Design optimized at 140 GHz. To be measured over 110-170 GHz and 170-260 GHz bands.
- Currently taped out and being manufactured by Teledyne



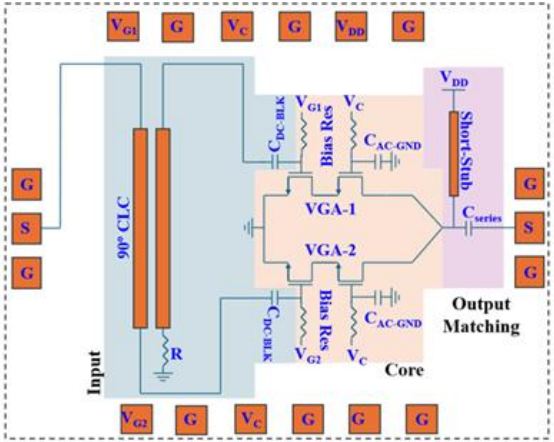


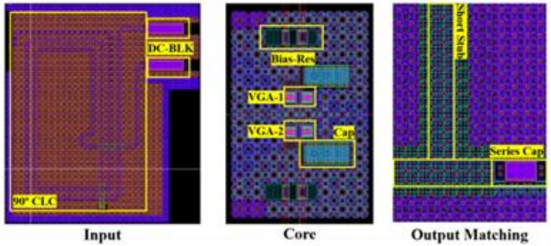




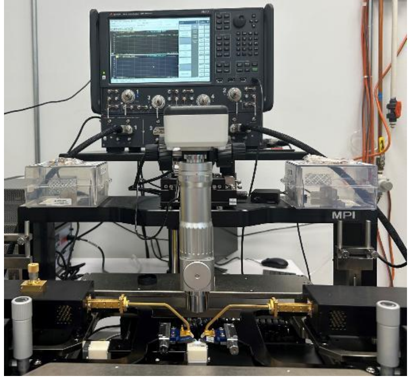
Phase Shifter (PS) Design

- Florida-based design capability for advanced CMOS is now online at FSE.
- Shah Zaib Aslam– PhD candidate from University in Florida.
- Active phase shifter is fundamental to beamforming for RF transceiver.
- Designed in GlobalFoundries 22 nm FDX+ advanced CMOS.
- Design defined and layout taking shape for active chip.
- Will also include test structures to characterize assembly to RF interposer.
- Structures to be designed considering Florida assembly capabilities.
- Tapeout in January with flip passive flip chips for RF characterization.

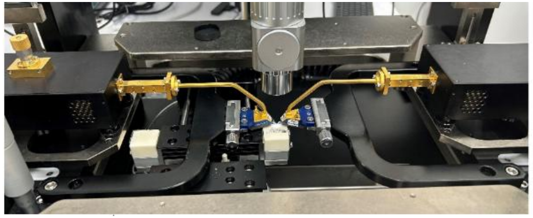


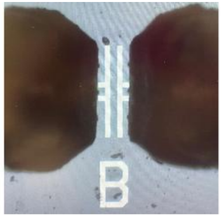


Current millimeter wave test capabilities



- Setup for probed measurements in D-band (110 – 170 GHz) shown.
- North-South positioners for on-chip biasing on hand and multi-contact probes arrive next week.
- G-band (170 – 260 GHz) test capabilities on order and scheduled to be live by the end of the year.





Baseline Plan for Next Phase (Pending Funding)

- **Currently funded through February to have component-level capabilities.**
  - Fully designed and characterized InP power amplifier optimized for D-Band.
  - Advanced CMOS active phase shifter design (building block for beamforming).
  - Production representative advanced CMOS structures for interconnect design characterization.
- **2026 focus: Florida design, bumping, and bondig of RF interposer made in imec Belgium.**
  - For chiplets in two different technologies: Advanced CMOS chiplets designed for assembly to interposer manufactured in imec Belgium.
  - RF interposer manufacturing capabilities development in Florida is separate parallel scope.
  - Understand the impact optimized assembly process has on performance - basis for co-design.
- **2027 focus: prove out co-design capabilities in Florida.**
  - First tackle the more challenging and complex interface of interposer to advanced CMOS.
  - Then add InP power chiplet to the co-designed combined advanced CMOS / interposer.
- **2028 focus: design a functional sub-system demonstrating D-band performance.**
  - Work closely with OEM partner
  - Partners within the FSE will be prioritized

Take-Aways

- Florida has a unique opportunity to be the go-to place to participate in innovative heterogeneous integration manufacturing solutions
- The access available to imec's world class capabilities in Florida are a key differentiator
- The Florida Semiconductor Engine provides a seamless way to work together with partners from start-ups to large OEM's
- The focus of Florida semiconductor work is low volume, high mix applications

FLORIDA SEMICONDUCTOR ENGINE

Thank You!

Questions?

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