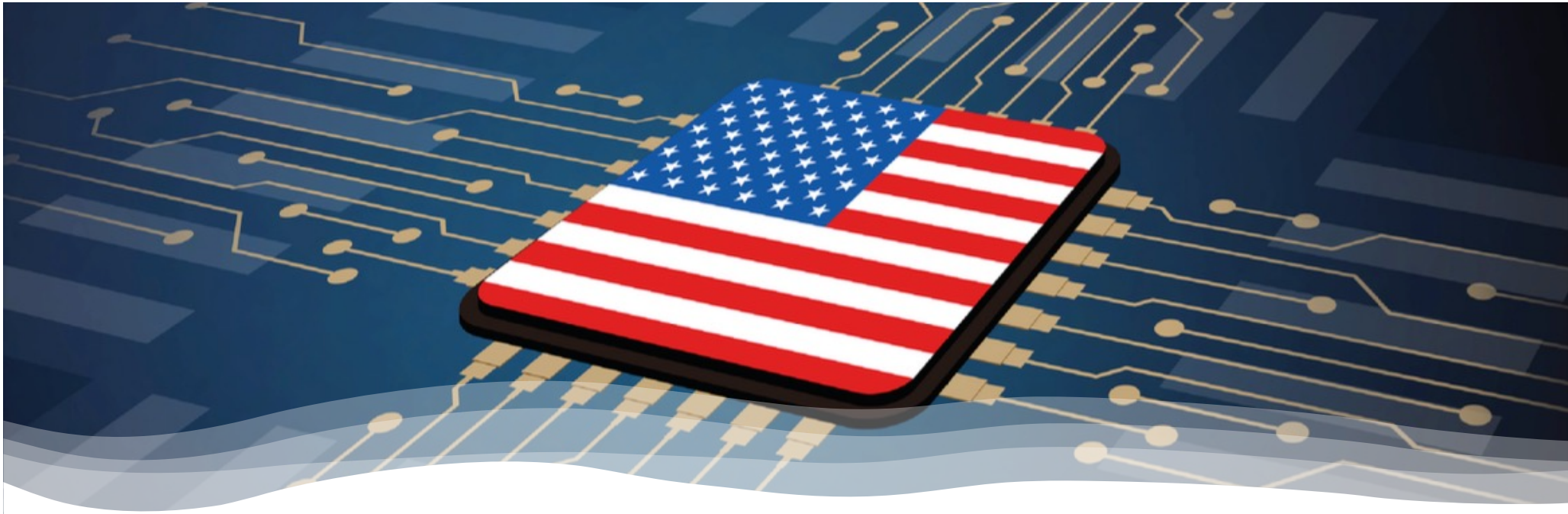




Making Florida a Microelectronics Hub: Updates on Federal & State Microelectronics Initiatives (CHIPS Act and Florida Semiconductor-Related Programs)

Prepared for International Microelectronics Assembly and Packaging Society Florida Workshop – Sept 23, 2025

Michael Aller, FloridaMakes



National Institute of Standards & Technology

- A Division of the US Department of Commerce
- National Bureau of Standards - 1901
 - Metrology: The Science of Measurement
- NIST Labs – Gaithersburg, MD & Boulder, CO
- [CHIPS Program Offices](#) – CHIPS R&D, CHIPS Metrology
- Innovation & Industry Services
 - [NIST Manufacturing Extension Partnership](#)
 - [Office of Advanced Manufacturing - Manufacturing USA Program](#)
 - [Baldrige Performance Excellence Program](#)



About the MEP National Network

NIST MEP National Network Manufacturing Extension Partnership



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it possible.



Learn more about the MEP National Network via: <https://www.nist.gov/mep/>



Mission

Strengthen and advance Florida's
manufacturing economy



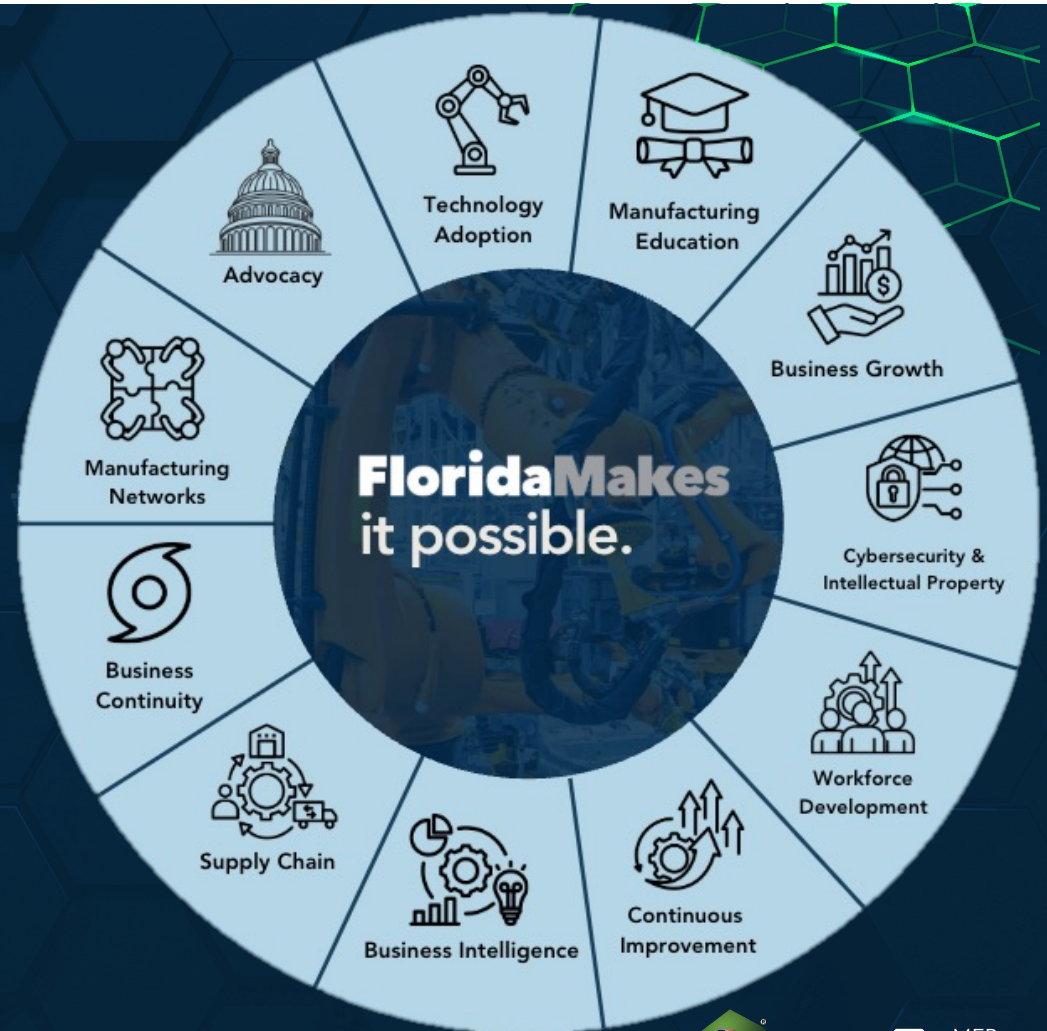
About FloridaMakes

FloridaMakes is a public-private partnership dedicated to strengthening and advancing Florida's manufacturing economy. Its goal is to deliver objective, unbiased advice and technical assistance to help manufacturers grow and become more profitable. The FloridaMakes team of manufacturing experts serves as trusted advisors, helping manufacturers navigate the public and private resources available to support their success.

FloridaMakes is the official representative of the Manufacturing Extension Partnership (MEP) National Network in the state of Florida, a program of the National Institute of Standards and Technology, an agency of the U.S. Department of Commerce.

Strengthening and Advancing Florida's Economy

FloridaMakes' Client Engagement Advisory Services are focused on helping manufacturers improve productivity, enhance technology-led performance, and leveraging valuable resources through our statewide and national networks.



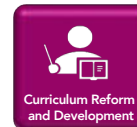
Manufacturing Education

The Florida Advanced Technological Education Center (FLATE), part of the FloridaMakes network, is the go-to program for manufacturing and advanced technical education, best practices and resources supporting the skilled workforce for Florida's manufacturing sectors.

FLATE provides exemplary industry partnerships, workforce opportunity, and educational synergy throughout the state of Florida by connecting industry and workforce needs to targeted educational endeavors at many community and state colleges across Florida.



FLATE Support for Florida Educators & Students



FLATE Support for Florida Manufacturers



Provide information about ET/MFG related AS college programs, career & college credit certificates, and career paths



Connect companies to colleges, Career and Technical Education high school programs



Provide resources to help prepare for MFG outreach events



Connect to Career and Technical Education high school programs



Connect to college & state university's faculty (technical subject matter experts)



Support outreach (MFG 2022) and educator professional development

flate.org

madeinflorida.org

manufacturingmattersfl.org

The Florida Advanced Technological Education Center materials are based upon work developed with funding from the National Science Foundation and revised, updated and disseminated with support from funds available under the Strengthening Career and Technical Education for the 21st Century Act of 2018 (Public Law 115-224) and the Florida Department of Education.

FLORIDA IS A MANUFACTURING STATE!

Scan the QR code to access the
digital version of this report



or visit the following link:
bit.ly/3UOMJxj



FloridaMakes
it possible.

COMPUTER & ELECTRONICS PRODUCT MANUFACTURING

Semiconductor and related microelectronics product manufacturing as well as broader electronics and communications equipment manufacturing are important elements of Florida's economy.

5TH

NATIONWIDE EMPLOYMENT

>\$3.7B

GDP GENERATED IN 2021

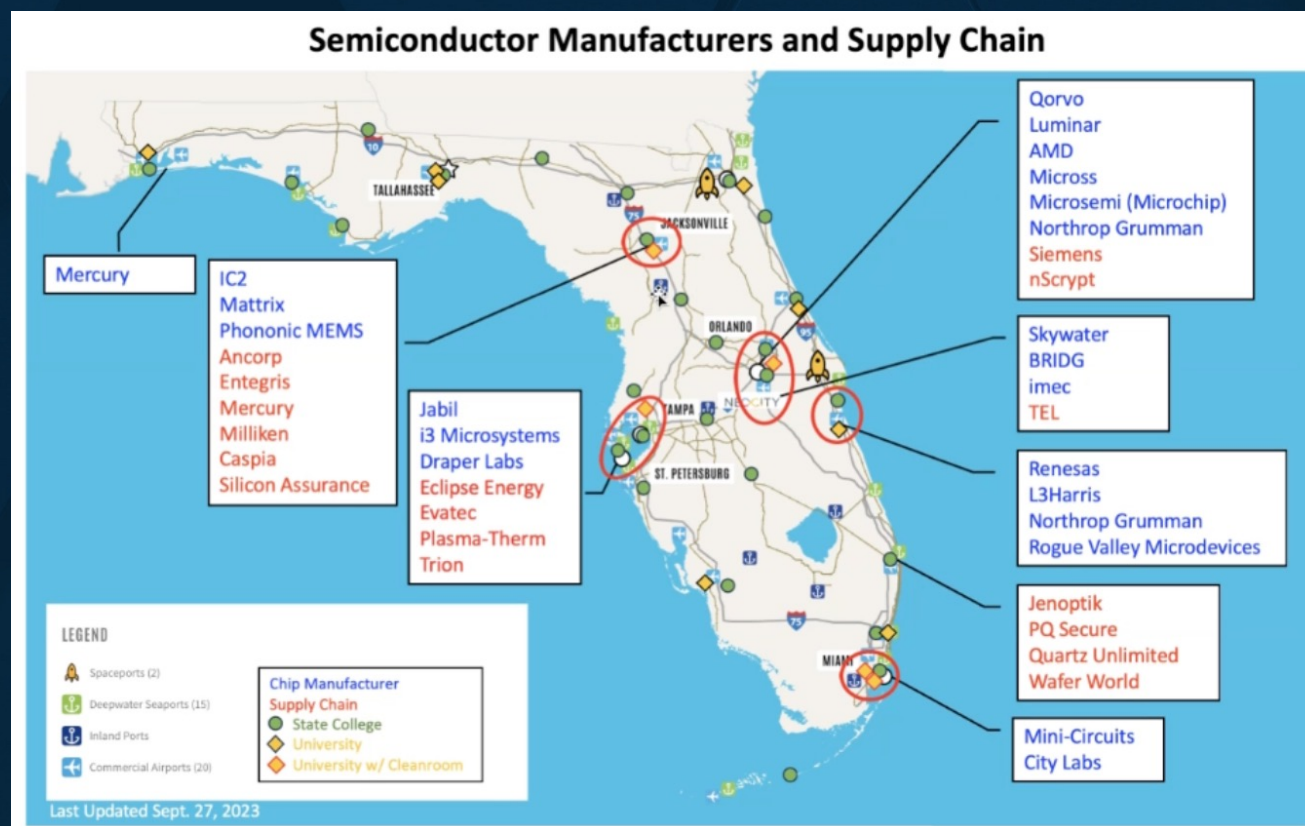
| FLORIDA MANUFACTURING 2023



MICROELECTRONICS & SEMICONDUCTORS MANUFACTURING AND SUPPLY CHAIN

FloridaMakes
it possible.

Florida has a broad and deep industry base in semiconductor and related microelectronics product manufacturing, as well as critical elements of the microelectronics supply chain. Florida's strongest "niche" is in advanced packaging of specialty electronics for the communications, aerospace and defense industries.



FLORIDAMAKES

Source: Florida Semiconductor Institute

DEFENSE MANUFACTURING

Defense Manufacturing: Florida is home to over 30,000 federal contractors, and over 25,000 manufacturers, many of which support defense.

>30K

FEDERAL CONTRACTORS

914,000

JOBS IN FLORIDA

3RD

NATIONWIDE
EMPLOYMENT

>\$21B

ANNUAL DEFENSE CONTRACTUAL SPEND



AVIATION AND AEROSPACE MANUFACTURING

Florida is a global leader in aviation and aerospace manufacturing, with over 17,000 aerospace-related companies, employing over 120,000 workers, and generating over \$19 billion in annual revenue.

17K

AEROSPACE RELATED COMPANIES

>120K

WORKERS
EMPLOYED

>\$19B

ANNUAL REVENUE



MEDICAL DEVICES, EQUIPMENT, AND PHARMACEUTICALS MANUFACTURING

Florida ranks second in the nation for medical device manufacturing, with strong production in medical device subcategories, such as \$2 billion (27% of the national total) for contact lens manufacturing.

2ND

IN THE NATION

27%

NATIONAL CONTACT
LENS MANUFACTURING



Semiconductor Internship Program

FloridaMakes
it possible.

BUILD YOUR FUTURE TALENT PIPELINE TODAY!

Partner with us to create internship opportunities that shape the next generation of semiconductor professionals. Together, we can close the skills gap and drive innovation in our industry.

UF | Florida Semiconductor Institute
UNIVERSITY of FLORIDA



**Partner With Us to Shape the
Workforce of Tomorrow!**



Let's collaborate to develop internships tailored to your needs. Together, we'll empower the workforce of tomorrow and ensure Florida stays at the forefront of semiconductor innovation.



Semiconductor Internship Program

FloridaMakes
it possible.



NSF
NSF Engines:
Central Florida
Semiconductor
Innovation Engine

Spring/Summer/Fall 2025

SEMICONDUCTOR INTERNSHIP *Opportunity*



Complete the student interest form today.

UF | Florida Semiconductor Institute
UNIVERSITY of FLORIDA

The Florida Semiconductor Institute (FSI) is pleased to announce a grant-funded semiconductor-focused paid internship program partnering with the NSF-funded Central Florida Semiconductor Innovation Engine.

Who is eligible? University, state college, technical college and high-school students from across Florida who are in engineering, manufacturing, chemical or related programs.

Internship details: Paid internships for up to 12 weeks with semiconductor-related companies in Florida.

If interested, please fill out the student interest survey using the QR code. The **Florida Advanced Technological Education Center (FLATE)** will host an information session with more details.

Contact ernie.friend@flate.org with any questions.



Questions? Contact Ernie.Friend@flate.org

CHIPS for America



\$39 billion for incentives

Two component programs to:

1. Attract large-scale investments in advanced technologies such as leading-edge logic and memory, and advanced packaging
2. Incentivize expansion of manufacturing capacity for mature and other types of semiconductors

\$11 billion for R&D

Four integrated programs to:

1. Conduct research and prototyping of advanced semiconductor technology
2. Strengthen semiconductor advanced packaging, assembly, and test
3. Enable advances in measurement science, standards, material characterization, instrumentation, testing, and manufacturing

\$2 billion for DoD Microelectronics Commons

A national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”

Workforce Initiatives



CHIPS for America – Incentive Programs

- The CHIPS Act's manufacturing incentives have sparked substantial investments in the U.S. Companies in the semiconductor ecosystem have announced [dozens](#) of new projects across America — totaling nearly \$450 billion in private investments — since the CHIPS Act was introduced. These announced projects will create more than 56,000 jobs in the semiconductor ecosystem and support hundreds of thousands of additional U.S. jobs throughout the U.S. economy.
- Thus far, the CHIPS Program Office (CPO) has announced **\$32.5417 billion in grant awards** and up to **\$5.5 billion in loans to 32 companies across 48 projects in 23 states**. These projects include total investment of more than \$380 billion over two decades, with the vast majority invested by 2030. **The projects are also expected to create over 145,000 new jobs – over 43,000 manufacturing jobs and over 102,000 construction jobs.**
- **Florida has received one CHIPS for America incentive award announced so far –** to [Rogue Valley Microdevices](#), a \$6.7 million CHIPS investment into a \$25 million project for a mature-node micro-electromechanical systems (MEMS) foundry to be developed in Palm Bay, Florida.

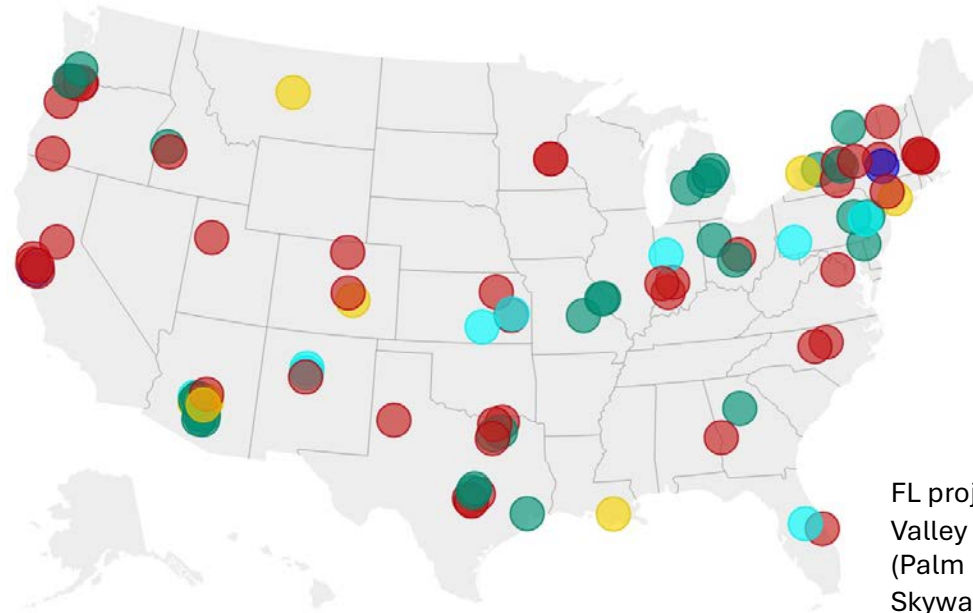
Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-incentives-awards/>

CHIPS for America – Incentives Program Awards

Semiconductor Supply Chain Investment Announcements, 2020-2025

Projects throughout the chip supply chain, including those with a CHIPS award or eligible for the Section 48D credit

■ Semiconductors ■ Packaging ■ Equipment ■ Materials ■ R&D Facility



FL projects are Rogue Valley Microdevices (Palm Bay) and Skywater expansion at NeoCity

Source: SIA Analysis • Created with Datawrapper

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-incentives-awards/>

March 2025: CHIPS Program Office Moves Under United States Investment Accelerator

On March 31, 2025 a new Executive Order Establishing the United States Investment Accelerator was signed, which specified that the CHIPS Program Office would now reside under the new US Investment Accelerator, and would “focus on delivering the benefit of the bargain for taxpayers by negotiating much better deals than those of the previous administration.”



*This covers the CHIPS for America incentives program, the CHIPS R&D Office and its programs has remained part of NIST



August 2025: CHIPS for America investment in Intel is re-structured as an equity investment of \$8.9 Bn

On August 22, 2025 it was announced that the U.S. Government would purchase 433.3 million primary shares of Intel common stock at a price of \$20.47 per share, equivalent to a 9.9 percent stake in the company. This investment provided American taxpayers with a discount to the market price, provided Intel with a much-needed infusion of capital, while enabling the U.S. and existing shareholders to benefit from Intel's long-term business success.

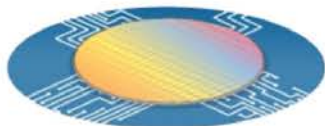


The government's equity stake will be funded by the remaining \$5.7 billion in grants previously awarded, but not yet paid, to Intel under the U.S. CHIPS and Science Act and \$3.2 billion awarded to the company as part of the Secure Enclave program. Intel will continue to deliver on its Secure Enclave obligations and reaffirmed its commitment to delivering trusted and secure semiconductors to the U.S. Department of Defense. The \$8.9 billion investment is in addition to the \$2.2 billion in CHIPS grants Intel has received to date, making for a total investment of \$11.1 billion.

Intel has also received a \$5 Bn investment from NVIDIA to co-design chips in Sept 2025, and a \$2 Bn investment from Softbank in Aug 2025.



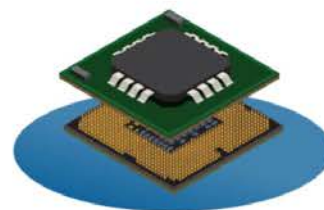
CHIPS R&D Programs



**CHIPS National
Advanced Packaging
Manufacturing
Program (NAPMP)**



**CHIPS Manufacturing
USA Program**



**CHIPS National
Semiconductor
Technology Center
(NSTC) Program**

Natcast 

Natcast is an independent nonprofit organization
and operator of the NSTC consortium



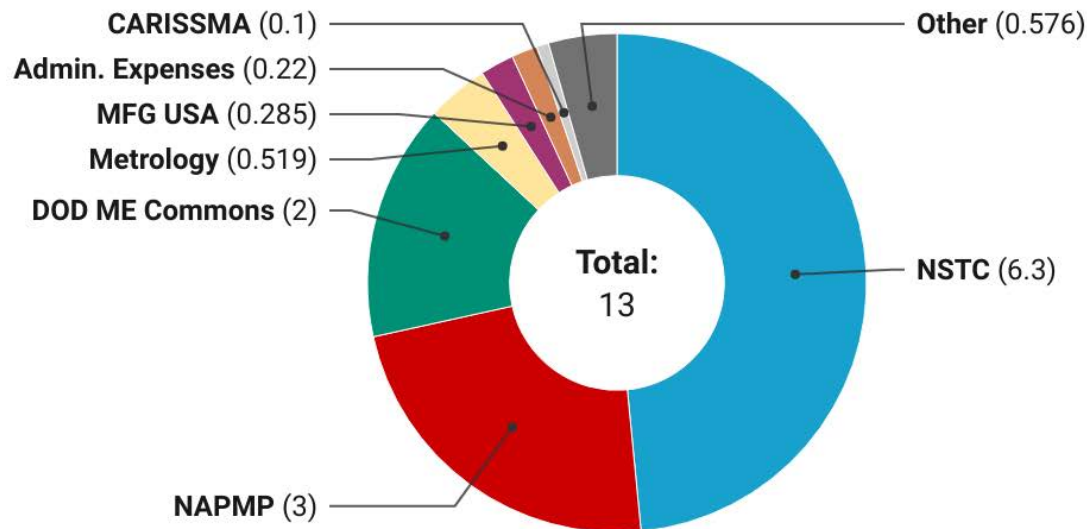
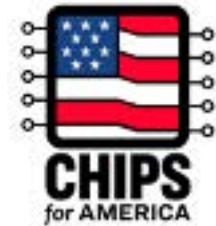
**CHIPS Metrology
Program**

Workforce Initiatives



CHIPS Research & Development Program Update

CHIPS R&D Programs Funding Allocation (\$ in Billions, approximate)



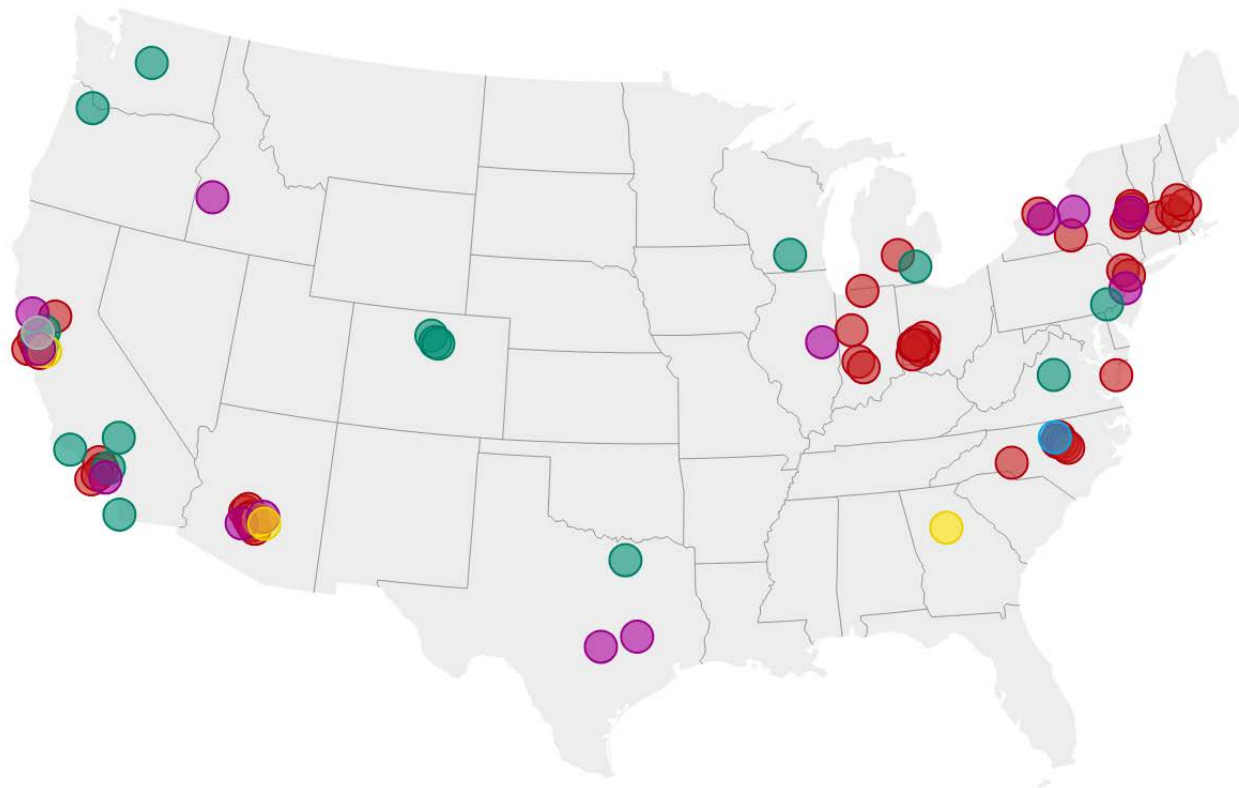
Source: Department of Commerce • Created with Datawrapper

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

CHIPS Research & Development Program Update

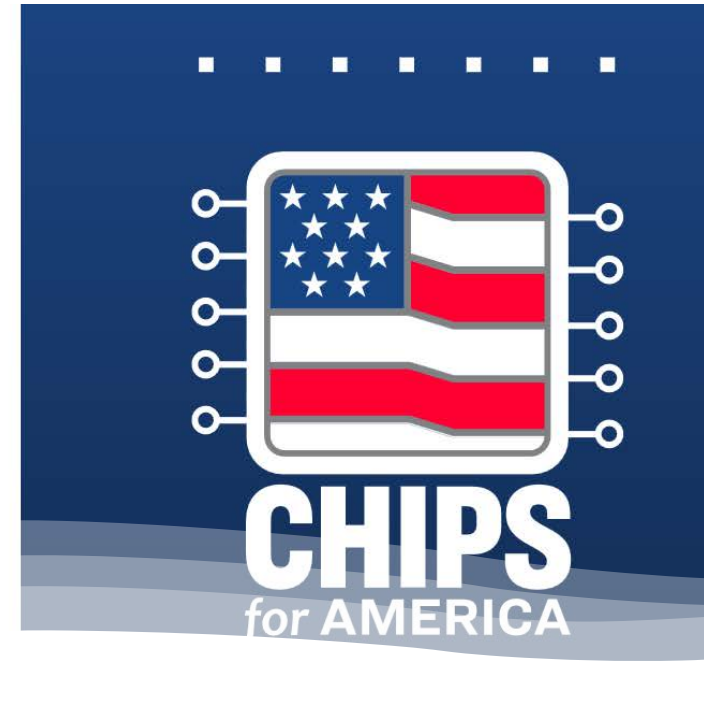
CHIPS R&D Programs Awards

■ DOD Microelectronics Commons ■ NSTC ■ NAPMP ■ Manufacturing USA ■ Metrology ■ Other



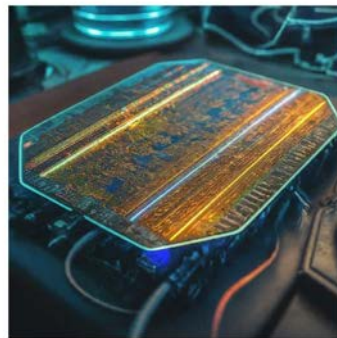
Source: Semiconductor Industry Association -
<https://www.semiconductors.org/chips-rd-programs/>

The Vision for the National Advanced Packaging Manufacturing Program



Why Advanced Packaging?

Continue advancements in computing power despite reaching the physical limits of miniaturization in increasing the number and density of transistors on existing silicon wafer technologies.



AI and HPC



**Low power edge
communication devices**



Medical Electronics

Use cases include high-performance computing and artificial intelligence, advanced telecommunications, medical devices, and autonomous vehicles, among others.



The Role of the package

Mechanical protection

- Handling
- Stability

Environmental protection

- Moisture
- Hermeticity
- Corrosion

Thermal protection

- Heat spreading
- Heat sinking
- Hotspot reduction

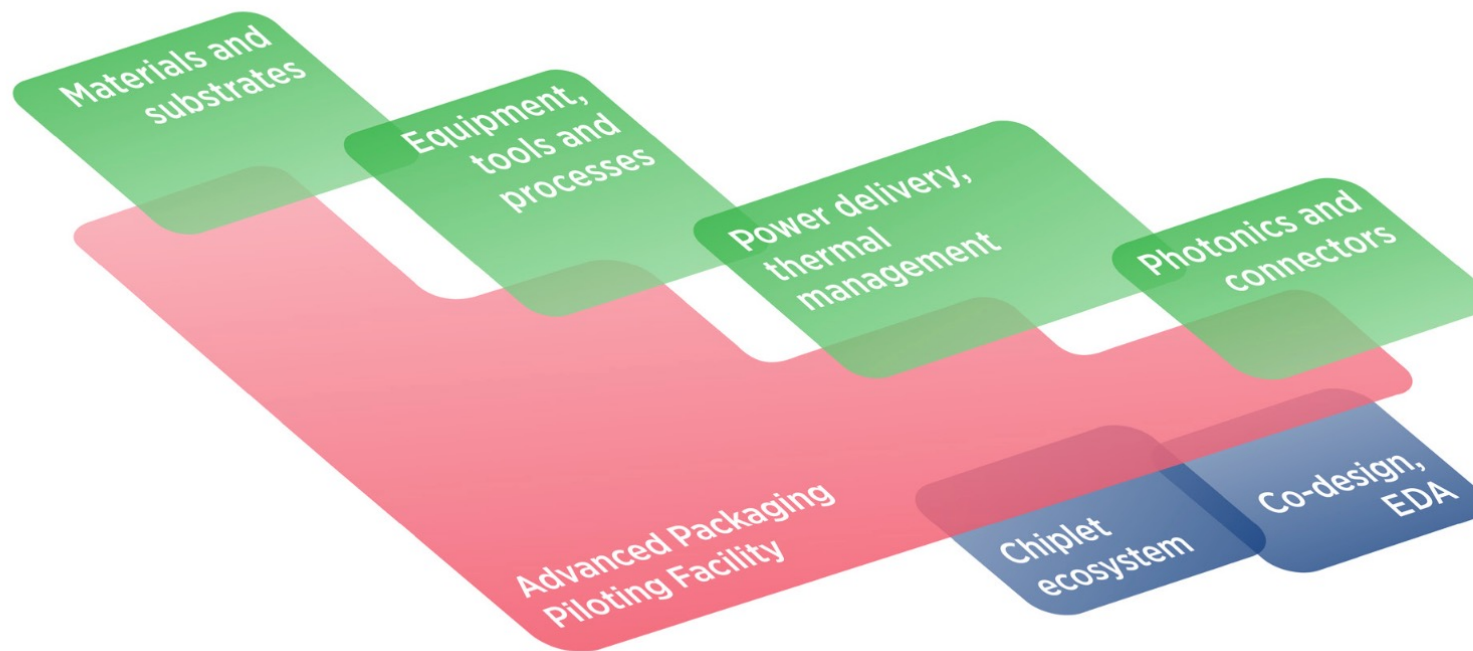
To protect and to serve

Connect electrically
to other chips

Deliver
power

Stable test and
integration platform

National Advanced Packaging Manufacturing Program (NAPMP)



Green = Technologies

Blue = Ecosystem Investments

Red = Integration & Testing Capabilities

National Advanced Packaging Manufacturing Program (NAPMP) Activities

The CHIPS National Advanced Packaging Manufacturing Program (NAPMP) will enable the development of a robust domestic advanced packaging ecosystem by:

- Establishing an advanced packaging piloting facility (or facilities) that accelerates the transfer of innovations in packaging, equipment, and process development into manufacturing;
- Driving the development of digital tools to reduce the time and cost of advanced packaging engineering; and,
- Establishing and supporting partnerships among industry, academia and training entities, and government to contribute to an advanced packaging workforce.



Technology Drivers & Funding Allocation

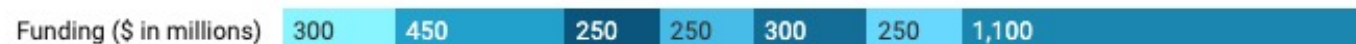


Five Drivers for Advanced Packaging advancements:

1. Scale-down and Scale-out
2. Heterogeneous Integration, including Chiplets
3. End-to-End Advanced Packaging Flows
4. Prototypes for Demonstrating Functionality
5. Aligned R&D efforts for Implementable Advanced Packaging Flows

Allocation of NAPMP Funds

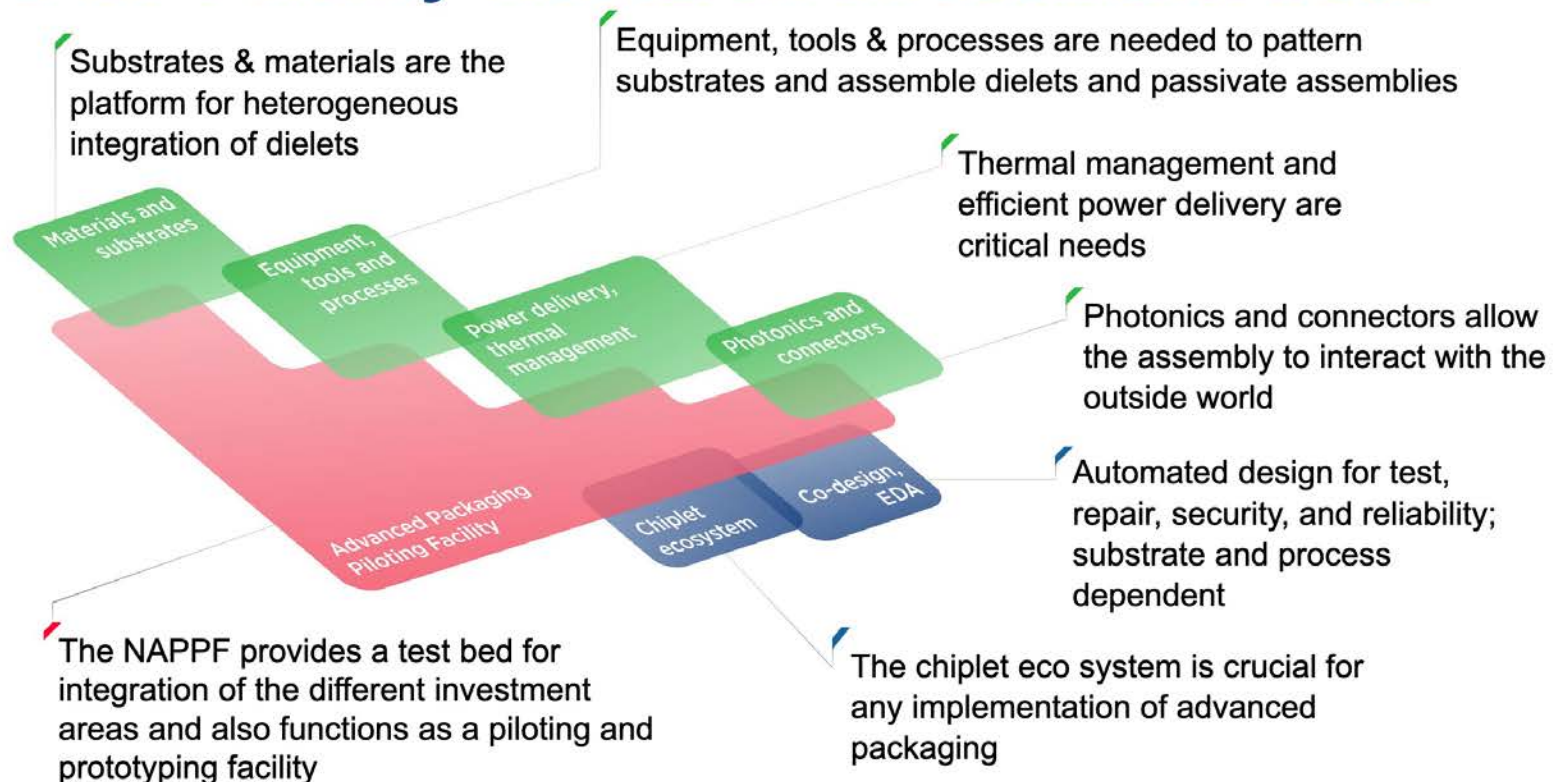
Materials & Substrates (\$300M) Equipment & Process (\$450M) Power Delivery & Thermal (\$250M)
Photonics & RF (\$250M) Chiplets Ecosystem (\$300) Co-Design & EDA (\$250M) Advanced Packaging
Piloting Facility (\$1.1B)



Created with [Datawrapper](#)



NAPMP Priority Research Investment Areas



NAPPF: National Advanced Packaging Piloting Facility



NAPMP Materials & Substrates Funding

- Funding Opportunity released on Feb 28, 2024 for R&D activities that will establish and accelerate domestic capacity for advanced packaging substrates and substrate materials
 - \$300 million total, up to \$100 million per award over 5 year period of performance
 - Evaluate multiple types of substrates: Silicon, Glass/Optics, Others
- Initial concept papers due April 2024
- 8 teams invited to submit final proposals that were due July 2024
- 3 selections: Absolics, GA; Applied Materials, CA; Arizona State, AZ – Nov 21, 2024
- <https://www.nist.gov/document/nofo-national-advanced-packaging-manufacturing-program-napmp-materials-substrates>
- <https://www.nist.gov/news-events/news/2024/11/chips-america-announces-300-million-funding-boost-us-semiconductor>

NAPMP Notice of Funding Opportunity #2: 5 R&D Areas

In October 2024, the Department of Commerce issued a NOFO to open a competition for new research and development (R&D) activities that will establish and accelerate domestic capacity for semiconductor advanced packaging. The CHIPS for America program anticipates funding up to \$1.6 billion in funding innovation across five R&D areas, as outlined in the vision for the NAPMP. Awards will be made for up to \$150 million per award over a 5-year period.

Funded activities are expected to be relevant to one or more of five R&D areas:

- Equipment, tools, processes, and process integration; \$450 million
 - Power delivery and thermal management; \$250 million
 - Connector technology, including photonics and radio frequency (RF); \$250 million
 - Chiplets ecosystem; \$300 million
 - Co-design/electronic design automation (EDA). \$250 million
-
- In addition to the R&D areas, the funding opportunity included opportunities for prototype development(s).
 - Notice of Intent: https://www.nist.gov/system/files/documents/noindex/2024/07/09/CHIPS%20NAPMP%20NOI_07092024.pdf
 - NOFO: <https://www.nist.gov/chips/r%2526d-funding-opportunities/notice-funding-opportunity-chips-napmp>
 - Concept Papers were due December 20, 2024; **Invited consortia will have 60 days from notice of invitation to submit a full proposal.**
 - CHIPS Teaming Partner List (to sign up or find other partners): <https://www.nist.gov/chips/chips-america-teaming-partner-list>

National Advanced Packaging Manufacturing Program (NAPMP)



\$300 mln funded
& awarded during
2024

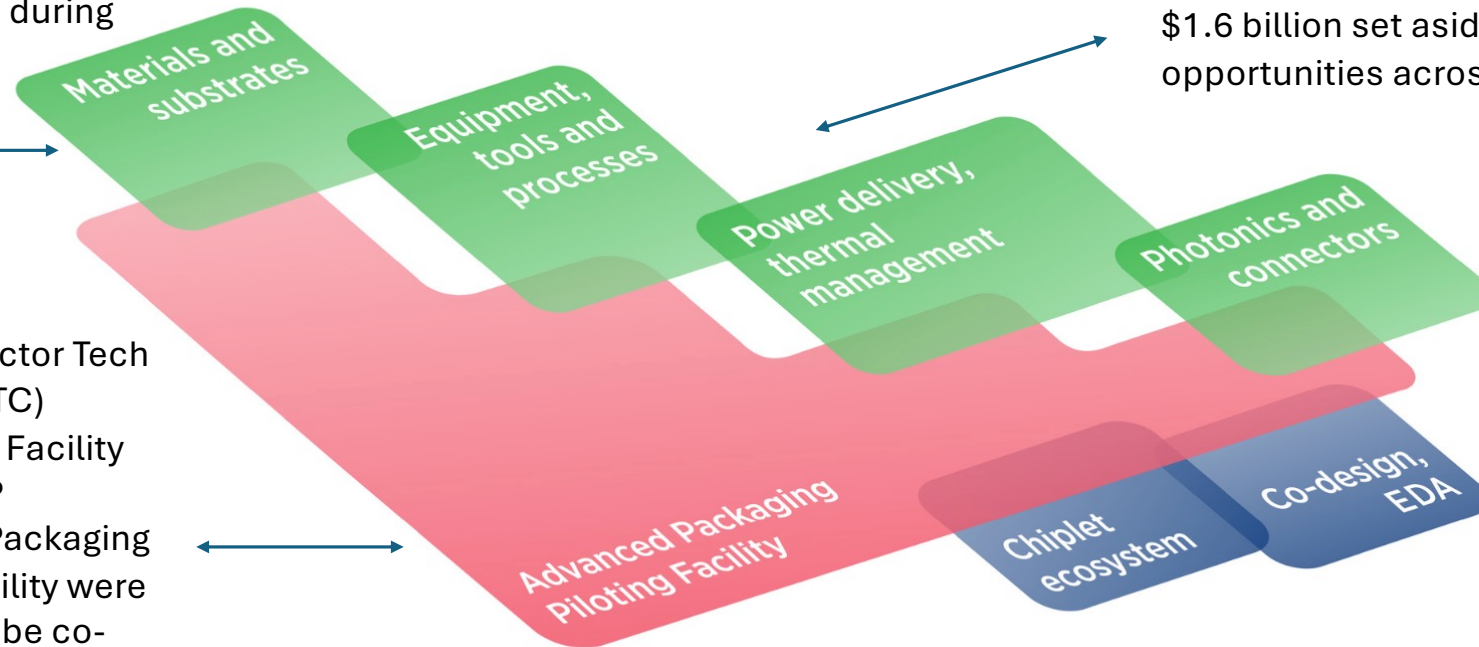
\$1.6 billion set aside for series of
opportunities across these 5 topics

National
Semiconductor Tech
Center (NSTC)
Prototyping Facility
and NAPMP
Advanced Packaging
Piloting Facility were
planned to be co-
located

Green = Technologies

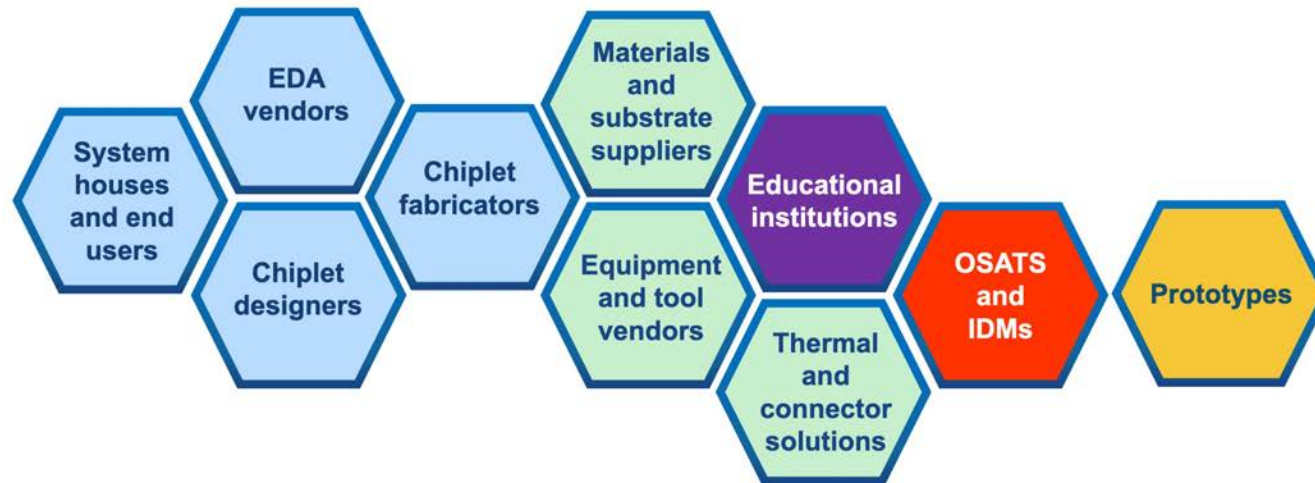
Blue = Ecosystem Investments

Red = Integration & Testing Capabilities



Plenty of Opportunities to Collaborate Across the Ecosystem!

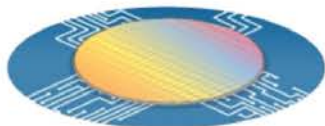
Collaboration is Critical for Success



We encourage you to begin identifying your individual contributions to the ecosystem as well as partners who can help accomplish the vision and goals of the NAPMP.



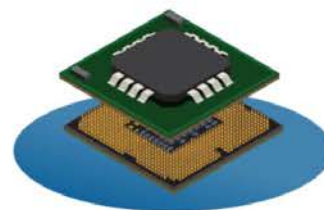
CHIPS R&D Programs



**CHIPS National
Advanced Packaging
Manufacturing
Program (NAPMP)**



**CHIPS Manufacturing
USA Program**



**CHIPS National
Semiconductor
Technology Center
(NSTC) Program**

Natcast 

Natcast is an independent nonprofit organization
and operator of the NSTC consortium



**CHIPS Metrology
Program**

Workforce Initiatives



CHIPS National Semiconductor Technology Center (NSTC) / Natcast

- The NSTC was originally set up to be operated by the National Center for the Advancement of Semiconductor Technology ([Natcast](#)).
- The NSTC was established to “conduct research and prototyping of advanced semiconductor technology and grow the domestic semiconductor workforce to strengthen the economic competitiveness and security of the domestic supply chain.”
- Natcast has distributed 3 “Jumpstart” funding opportunities - [Artificial Intelligence Driven RF Integrated Circuit Design Enablement \(AIDRFIC\)](#) (\$30M, 3 awardees) [Test Vehicle Innovation Pipeline \(TVIP\)](#) (\$55M, Proposals due Oct 2024, Under Evaluation), and PFAS Reduction and Innovation in Semiconductor Manufacturing (PRISM) (\$35M – Proposals due Jan 2025, Under Evaluation)
- NSTC [Workforce Partner Alliance \(WFPA\) Program](#) (\$11M to 7 awardees (AZ, CA, ID, IL, NY, TX))

Allocation of NSTC Funds



Created with [Datawrapper](#)

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

CHIPS National Semiconductor Technology Center (NSTC)

Natcast: Facilities Strategy and Opportunities

- **Facilities Model and Selection Process** – [Natcast webpage](#), [model factsheet](#), [process factsheet](#), [press release](#), [webinar](#), [slides](#)
- **NSTC Administrative, Collaboration and Design Facility** – a multi-functional facility, serving as the location for key operations of the NSTC, including convening, design research, workforce efforts, and administrative offices. **Sunnyvale, CA**
 - Host Natcast administrative functions and convening NSTC consortium members
 - Conduct NSTC programmatic activity like the Workforce Center of Excellence and the NSTC Design Enablement Gateway
 - Support advanced semiconductor research in chip design, electronic design automation, chip and system architecture, and hardware security
- **NSTC EUV Center** – access to EUV lithography for the NSTC through an agreement with an existing facility that meets the NSTC program requirements. **Albany, NY**
 - Provide NSTC members with access to EUV technology to facilitate a wider range of research and a path to commercialization, including technologies with the most challenging feature sizes.
 - Provide appropriate space for Natcast researchers and staff as well as member assignees to conduct research and collaborate in the facility.
- **NSTC Prototyping and NAPMP Advanced Packaging Piloting Facility** – co-located research and development for prototyping and advanced packaging capabilities to further both the NSTC and NAPMP programs. **Tempe, AZ**
 - Provide NSTC members with 300mm research and prototyping front-end manufacturing and packaging capabilities allowing for access to state-of-the-art and development of next-generation technologies
 - Provide the domestic semiconductor ecosystem with unique value to conduct coordinated and collaborative front-end semiconductor and advanced packaging R&D

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

August 2025: U.S. Department of Commerce announces that it is relieving Natcast of responsibilities for managing NSTC, bringing that program authority back into NIST

On August 25, 2025 Commerce Secretary Howard Lutnick sent a [letter](#) to the leadership of Natcast declaring that, in the view of the US Department of Commerce, the Biden Administration's establishment and designation of the non-profit consortium (Natcast) for the purpose of operating the NSTC violated the lawful limits on the federal government's authority imposed by the Government Corporations Control Act (GCCA). Therefore, the Department would "no longer rely upon Natcast to operate NSTC on behalf of the government" and would return all authority and budget to the Department.



Since this action by the Trump Administration, Natcast has begun the process of winding down its operations. It is unclear what portions of the program(s), awards and agreements previously issued and funded by Natcast will remain funded and operational and what may be re-programmed or re-competed.

Sept 24, 2025: U.S. Department of Commerce announces new CHIPS R&D Office Broad Agency Announcement funding opportunity focused on semiconductors, quantum and AI technology

On September 24, 2025 the CHIPS R&D Office issued a Broad Agency Announcement for a new funding announcement "to advance semiconductor technology and accelerate the pace of commercialization to enable technology dominance in the industries of the future." The funding announcement highlighted areas including "advanced microelectronics research and development with a nexus to Artificial Intelligence (AI), Quantum Technology, Biotechnology, Biomanufacturing, Commercialization of Innovation, and/or Standards Development."

This Broad Agency Announcement appears to re-program / re-compete some of the funding previously allotted to Natcast and the National Semiconductor Technology Center (NSTC).

More information is available via the NIST CHIPS R&D website here: <https://www.nist.gov/chips/r%2526d-funding-opportunities/crdo-broad-agency-announcement-baa>

Frequently Asked Questions regarding this Broad Agency Announcement are available at [this link](#)

U.S. Department of Commerce CHIPS R&D Office Broad Agency Announcement funding opportunity application process *(\$10 million minimum project size, up to 5 year period of performance)*

#1) White Paper: White Papers are required and may be submitted at any time via grants.gov. CRDO will review White Paper submissions as soon as practicable after they are submitted ... for eligibility, completeness, and responsiveness. White Papers deemed eligible, complete, and responsive will be reviewed for (1) scientific and technical merit and (2) the potential contribution to national and economic security.

#2) Pre-negotiation Package: Applicants whose White Papers are determined to have sufficient scientific and technical merit and potential contributions to national and economic security will be invited to submit a Pre-negotiation Package, which will include a detailed technical and cost proposal, and other required documents. Pre-negotiation Packages may only be submitted by entities that are invited to do so by CRDO. Pre-negotiation Packages submitted in the absence of a specific invitation will not be reviewed or evaluated in any way. Additional information will be provided to those invited to submit a Pre-negotiation Package.

Additional information regarding the [Submission Instructions and Package Requirements](#) and [Administrative and National Policy Requirements](#) for this BAA is available.

Submissions are via grants.gov here: <https://www.grants.gov/search-results-detail/360651>

Florida Semiconductor Innovation Engine funding opportunity

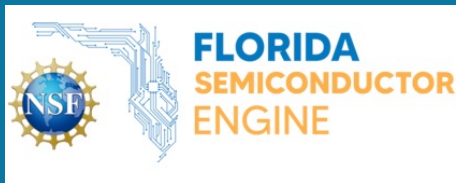
November - December 2025

The Florida Semiconductor Innovation Engine is excited to announce the official launch of a Request for Proposals (RFP) aimed at advancing design, testing, and prototyping in advanced specialty packaging. This opportunity is exclusively available to Florida Semiconductor Engine Association Members and Semiconductor Cluster Members, reinforcing our commitment to fostering innovation and collaboration within our growing network.

Application period opens November 1, 2025; and applications will be due December 13, 2025.

Additional information regarding this opportunity is available on the Florida Semiconductor Engine website:
<https://semiconductorengine.org/>

An application for membership in the Florida Semiconductor Engine (and eligibility for this funding opportunity) is available here: <https://semiconductorengine.org/join-the-engine>



NIST CHIPS Metrology Program

- Led by Director Dr. Paul Hale, the CHIPS Metrology Program has ongoing research activities and is leading NIST semiconductor and microelectronics metrology efforts centered around 7 grand challenges.

CHIPS Metrology Grand Challenges

1. Metrology for Materials Purity, Properties, and Provenance
2. Advanced Metrology for Future Microelectronics Manufacturing
3. Enabling Metrology for Integrating Components in Advanced Packaging
4. Modeling and Simulating Semiconductor Materials, Designs, and Components
5. Modeling and Simulating Semiconductor Manufacturing Processes
6. Standardizing New Materials, Processes, and Equipment for Microelectronics
7. Metrology to Enhance Security and Provenance of Microelectronic-based Components and Products

Allocation of CHIPS Metrology Funds



Created with [Datawrapper](#)

NIST CHIPS Metrology Program Activities & Opportunities

- The CHIPS Metrology Program is a NIST R&D program that enables advances and breakthroughs in measurement science, standards, material characterization, instrumentation, testing, and manufacturing capabilities that will accelerate the underlying research and development for metrology of next generation microelectronics and ensure the competitiveness and leadership of the United States within this sector.
- Small Business Innovation Research (SBIR) [NOFO](#) closed June 14 – \$54 million funding opportunity for eligible small businesses to explore the technical merit or feasibility of an innovative idea or technology for developing a viable product or service for introduction in the commercial microelectronics marketplace.
 - April 2024 Webinar – [Slides](#) and [recording](#)
 - **NIST Metrology SBIR Funding - \$4.8 million awarded to 17 Phase I awards across 9 states**
- [Ongoing Projects and Programs](#) – Over 30 R&D projects and programs initiated so far (\$109M)
- January 2024 webinar “Inside CHIPS Metrology: Research that Accelerates Innovation” – [slides](#) and [recording](#)
- June 2023 – [Metrology Gaps in the Semiconductor Ecosystem](#)
- August 2022 – [Strategic Opportunities for U.S. Semiconductor Manufacturing](#)

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

CHIPS Manufacturing USA Institute

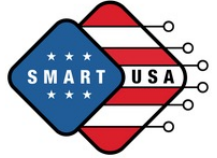
- The CHIPS Manufacturing USA institute will be “an entirely new and unique institute that facilitates the manufacturing of semiconductor digital twins” to “reduce U.S. chip development and manufacturing costs, such as by improving capacity planning, production optimization, facility upgrades, and real-time process adjustments.”

The objectives of the CHIPS Digital Twins Manufacturing USA Institute include:

- Convene stakeholders across the semiconductor production ecosystem
- Improve the state of the art in manufacturing-relevant digital twins
- Significantly reduce cost for U.S. chip development and manufacturing
- Improve development cycle times of semiconductor product innovation
- Advance digital twin-enabled curricula for training a domestic semiconductor workforce
- Create a digital twin marketplace for industry to access digital models

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

CHIPS Manufacturing USA Institute – SMART USA



- Led by Director Dr. Eric Forsythe, the CHIPS R&D Office launched a [NOFO](#) for up to \$285 million the establishment of a Manufacturing USA Institute focused on digital twins for the semiconductor industry. Digital twins are virtual models that mimic the structure, context, and behavior of a physical counterpart.
- **The Semiconductor Research Corporation (SRC) was selected to establish the Semiconductor Manufacturing and Advanced Research with Twins USA, or SMART USA, Institute** to focus on efforts to more rapidly develop, validate, and use digital twins to improve domestic semiconductor design, manufacturing, advanced packaging, assembly, and test processes. The institute will be supported by \$1 billion in funding, including \$285 million from the Department of Commerce. The CHIPS Manufacturing USA Institute will join an existing network of seventeen Institutes.
- University of Florida Florida Semiconductor Institute has a role as the convener of the regional hub for Florida and Puerto Rico. UF Professor Volker Sorger has a role as a technical lead for the SMART USA Institute as well.

SMART USA Institute: <https://www.src.org/about/smart-usa-institute/>

Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

DOD Microelectronics Commons (ME Commons)

The goal of the Microelectronics Commons programs is to address the "valley of death" and facilitate the lab-to-fab transition for microelectronics research with defense applications. The ME Commons is led by Dr. Dev Shenoy at DOD and Stephanie Lin at NSTXL.



The ME Commons awarded \$269 million to 33 projects in 27 states. Additional information about the projects is forthcoming, with preliminary detail below

- Quantum: 4 projects, \$32 million
- Secure edge computing: 4 projects, \$25 million
- 5G/6G: 5 projects, \$42 million
- Electromagnetic warfare: 6 projects, \$51 million
- Commercial leap-ahead: 7 projects, \$38 million
- Artificial intelligence, 7 projects, \$42 million
- Cross-Hub Enablement Solution (CHES) award: \$39 million.

Microelectronics Commons Hubs



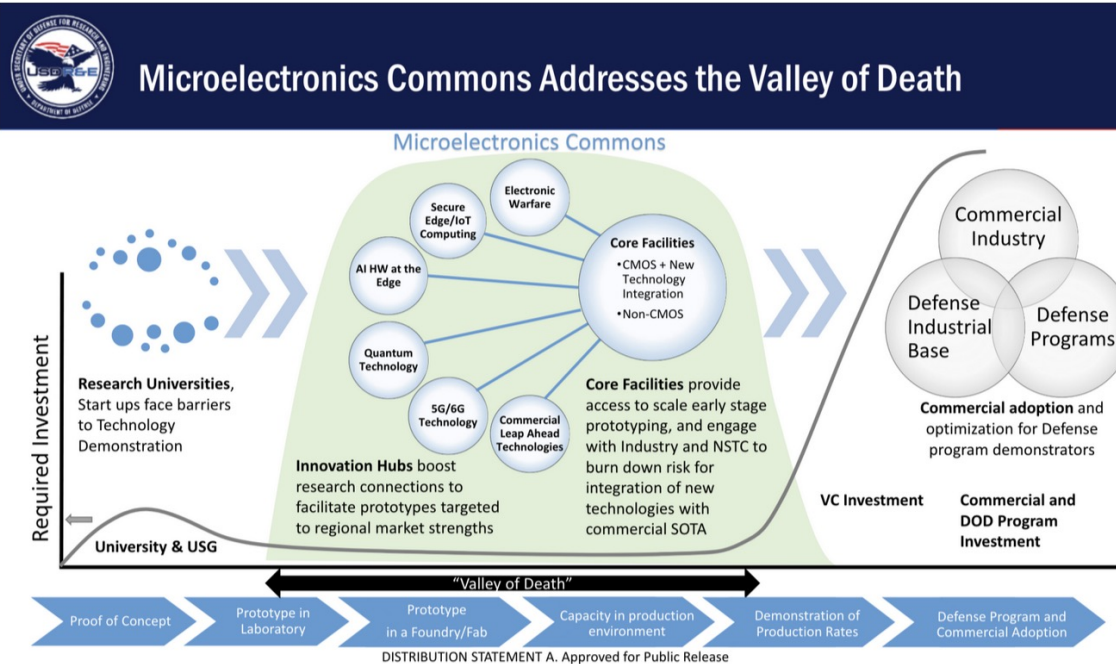
Source: Semiconductor Industry Association - <https://www.semiconductors.org/chips-rd-programs/>

DoD ME Commons Hubs

Allocation of DOD Microelectronics Commons Funds



Created with [Datawrapper](#)



State	Hub	Hub Leader	Members #	Initial Award (\$ in Millions)	Hub Website
Westborough, MA	Northeast Microelectronics Coalition (NEMC) Hub	Massachusetts Technology Collaborative (MassTech)	90	\$19.7	Source
Bloomington, IN	Silicon Crossroads Microelectronics Commons (SCMC) Hub	Applied Research Institute (ARI)	130	\$32.9	Source
Los Angeles, CA	California Defense Ready Electronics and Microdevices Superhub (California DREAMS) Hub	University of Southern California (USC)	16	\$26.9	Source
Raleigh, NC	Commercial Leap Ahead for Wide Bandgap Semiconductors (CLAWS) Hub	North Carolina State University (NCSU)	7	\$39.4	Source
Tempe, AZ	Southwest Advanced Prototyping (SWAP) Hub	Arizona State University (ASU)	27	\$39.8	Source
Dayton, OH	Midwest Microelectronics Consortium (MMEC) Hub	MMEC	65	\$24.3	Source
Albany, NY	Northeast Regional Defense Technology Hub (NORDTECH)	State University of New York (SUNY)	51	\$40.0	Source
Stanford, CA	California-Pacific-Northwest AI Hardware Hub (Northwest-AI Hub)	Stanford University	44	\$15.3	Source

Semiconductor Internship Program

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Spring/Summer/Fall 2025

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The Florida Semiconductor Institute (FSI) is pleased to announce a grant-funded semiconductor-focused paid internship program partnering with the NSF-funded Central Florida Semiconductor Innovation Engine.

Who is eligible? University, state college, technical college and high-school students from across Florida who are in engineering, manufacturing, chemical or related programs.

Internship details: Paid internships for up to 12 weeks with semiconductor-related companies in Florida.

If interested, please fill out the student interest survey using the QR code. The **Florida Advanced Technological Education Center (FLATE)** will host an information session with more details.

Contact ernie.friend@flate.org with any questions.



Questions? Contact Ernie.Friend@flate.org

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**Partner With Us to Shape the
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Let's collaborate to develop internships tailored to your needs. Together, we'll empower the workforce of tomorrow and ensure Florida stays at the forefront of semiconductor innovation.



Questions



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Thank You

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