Warpage analysis of lidded flip chip CSP: Impact of material properties and dimensions

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Abstract

The primary objective of this study was to investigate the influence of various material properties and dimensions on the warpage of lidded flip chip chip-scale packages (fcCSP). While simulation approaches are often more efficient and cost-effective for such studies, accurately predicting warpage remains a significant challenge. Numerous factors are simplified during modeling, which limits the accuracy of the results. As a result, simulation cannot fully replace experimental data. Hence, this study used experimental methods to study warpage in lidded fcCSP. Two test vehicles with package body sizes of 19x19 mm and 21x21mm were used with different die thicknesses, substrate core materials, molding compound (MC) materials, and other packaging variations. The goal was to determine which materials affect warpage the most and what coefficient of thermal expansion (CTE) combinations lead to a fcCSP package within JEDEC warpage specifications. An optical inspection system was used to measure the coplanarity at room temperature, and shadow moiré was used to measure warpage at reflow temperature of 245 °C. Although the simulation may not precisely capture the magnitude of warpage, simplified models (excluding residual stresses, cure shrinkage of MC, spatial non-uniformity in material properties, etc.) were still used to evaluate warpage trends and compared it against experimental data. Results from this study can be utilized to optimize the material set and material properties for large body fcCSP package.

Key words

coplanarity, warpage, experimental validation, fcCSP, FEA, package warpage

I. Introduction

Compared to wire bond packaging, flip chip technology has become increasingly popular in high-performance integrated circuits (IC) due to its numerous advantages. One of the key benefits is its ability to provide more I/O connections while reducing the overall package size. This is achieved by directly connecting the chip to the substrate through solder/copper pillar bumps, which significantly reduces parasitic inductance and capacitance, thereby enhancing device performance. Since IBM's invention of flip chip packaging in 1961, over 60 years has passed, and the technology has evolved to become mature. However, as the industry shifts toward smaller dies due to advanced technology nodes and larger packages driven by higher I/O requirements, the warpage issue, which critically affects both surface-mount technology (SMT) yield and package reliability, has become more challenging. A large body fcCSP is referred to as any package with dimensions 17 x 17mm and above, presenting a challenge with higher warpage.

Warpage can occur at many stages throughout the packaging process: (1) substrate fabrication often introduces initial warpage due to CTE mismatch among the core, build-up layers, and metal traces, leading to deformation even before assembly begins [1]; (2) During die attach, further stress develops as a result of mismatched CTE between die and substrate [2]; (3) Underfill curing causes additional warpage, because of shrinkage of underfill material [3]; (4) Molding and post mold cure (PMC) are widely regarded as the most significant contributor to warpage, primarily due to the volumetric shrinkage of MC during the cure process, which generates substantial residual stresses [4]-[6]; (5) Finally, as the package cools down to room temperature after PMC, CTE mismatch of all different layers lead to further changes in package shape.

During the subsequent SMT reflow process, the package

must remain well aligned with the solder pads throughout the process, both at room temperature and under elevated reflow temperatures. Any misalignment caused by poor coplanarity, or excessive warpage may result in soldering defects, such as non-wet opens or solder bridging, which negatively impacts the SMT yield. Moreover, uneven solder joint formation can degrade long-term reliability. To mitigate these risks, industry standards have been established to defined acceptable limits for coplanarity at room temperature and warpage at high temperature. JESD22-B108B [7] provides a coplanarity testing method at room temperature by measuring the distance of the apex of solder balls relative to a reference plan. The recommended flatness requirements for packages with body sizes equal or less than 21mm are presented in table I of JEP95 [8]. For warpage during high-temperature reflow process, JESD22-B112C [9] provides detailed measurement methods, including thermal shadow moiré, 3D digital image correlation and laser reflection method, etc. For package sizes greater than 15mm, the recommended warpage limit values can be found in table II of SPP-024 [10].

Symbol	Definition	Values	
		b (nom)	ddd
ddd	The profile tolerance controlling the location of the crowns of the balls with respect to Datum C (either the seating plane or the LBR plane). (See Figure 4.5-5) The zone is unidirectional and extends upward from Datum C. Refer to SPP-024 for Reflow Flatness Requirements (RFR) which is more relevant for Surface-Mount Technology (SMT).	0.50 0.438-0.450 0.437-0.413 0.412-0.338 0.337-0.313 0.312-0.300 0.25 0.20	0.20 0.20 0.15 0.10 0.09 0.08 0.08 0.08

Table I: BGA Coplanarity Specification Based on Ball Sizes

Table 2 — Flatness requirements (mm) during reflow for components greater than 15mm on any side, applies to temperature range from flux activation to reflow peak.

e - Ball Pitch (mm)	b - Ball Diameter (mm)[v]										
	0.20	0.25	0.30	0.35	0.40	0.45	0.50	0.55	0.60	0.80	0.90
0.40	-0.09 +0.12	-0.10 +0.15	-0.12 +0.17								
0.50		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20							
0.65		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20	-0.14 +0.22	-0.14 +0.23					
0.80		-0.10 +0.15	-0.12 +0.17	-0.13 +0.20	-0.14 +0.22	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23			
1.00					-0.14 +0.22	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23	-0.14 +0.23		
1.27									-0.14 +0.23	-0.14 +0.23	-0.14 +0.23
1.50									-0.14 +0.23	-0.14 +0.23	-0.14 +0.23

Table II: Allowable Reflow Temperature Warpage for Packages Above 15mm

Typically, to meet the specified coplanarity/warpage standards, a common practice is to perform finite element analysis (FEA) simulation to identify optimal combinations of materials and package structures. Although this method is generally effective, relying solely on simulations for precise warpage prediction remains challenging. FEA is generally conducted to evaluate how stresses or flatness vary relative to a baseline condition, typically assumed to be stress-free with no associated warpage. However, accurately predicting package warpage demands a comprehensive understanding of the "absolute" stress conditions in a package. This includes consideration of intrinsic residual stresses or deformation introduced during fabrication steps, which are often not considered in simulations. For example, shrinkage of MC during curing process has either been neglected or assumed to be constant in simulations, primarily because it is difficult to measure [11]-[13]. Nonetheless, many researchers have emphasized the importance of MC shrinkage in achieving accurate warpage predictions [14]-[17]. Neng et al. [16] reported that neglecting MC shrinkage could lead to errors as high as 90%. Lee et al. [17] demonstrated that cure-induced effects dominate over CTE mismatch. Besides EMC shrinkage, many other factors are also neglected, such as substrate shrinkage caused by relaxation of residual stresses in glass fibers during the substrate lamination process [18], and material property variations due to non-uniform filler distributions in EMC resulting from filler migration during the molding process [19]. Given these limitations, this study focuses primarily on experimental investigation to evaluate the warpage behavior under different material and structural combinations. Warpage simulation was also performed to study the gaps between prediction and experimental warpage measurement.

II. Test Vehicle Configuration

Fig. 1 depicts a typical lidded fcCSP package. The package includes a lid that acts as a heat spreader, with thermal interface material (TIM) between the chip and the lid for heat transfer. The chip is connected to the substrate via copper pillars. The substrate forms the base of the package, supporting the entire structure and providing electrical connections to external circuits. The molded compound enhances the overall strength of the package.

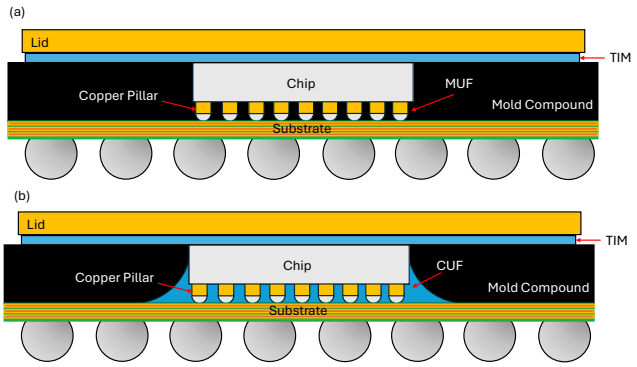


Fig. 1 Lidded fcCSP Construction, (a) MUF: Molded Underfill, (b) CUF: Capillary Underfill

The lid on the exposed die surface is achieved using film-assisted molding (FAM). In this process, a polymer film is vacuumed onto the top surface of the mold chase, allowing the EMC to flow around the package while keeping the top of the die uncovered. The film serves as a protective barrier

that prevents the EMC from contacting areas that need to remain exposed for subsequent lid attachment as shown in Fig. 2. However, under this configuration, using molded underfill (MUF) introduces additional challenges. Excessive transfer molding pressure can lead to mold flash- resin leakage past the film barrier- while insufficient pressure may result in void formation beneath the die due to incomplete underfill coverage. These voids have a significant impact on coplanarity/warpage, and the corresponding experimental results will be presented in a later section.

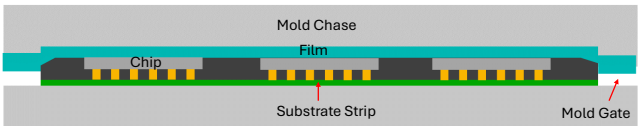


Fig. 2 FAM process

21 x 21 mm lidded fcCSP

The first test vehicle evaluated in this study is a 21 x 21 mm lidded fcCSP package with a 10.1 x 9.4 mm die mounted at the center. The package has 1064 solder balls arranged in a 0.5 mm pitch BGA array, with 0.3 mm ball diameter. The substrate consists of 6 metal layers, with a core thickness of 200 um and a solder mask thickness of 15 um, both of which are kept constant across all experimental groups. According to Table I and II, the maximum allowable coplanarity at room temperature is 80 um, while the acceptable warpage range at reflow temperature for this package body size and ball pitch is between -120 um to 170 um.

The experimental groups are designed to evaluate the impact of key material and structural parameters on package warpage. The configurations for all test vehicles are summarized in Table III.

Group	Core Material	Underfill (CUF)	EMC material	Die thickness (um)
1	C1	U1	M1	340
2	C1	U1	M1	180
3	C2	U1	M1	180
4	C1	N/A	M2	340
5	C1	N/A	M2	180
6	C2	N/A	M2	180
7	C2	N/A	M3	180

Table III: 21 mm Package Configurations for Warpage Evaluation

19 x 19 mm lidded fcCSP

The second test vehicle has body size of 19 x 19 mm and contains a 8.6 x 8.1 mm die. It includes 525 solder balls, arranged in a BGA layout with 0.8 mm pitch BGA and 0.45 mm ball diameter and shares the same substrate stack-up as the 21 x 21 mm package. The coplanarity limit at room temperature is 200 um, and the allowable warpage range at reflow is between -140 um to 230 um. The experimental groups for this package are summarized in Table IV. Group 5 adopts a package without molding, which enables a direct comparison against the molded version.

Group	Core Material	Underfill (CUF)	EMC material	Die thickness (um)
1	C1	U1	M1	340
2	C1	U1	M1	180
3	C1	N/A	M2	180
4	C1	N/A	M2	340
5	C1	U1	N/A (non-molded)	180
6	C1	N/A	M3	180
7	C1	U1	M3	180

Table IV: 19 mm Package Configurations for Warpage Evaluation

Fig. 3 shows warpage related properties: E1, E2, CTE1, and CTE2 represent the storage modulus and coefficient of thermal expansion below and above the glass transition temperature Tg, respectively.

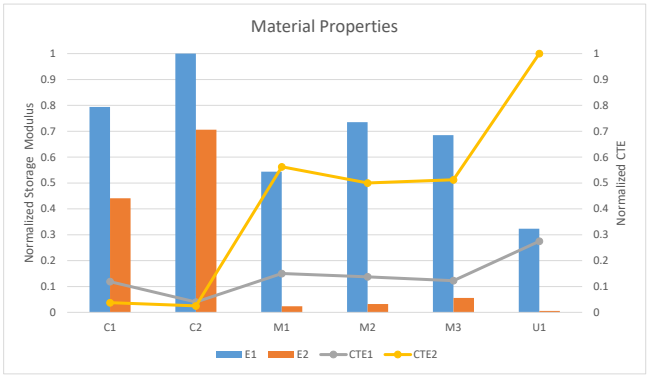
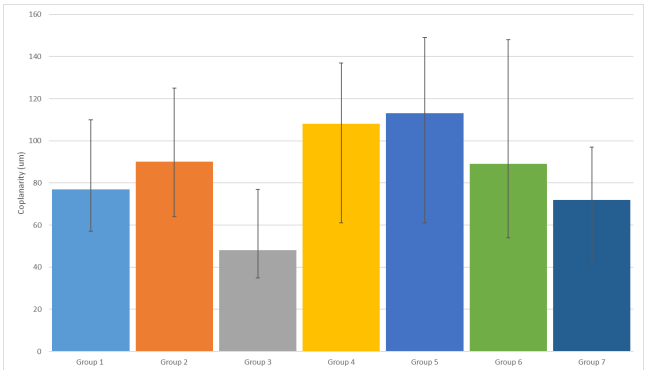


Fig. 3 Material Properties

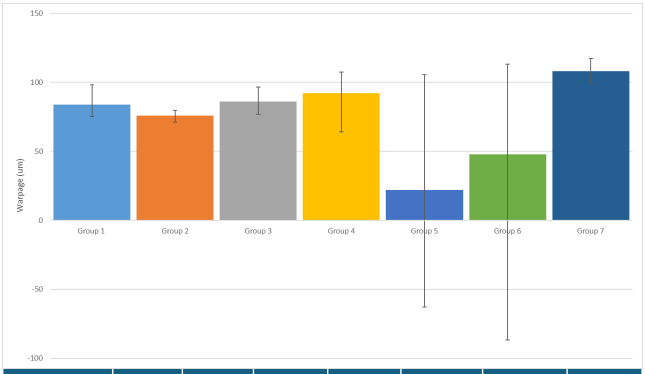
III. Experimental Results and Discussion

Fig. 4 and 5 illustrates the coplanarity at room temperature (25 °C) and warpage at peak reflow temperature (245 °C) for the 21 x 21 mm package. Coplanarity values were collected from 100 samples, and warpage values were obtained from 10 samples. The definition of positive and negative warpage in this study follows the JESD22-B112C [9].



Coplanarity (um)	1	2	3	4	5	6	7
Avg	77	90	48	108	113	89	72
SD	11	12.6	8.6	18.5	19.4	23.6	12.3

Fig. 4 Coplanarity results for 21 x 21 mm package at 25 °C



Warpage (um)	1	2	3	4	5	6	7
Avg	84	76	86	92	22	48	108
SD	7.7	3.3	7.6	13.7	68.3	86.6	6.2

Fig. 5 Warpage results for 21 x 21 mm package at 245°C

The error bars in the figure indicate the maximum and minimum values observed in the experiments, while the average and standard deviation are listed in the table within the figure.

By comparing group 1 and 2, the influence of die thickness on warpage behavior can be observed. It should be noted that the MC thickness increases along with the die thickness in order to maintain a flat top surface between the die and the MC. In general, a thicker die and MC tend to reduce warpage[20], which is consistent with the results observed at room temperature. However, at high temperature, packages with thicker die/MC exhibit larger warpage as shown in Figure 5. This may be due to the softening of organic materials after exceeding their Tg, resulting in the warpage being dominated by the lid, therefore, structures closer to the lid or thinner package tend to remain flatter. Group 2 and 3 compare the effect of substrate core CTE. The results show that core CTE has a significant impact on coplanarity at room temperature. The CTE of C2 at room temperature is about 30% of C1, and the coplanarity of group 3 is approximately half of group 2. The warpage results at high temperature become more similar. This is likely because 245°C is slightly above the Tg of C1 but lower than the Tg of C2, causing their CTEs to become closer. For group 4,5,6, and 7 using molded underfill, the variation in coplanarity results becomes significantly larger. This is especially evident at high temperatures, where some samples even exhibit warpage in the opposite direction. C-SAM inspection revealed that samples located farther from the mold gate contain numerous voids under the die, as shown in Fig. 6. Therefore, MUF groups are excluded from further discussion.

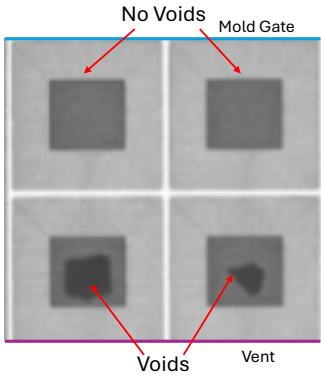
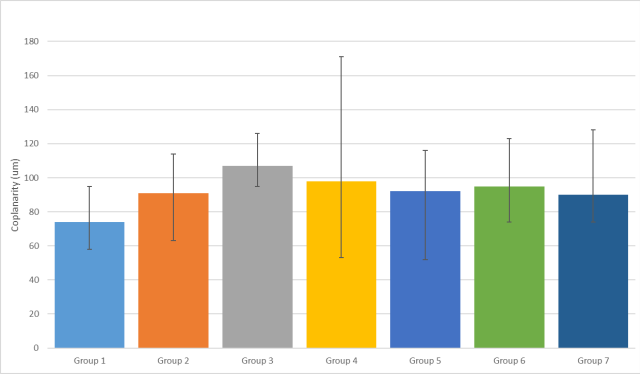


Fig. 6 C-SAM inspection for MUF samples

Based on the results, excluding MUF groups, all test groups easily meet the SPP-024 warpage requirements. However, coplanarity remains a challenge, with only group 3 meeting the JEP95 criteria. The results also indicate that the substrate core CTE has significant impact on warpage.

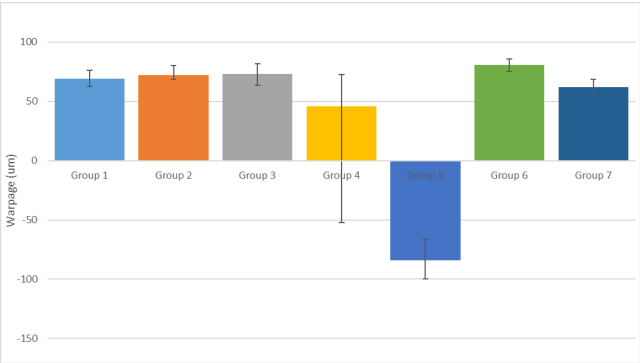
Similar to 21 x 21 mm package, Fig. 7 and Fig. 8 present the results for the 19 x 19 mm package. Group 1 and 2 compare the effect of die thickness. At room temperature, the coplanarity results are similar to those of the 21 mm package: a thicker die lead to lower coplanarity. At high temperature, however, the warpage values are very close. Since the 21 mm and 19 mm packages share the same bump size and pitch, both encountered the void issues with MUF. Due to the absence of molding in group 5, the package exhibits a warpage direction opposite to other groups. Group 2 and 7 investigate the effect of different molding compounds. As shown in Fig. 3, the CTEs of M1 and M3 are very similar. At room temperature, the storage modulus of M1 is 20% lower than that of M3. And the modulus of M1 is only half of M3's at high temperature. As a result, the two groups show comparable coplanarity, but at high temperature, the higher modulus of M3 leads to lower warpage.

Due to the larger ball size in 19 mm package, the coplanarity and warpage requirements are more relaxed, allowing all test groups to easily meet the JEDEC standard.



Coplanarity (um)	1	2	3	4	5	6	7
Avg	75	91	108	98	92	95	91
SD	8.1	9.2	6.6	26.4	11.4	8.6	8.3

Fig. 7 Coplanarity results for 19 x 19 mm package at 25 °C



Warpage (um)	1	2	3	4	5	6	7
Avg	69	72	73	46	-84	81	62
SD	4.2	3.4	5.2	36.5	10.0	4.2	3.7

Fig. 8 Warpage results for 19 x 19 mm package at 245°C

IV. Simulation Description

A quarter symmetry model of 19x19 mm and 21x21 mm lidded FCCSP was created. Fig. 9 illustrates the quarter symmetry boundary condition, while Table V details the constitutive material models used for the various elements in the package. Lumped properties were applied to the flip chip die bumps and Capillary Underfill (CUF). A Representative Volume Element (RVE) [21, 22] was created, and the Ansys Material Designer module was utilized to extract the lumped properties, representing the combined properties of the copper pillar, bumps and CUF. Table VI shows the stress-free temperatures of the different elements in the package, selected based on the assembly process temperatures. The element birth and death technique was used to capture the residual warpage from the assembly process. This method ensures that the mold compound attaches to the die/substate at a pre-warped state due to difference in stress free temperature and similarly lid/lid epoxy attaches to the pre-warped state of mold-die-substrate stack. To account for the metal traces, the trace mapping [23] feature in Ansys was used to capture the effective contribution of the metal traces. An example of this is illustrated in Fig 10. The reflow temperature profile was applied to all bodies. Shrinkage effects are not included in the model. Finally, warpage was simulated at 25°C and 245°C.

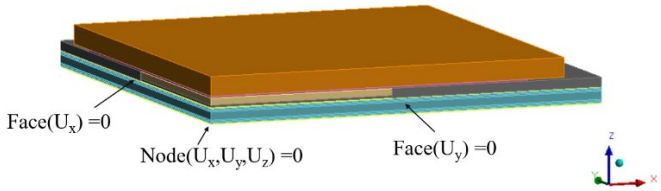


Fig. 9 Simulation boundary condition

Geometry element	Material model
Die	Temperature dependent Orthotropic
Mold	Temperature dependent Viscoelastic
Core	Temperature dependent linear elastic
Prepreg	Temperature dependent linear elastic
Solder mask	Temperature dependent linear elastic
Copper pillar/Solder/CUF	Temperature dependent linear elastic lumped model
Lid epoxy	Linear elastic
Lid	

Table V: Constitutive model

V. Simulation Results and Discussion

The simulation was performed for all the groups with CUF. The MUF cases were not simulated as voiding was observed in the experiment. For 21x21 mm, group numbers 1,2,3 was simulated and for 19x19 mm, group numbers 1,2,5,7 was simulated. Fig. 11 illustrates the warpage simulation results at 245°C whereas Fig. 12 illustrates the warpage simulation results at 25°C. Here the simulated and experimental warpage are compared for each group.

Geometry	Stress free temperature(° C)
Substrate, Die, interconnect	220
Mold	175
Lid and Lid epoxy	150

Table VI: Stress free temperature

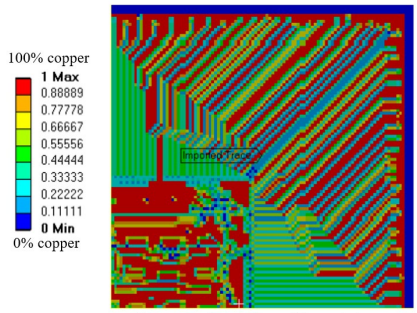


Fig. 10 Trace mapping

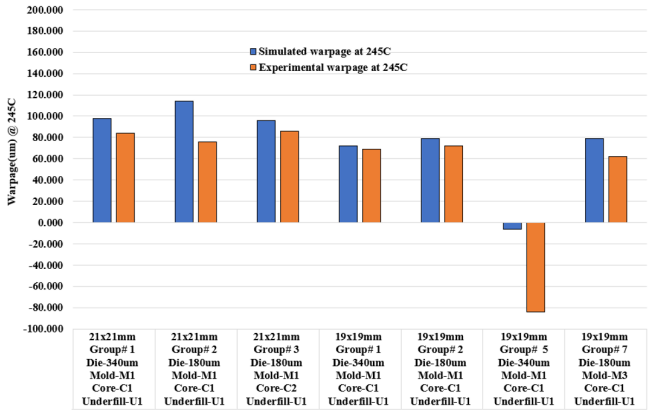


Fig. 11 Simulated and experimental warpage at 245°C

For the 245°C results, except group #5, all 21x21 mm and 19x19 mm warpage predictions errors are within 35um. Similarly, except group #5, warpage prediction errors are within 50um for the 25°C case. Overall, the prediction for 19x19 mm is better than the 21x21 mm . These differences in warpage can be attributed to factors highlighted earlier such as shrinkage effects of core/mold/build up layer, stress free temperature and residual strains from processing. The group# 5 which shows a large error is explored further. The reason for the large error in the warpage prediction for group# 5(bare die, no mold/Lid case) comes from the 220°C stress free temperature. This stress-free temperature represents the flip chip attach temperature. For group #5, the simulation predicts low warpages at 245°C (~10um) and high warpage at 25°C(~160um) which directly arises due to the respective temperature difference with the 220°C stress free temperature. However, the experimental measurements show a opposite warpage trend with 245°C warpage as the higher value than 25°C. It was also observed in experimental measurement that the zero warpage occurs around ~50°C suggesting the actual stress-free temperature to be different from the selected 220°C in the simulation. It is likely that the substrate lamination, chip attach and underfill attach may have relaxed the package to a new stress-free state. On the contrary, the selection of 220°C stress free temperature seems to work better for the molded groups as it relatively has a better match to the experimental measurement than group #5. It is likely that the addition of a large volume such as molding and lid attach, and its processing temperatures and residual strains maintained a high stress-free temperature for the die and substrate. The error in warpage prediction varied for different package size, package type and temperature. Overall, the simulation inputs required for the warpage prediction are strongly influenced by the package manufacturing process, which further complicates accurate warpage prediction.

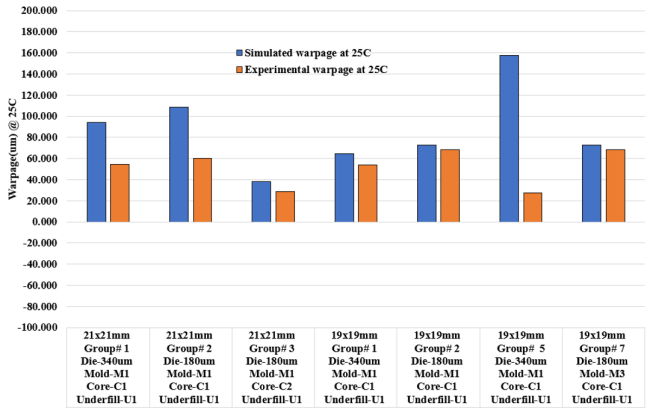


Fig. 12 Simulated and experimental warpage at 25°C

VI. Conclusion

Given the complexity of manufacturing processes, package structures, and material properties, numerical simulation still cannot fully replace traditional experimental methods. The experimental results indicate that among various factors, modifying the substrate core material is the most effective approach for controlling coplanarity. In lidded fcCSP package with a 21 x 21 mm body size and 0.3 BGA diameter, meeting JEDEC requirements for coplanarity remains a challenge for the industry, whereas the warpage criteria are easier to satisfy. In contrast, for packages with a 19 x 19 mm body size and 0.45mm BGA diameter, both coplanarity and warpage requirements are more easily met. Warpage simulation was performed, and the error in prediction was observed to vary across package size, package type and temperature. Comparison was performed between the molded and bare die package and the impact of stress-free temperature to warpage prediction errors and its dependence on manufacturing process was highlighted.

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