Additive Manufacturing of Interposers with Curved Vias

Tobias A. Schaedler, Kayleigh A. Porter, Alex C. Yu, Souren Soukiazian, Trevor Sasse, Erin S. Wernick,
Phuong P. Bui, Jacob M. Hundley, Mark R. O'Masta
HRL Laboratories, LLC
3011 Malibu Canyon Road
Malibu, CA 90265, USA
Email: taschaedler@hrl.com

Abstract

Additive manufacturing by digital light processing (DLP) has advanced rapidly, and micro-printers are now commercially available that use lens systems to expose arrays of 1920 x 1080 pixels of 2 µm x 2 µm size with ultraviolet (UV) light, while higher resolution printers with even smaller pixels are in development. Selective polymerization by localized UV curing on this scale enables microfabrication of features around 10 µm, while offering print rates sufficient for parts on the order of centimeters. In addition to UV curable polymers, ceramics can be additively manufactured by DLP, either by curing suspensions of ceramic particles or preceramic polymers. We present a novel interposer fabrication process based on additive manufacturing, whereby interposers can be created with near arbitrary routing of electrical signals. We first present the method to create a ceramic dielectric using micro stereolithography of a preceramic resin slurry. Then we explore the use of solder alloys with high capillary action to fill vias with aspect ratios greater than 100:1 by melt infiltration. Finally, we present two interposer demonstrations relevant to imaging applications, including ceramic interposers containing arrays of vias with diameters and pitches as small as 9 µm and 18 µm, respectively and sizes up to 2 cm x 2 cm x 0.7 cm. After melt infiltration of the vias with a copper indium solder, via resistivities as low as ~4 x 10-8 Ω·m were measured, close to 2X the international annealed copper standard. With our novel approach, we demonstrated two different interposer designs: 1) a curved interposer intended to connect a curved infrared detector with a planar read-out integrated circuit (ROIC); and 2) a fan-out interposer that spreads the pitch of an array of vias from 60 µm to 220 µm. These interposers require thousands of curved and angled vias, respectively, that cannot be realized using conventional microelectronics processing approaches. The unprecedented via routing enabled by this additive technology offers new packaging options for the 3D integration of microelectronic subsystems beyond imaging applications.

Key words

Additive Manufacturing, digital light processing, micro-printing, interposer, preceramic polymer, sensor integration

I. Introduction

Additive manufacturing promises increased design freedom, as well as a cost-effective prototyping capability [1, 2]. This is of interest to the broad field of semiconductor packaging and is relevant to current efforts towards 3D heterogeneous integration (3DHI), whereby different semiconductor devices and components are integrated in three dimensions to decrease subsystem size and increase performance [3]. 3DHI requires complex routing of signals and power, as well as advanced thermal management. In conventional packaging technologies, such as lithography, printed circuit boards (PCB), low temperature co-fired ceramic (LTCC) packages or high temperature co-fired ceramic (HTCC) packages, electrical routing is limited to vertical vias and horizontal traces with minimum via diameter and pitch determined by the selected fabrication process. Additive manufacturing methods are not similarly limited.

An example of a key component in semiconductor packaging that would benefit from increased design freedom is an interposer. Interposers are inserted between two electrical interfaces to reroute connections or spread them over different sized areas or pitches. An interposer comprises a dielectric material that defines the package envelop and prevents crosstalk between electrical traces made from highly conductive metals. The ability to design interposers

with curved and angled vias would enable electrical routing with greater complexity than presently possible.

Imaging sensors are one area that could utilize an interposer with complex routing. They often comprise a front detector portion that converts incoming light to electrons that are then collected and processed by a readout integrated circuit (ROIC) placed on the backside of the detector. For infrared focal plane arrays (FPAs), the detector device is processed from specialty compound semiconductors, such as indium gallium arsenide (InGaAs) or mercury cadmium telluride (HgCdTe), while the ROIC is a silicon-based chip. Therefore, detector and ROIC must be fabricated separately and then each pixel on the detector is electrically connected to the corresponding pixel on the ROIC. While smaller detector pixels are desirable for higher resolution, the one-to-one matching between detector and ROIC pixels limits the ability to increase individual pixel logic within the ROIC backplane. Placing an interposer with angled vias between the two layers would decouple the pixel pitches. This would allow for smaller detector pixels for increased resolution, while allowing the ROIC pixel footprint to grow for increased individual pixel logic. Furthermore, a ceramic interposer would be advantageous due to large processing and usage temperature ranges, as well as the low-vacuum compatibility needed for infrared imaging.

A second imaging application would be the ability to create a highly curved imaging surface. For wide field of view (FOV) imaging, a curved sensor offers improved resolution and illumination uniformity, while lowering optics complexity and decreasing size, weight and cost. [4, 5]. If only a hemispherical sensor could be fabricated, the volumetric efficiency becomes especially pronounced as the FOV increases, with up to 10X improvement expected over conventional flat sensor systems for 120° FOV imaging [6]. Multiple approaches to curve an image sensor have been pursued [5], but an interposer-based approach has not been reported previously. One distinct advantage to an interposer approach is that only the detector has to be customized and curved. This allows the use of standard flat ROICs, saving considerable cost and time to design and fabricate a new ROIC. The challenge is the interposer must be able to route the electrical signal from each pixel on the curved detector to the flat ROIC.

In the burgeoning field of using additive manufacturing for microelectronics packaging, most studies have focused on direct writing of conductive lines and dielectric layers on surfaces – either planar [7,8] or of complex shape [9]. Other studies have deposited dielectric to build a foundation or encapsulate conductive lines [10]. However, none of these methods are well suited for the complex routing of conductive lines throughout a dielectric volume, which is needed to create an interposer.

We present a novel interposer fabrication process, whereby interposers can be created with near arbitrary routing of electrical signals, with feature sizes down to 10 µm over a 2 cm x 2 cm x 0.7 cm volume [11]. We first present the method to create a ceramic dielectric using micro stereolithography of a preceramic resin slurry. Then we explore the use of electrically conductive solder alloys to fill the vias with aspect ratio of >100X. Finally, we present two interposer demonstrations relevant to imaging applications: the first containing curved interconnects to connect a curved detector with a planar ROIC (Fig. 1); and the second showing the ability to change pixel pitch from one side to the opposing side.

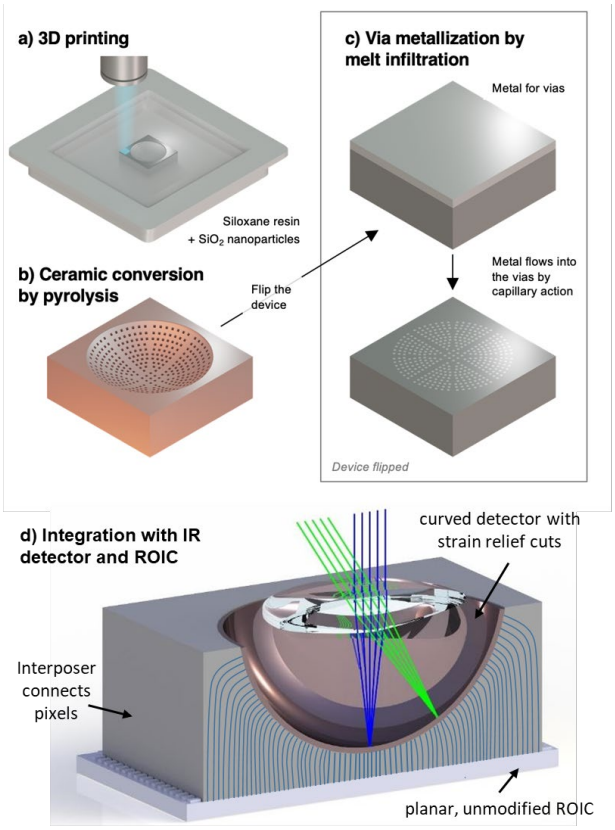


Fig. 1: Schematic of additive interposer fabrication

II. Experimental Procedures

A. Additive Manufacturing

A microArch® S230 printer (Boston Micro Fabrication) was used to 3D print samples via micro DLP. To this end, a projector with 1920 x 1080 pixels selectively exposed a 5 – 10 µm thin layer of resin, with UV light of 405nm wavelength. A lens system focused the pixels down to a size of 2µm x 2µm, resulting in an exposure area of 3.8mm x 2.2mm. By moving the build platform to expose adjacent areas along a 13 x 23 tile grid, this printer can build parts up to 50mm x 50mm in x and y, with the z-height limited to 50mm.

To deposit a new layer during 3D printing, the build platform of the printer dips down into a vat of resin and allows the resin to flow over the surface of the part. Then the platform comes back up and stops one layer height away

from the membrane that covers the vat surface. A roller moves across the membrane to ensure a uniform resin layer thickness. This active leveling system in the membrane-covered vat printer prevents the formation of a meniscus that would otherwise form at the resin-air surface in open vat 3D printers, which impacts the accuracy and flatness of the subsequent layer.

Print layer thicknesses of 5µm and 10µm were used. To print layers with 5µm thickness, an exposure time of 0.9 seconds was chosen with a UV intensity of 47 mW/cm^2, resulting in an energy dose of 42.5 mJ/cm^2. To print layers with 10µm thickness, an exposure time of 1.2 s was selected, with a UV intensity of 57 mW/cm^2, resulting in an energy dose of 68.4 mJ/cm^2.

Uncured resin was removed from the printed vias by applying a vacuum using a pump fitted with a syringe. The printed parts were cleaned further by a 10-minute sonication in an inert, low viscosity siloxane (Dynasylane 6490, Evonik) followed by another vacuum step. This process was repeated until all vias were clear. Further details about the UV curable resin have been reported previously [11].

B. Pyrolysis and Metallization

After printing and cleaning, the green parts were converted to a silicon oxycarbide (SiOC) ceramic, with silica particle inclusions, by a pyrolysis heat treatment in flowing argon gas. The pyrolysis schedule followed a heating rate of 1°C/min to 1000°C, a dwell for 30 min, and a cooling rate of 1°C/min to room temperature.

The empty vias within the ceramic interposer were then infiltrated with a custom metal alloy. Ingots of CuInTi and AgInTi solder were arc melted, and 1mm thick slices were cut off the ingots by electron discharge machining. Alloy slices were placed on top of the interposer for gravity assisted, capillary force driven melt infiltration. Metallization was carried out by heating at a rate of 3°C/min in vacuum to a temperature of 900°C, holding for 20 min and cooling at 3°C/min. Excess metal left at the surface was then removed by sanding. Finally, the metal-filled interposers underwent surface finishing processes. The planar interposer surfaces were subjected to lapping with progressively finer grit SiC papers, followed by a fine polishing with a 0.5 µm diamond suspension slurry. The curved interposer surfaces were polished with progressively finer diamond paste on a lathe with a polishing attachment.

III. Results And Discussion

A. Minimum Via Size and Pitch

Arrays of vertical vias, with different dimensions, were printed to determine the minimum via size and pitch achievable. Square vias, of a prescribed side length, were printed instead of round vias to better align to the square pixels of the printer. A via pitch to side length ratio of ~2:1 was used for most prints. Fig. 2a shows an optical image of an as-printed via array. Fig. 2b shows the same via array after conversion to ceramic. Conversion of the polymer to ceramic resulted in ~25% linear shrinkage, for a final pitch of 18µm and an average via side length of 9µm. These were the smallest values that could be achieved reliably for vertical vias. To account for the ~25% linear shrinkage during conversion from polymer to ceramic, a scale factor of 1.33 was applied to the print file.

Printing of fine-sized, angled vias was more challenging due to overcure effects. Some overcure in the depth direction is necessary to ensure adhesion of the cured resin to the underlying layer. However, the extent of it has to be minimized when printing non-vertical vias, so as not to close the volume that was intentionally not cured in the previous layer. The difficulty in resolving small via diameters and pitches increased with angle. Fig. 2c shows vias printed at a 45° angle, with approximately 12 µm side length. To adjust for the depth of overcure, the height (in the build direction) of the vias was increased resulting in a rectangular shape in the CAD file. The 10 µm print layer thickness introduced stair steps, with ~7.5 µm height, after shrinkage on pyrolysis (Fig. 2d).

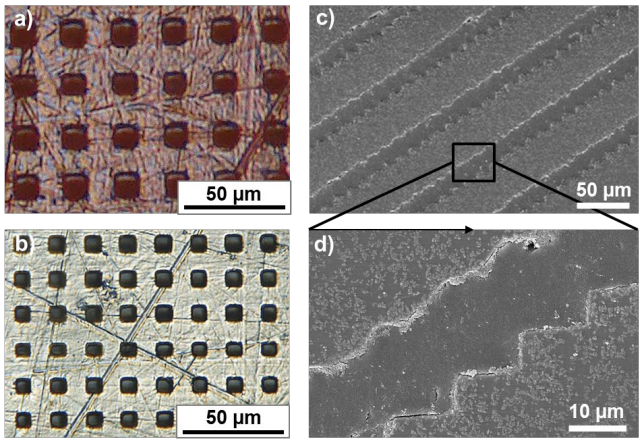


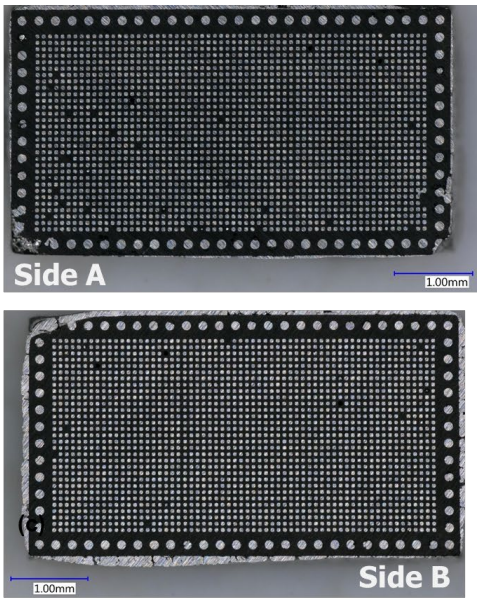
Fig. 2: Via-array in the as-printed state (a) and after conversion to ceramic, with a pitch of 18 µm (b). The sample was not polished before taking images. (c) Vias printed at a 45◦ angle. The vias are filled with epoxy resin from the mounting and polishing process conducted before imaging. (d) Angled via shows steps from print layers.

B. Metal Melt Infiltration

Silver- and copper-based alloys were chosen for melt infiltration studies, since they offer the highest electrical conductivities. Indium was added to lower the melting point, while maintaining good electrical conductivity. To infiltrate the vias well, a high capillary force, p_c, is needed. The capillary force is defined as

$$p_c = \frac{2\gamma cos\theta}{r} \quad (1)$$

whereby γ is the liquid to air surface tension, θ is the contact angle between the liquid and capillary, and r is the radius of the capillary. To reduce the contact angle between the liquid alloy and the silica surface oxide on the 3D printed interposer vias, titanium was added to the alloy. Titanium oxide has a higher free energy of formation than silicon oxide [12], and therefore the titanium in the molten alloy should react with the silicon oxide at the via surface to promote wetting and reduce the contact angle. Melt infiltration experiments were conducted with Ag – In alloys of equal at% and 1.5, 3 or 5 at% of Ti, as well as Cu – In alloys of equal at% and 1.5, 3 or 5 at% Ti. While good wetting of the 3D printed ceramic was observed for all alloys, higher Ti loadings more completely infiltrated 2.5 mm long vias with high aspect ratios (100:1). Differences between AgInTi and CuInTi were not statistically significant after the limited number of experiments.



	% Pass
Side A	99.4%
Side B	98.3%
Both Sides	98.1%

Fig. 3: Image analysis revealed that 98.1% of vias in a 2000 via array are fully metallized after melt infiltration.

We selected the alloy with 47.5 at% Cu, 47.5 at% In and 5 at% Ti for further metallization studies. Fig. 3 shows a metallized planar interposer with 2000 straight vias. A metallization yield of 98.1% was measured by image analysis.

C. Fabrication Quality

We measured via positional accuracy using a flat interposer, with a square array of vias on a nominal 81 µm pitch similar to the interposer shown in Fig. 3. After printing, pyrolysis, metallization and surface polishing, image analysis identified the via centroid locations to within ±0.5 µm, using a thresholding analysis method written in the Python programming language. A least squares calculation extracted the best-fit pitch. Fig. 4a shows the image analysis of the deviation from the intended via locations.

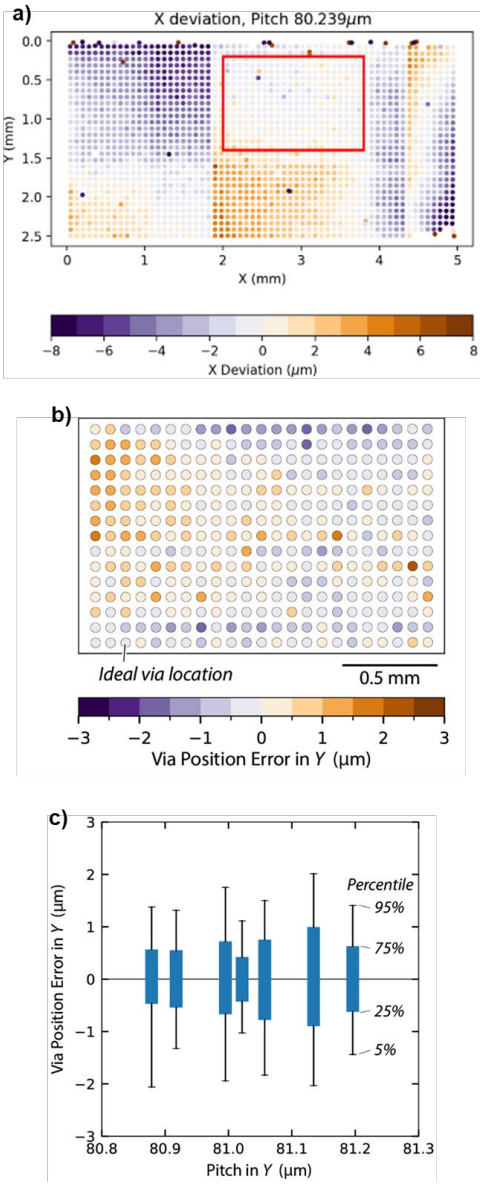


Fig. 4. Via positional error analysis.

Clusters of vias with similar deviation can be observed and correspond to print exposure areas. Position accuracy limitations of the printer's XY stage were found to cause via pitch deviations up to ±8µm when the stage moves to the next exposure area. However, within the center tile in Fig 4a (3.8x2.2mm marked with a red border) the via positional error relative to the best fit pitch is less than ±2µm as shown in Fig. 4b. This demonstrates the accuracy and fabrication quality without the error introduced by the printer's XY stage, which could be upgraded to a higher precision system. Fig. 4c compares the pitch and via error statistics for seven nominally identical interposers considering only one tile. The average pitch varied by <0.2%, and 90% of the vias were within ±2 µm of positional tolerance, with ~50% of the vias falling within measurement error.

D. Interposer Demonstrations

Two interposer demonstrations were designed to test the ability to produce fine pitch via arrays over centimeter sized areas, with relevance to imaging applications. The first design would enable connection of a curved detector to a planar ROIC to create a curved IR sensor, as shown in Fig. 1d. A cross-section of an as-printed polymer interposer section is depicted in Fig 5a showing the curved vias. A ceramic interposer with approximately 75,000 vias, is shown in Fig. 5b and a cross section in Fig. 5c. The central region of the interposer had a pitch of 30 µm that increased to 70 µm in the outer region, with an in-between region of 50 µm. This simulated a foveated imaging concept, containing a central fixation point with increased resolution. To balance print speed with required accuracy, the top half of the interposer was printed with a 5 µm layer thickness to resolve the curved vias, while the bottom half of the interposer, with relatively straight via sections, was printed at a 10 µm layer thickness. This reduced the print time to approximately 100 hours. Artificial porosity was placed at the edges and corners of the interposer to provide an escape path for gases evolving during pyrolysis and relieve internal stresses in the otherwise solid regions of the interposer.

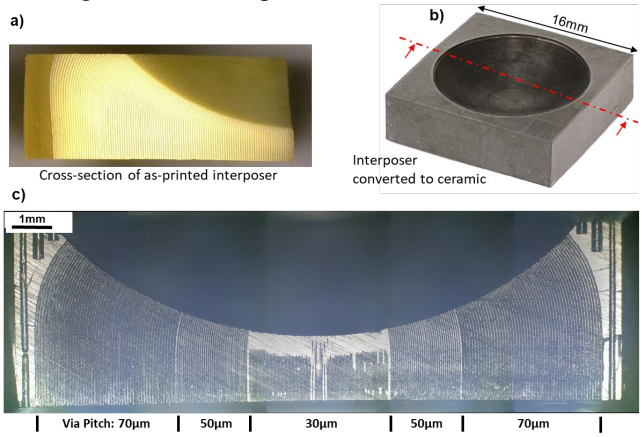


Fig. 5. Interposer prototype to connect a curved IR detector to a planar ROIC.

Earlier designs included 250 µm diameter vertical holes, which were replaced with a gyroid cellular architecture in later designs (Fig. 5b). While cracks can be observed at the edges in a cross-section of the earlier design (Fig. 5c), crack formation was mitigated with the finely distributed porosity of the gyroid structure.

After conversion to ceramic, the interposers were metallized, as described in Section II.B. Fig. 6a shows an optical micrograph of a cross-section after metallization. Residual metal from the infiltration can be seen at the planar bottom where the infiltration started. The melt infiltrated all the way to the curved side for nearly all vias. Because the vias are not fully aligned with the plane of the cross-section, they disappear and reappear when intersecting the cross-section, causing the pattern seen in Fig. 6a and in the center of Fig. 5b. In some locations the metal was pulled out of the vias during polishing, resulting in empty sections. Fig. 6b shows an optical micrograph of the flat side of the interposer. Fig. 6c shows a micrograph of the curved side of the interposer with 20 µm diameter vias at 40 µm pitch, and Fig. 6d shows a few of those vias at a higher magnification, where the composition was measured by EDS.

The composition of the ceramic phase was measured as 14 at% Si, 18 at% C and 68 at% O. EDS analysis measured a surface composition at the center of the via of 30.1 at% Cu, 14.9 at% In, 41.7 at% C, 11.5 at% O, 1.7 at% Si and 0.1 at% Ti. It is assumed that most of the measured C is due to surface contamination with hydrocarbons, the oxygen is due to surface oxidation and the Si is introduced during polishing. The composition of the infiltrated alloy is therefore assumed to be close to 67 at% Cu and 33 at% In, consistent with the observation that some In evaporated during the melt infiltration. This alloy composition is also consistent with the electrical resistivity reported below when assuming a rule of mixture and using bulk resistivities of 1.7×10^{-8} Ω·m and 8.2×10^{-8} Ω·m for Cu and In, respectively.

Only a trace of Ti was observed in the center of the via as almost all of the Ti migrated to the interface and reacted with oxygen from the ceramic. EDS analysis of the phase surrounding the interface measured a composition of 25.6 at% Ti, 30.2 at% O, 35.3 at% C, 7.5 at% Si, 0.7 at% Cu and 0.7 at% In.

As intended, the 5 at% Ti added to the CuIn alloy promotes wetting of the ceramic by reacting with it and forming titanium oxide at the interface. This reaction depletes the Ti in the alloy and explains why more complete infiltration of long, high aspect ratio vias was observed with higher Ti loadings. Since almost all the Ti ends up in the interfacial layer, detrimental effects of Ti on the electrical conductivity can be avoided.

A resistance of 0.1 – 0.5 ohm was measured for vias of different length resulting in an approximate electrical resistivity of the CuIn alloy of ~4×10^{-8} Ω·m. This is only ~2X the international annealed copper standard (IACS) value of 1.7×10^{-8} Ω·m.

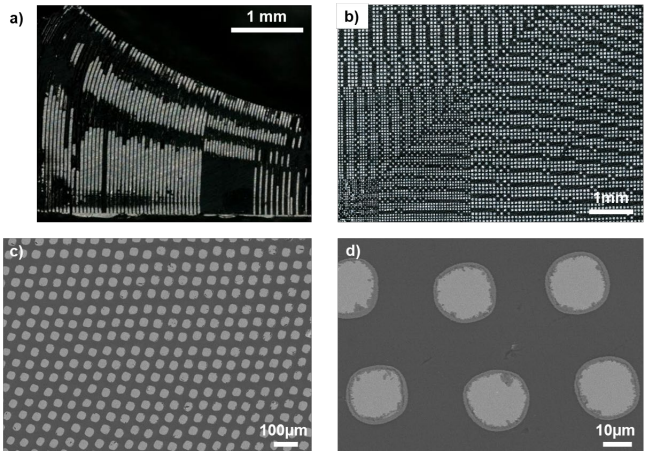


Fig. 6. Curved interposer after metallization. (a) Optical micrograph of cross section. (b) Optical micrograph of planar bottom. (c) SEM of curved bowl. (d) SEM of vias in curved bowl selected for EDS measurements.

The second design spread the via pitch from one side of an interposer to the opposing side (Fig. 7a). Such an interposer requires angled vias that would be infeasible to produce using conventional processing. An interposer was designed with two bundles of 22 x 45 vias separated by an 8 x 45 bundle that spread the pitch from the top to bottom surface. After conversion to ceramic, the via side length was 45 µm and the pitch was 60 and 220 µm at the top and bottom surfaces, respectively (Fig. 7b). The internal routing of the vias is observable in Figs 7c and 7d. A 47° maximum via angle from vertical was measured. The XCT images also show that the via side length opened wider along the bottom surface. This was to simulate a potential need for increased bonding surface area on the larger pitch side.

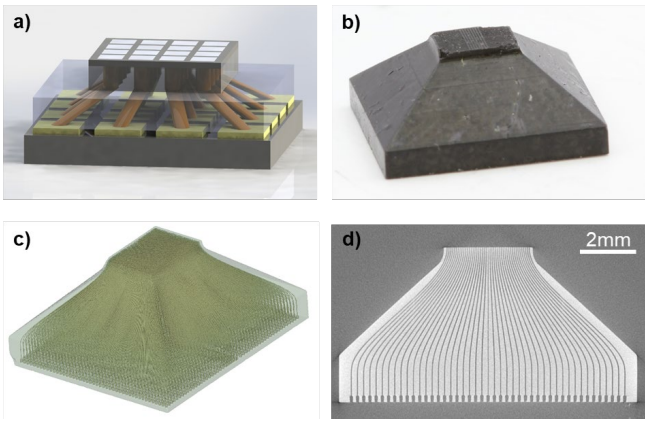


Fig. 7. (a) Concept of fan-out interposer spreading pitch from a sensor to a readout IC. (b) Picture of the 3D printed ceramic interposer after ceramic conversion. (c) Oblique view of the XCT reconstruction, where the interposer walls have been rendered translucent to reveal the internal via structure. (d) Cross-sectional XCT reconstruction, showing interposer walls (nearly white) and vias (grey).

The print lasted 66 hours. The 0.9 second cure time used for 5 µm layers in this study results in a peak printing rate of 2.3 x 10^6 voxels/second, comparing favorably with other approaches [13]. Additional time is required for applying new layers of resin, as well as moving the build platform to expose adjacent areas when printing larger parts. Including all these steps, an average print rate of 20 mm^3/h was typical for this study. This average print rate is two orders of magnitude faster than the rate of commercially available two photon lithography printers, which offer sub micrometer voxel sizes and can print similar preceramic resins [14].

E. Interposer Integration

Integration trials were carried out with planar interposers similar to the interposers shown in Fig. 3. Two integration methods were pursued, conventional single sided indium bump bonding and small pitch integrated knife edge (SPIKE) bonding [15]. Fig. 8 shows a planar interposer bonded to a fan-out chip by single-sided indium bump bonding and a test chip by SPIKE bonding. The via positional error described in Fig. 4 limited successful registration and electrical connection to the area of a single 3D printing exposure tile. Therefore, the test chip covers only one corner of the interposer. Registration of vias beyond the exposure tile in this corner was not feasible due to the positional error. But within the corner area connectivity checks and electrical testing were successful for the majority of the vias. This experiment demonstrates that 3D printed parts can be integrated with conventionally fabricated semiconductor chips.

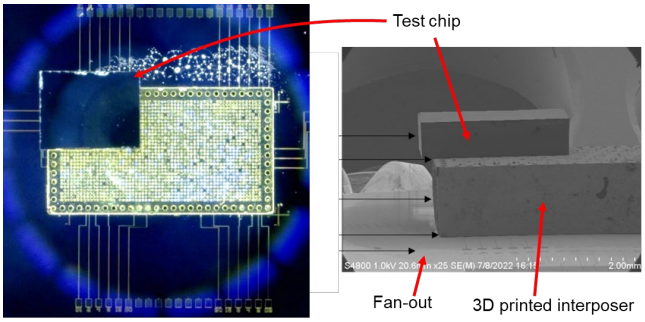


Fig. 8. Integration of 3D printed interposer with conventionally fabricated chips by single sided indium bump bonding and SPIKE bonding.

IV. Conclusion

This paper introduces an additive approach to interposer fabrication that offers flexible electrical routing, including curved and angled vias. A siloxane based preceramic resin was formulated for UV curing in a micro DLP printer. Interposers were printed and converted to a $SiOC/SiO_2$ ceramic composite by pyrolysis heat treatment. The vias were then metallized by melt infiltration with a CuInTi solder alloy followed by surface finishing. A minimum via

pitch of 18µm was demonstrated for short vertical vias and a range of 30µm – 70µm pitch for curved vias with aspect ratios up to 150:1. The vias were metallized and exhibited a resistance of ~4 x 10^{-8} Ω·m, which is within the same order of magnitude as silver and copper. The results demonstrate that the electrical routing limitations of conventional packaging approaches can be overcome, enabling 3D integration of microelectronic subsystems, such as a curved IR FPA.

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