Enhancing Efficiency in Packaging Substrate Reliability Evaluation Through AC Electrical Resistivity Measurement

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Abstract
The reliability assessment of packaging substrates is essential for both the design and quality control of electronic devices. However, such evaluations often involve prolonged testing periods, which potentially impede the development and optimization of substrates. In this study, two distinct substrates were fabricated with identical circuit designs and layered materials, differing only in the manufacturing processes of their microvias used for interconnection. Substrate A exhibited a higher void fraction at the microvia bottom than substrate B. Both substrates were subjected to thermal shock testing under cyclic conditions of -55°C for 15 min followed by 150°C for 15 min, with testing continued for over 1000 cycles. Electrical resistance was continuously monitored using either an alternative current (AC) or a direct current (DC)), with voltage measurements taken accordingly. A circuit was considered to have failed when its resistance first reached an infinite value. Failed cycle numbers were further analyzed using a Weibull plot. The results indicated that both AC and DC measurement consistently demonstrated lower reliability for substrate A compared to substrate B. However, the cumulative failure rate F(10%) was observed to be shorter when measured using AC than with DC. These findings indicate that AC-based resistance monitoring resulted in an approximately 25% reduction in testing duration for both substrates compared to DC-based measurements. This study suggests that switching from DC to AC electrical resistance measurements can significantly shorten reliability evaluation periods while maintaining assessment accuracy.

Key words
Microvia, reliability, thermal shock, direct current, alternative current

I. Introduction
With the transition from post-5G to 6G, the rapid advancement of an increasingly information-centric society—driven by the widespread adoption of artificial intelligence (AI) and internet of things (IoT) and other digital technologies—is accelerating. As modern lifestyles and industrial activities become ever more dependent on massive volumes of rea-time data, the underlying infrastructure must evolve accordingly. From digital communication frameworks, such as base stations, servers, and high-speed network systems that form the social and industrial backbone, to high-performance consumer electronics like smartphones and wearable devices with computational capabilities rivaling those of personal computers, all electronic hardware is now expected to be highly compact, energy-efficient, and capable of high-speed, low-latency data transmission and reception. network systems and equipment serving as social backbones, to advanced consumer devices like smartphones with computing capabilities comparable to personal computers, all electronic hardware is now expected to be compact, energy-efficient, and capable of high-speed, low latency data transmission and reception.

In parallel with this technological shift, the role of packaging substrates—key structural and functional elements that enable interconnection and integration of semiconductor devices—has become increasingly critical. The performance, integration density and thermal-electrical reliability of packaging substrates directly influence the overall

functionality and durability of next-generation electronic systems. To meet the rapidly evolving technological demands, the design and development of next-generation packaging substrates must progress at an accelerate pace, incorporating finer wiring, smaller microvias, and multilayered architecture, while maintaining mechanical and electrical robustness under harsh operating environments. Ensuring the reliability of such advanced substrates requires not only the reproduction of failure modes that reflect realistic field-use conditions but also the establishment of reliability assessment methods that are both accurate and efficient in terms of test duration and cost. Conventional reliability evaluation techniques are typically time-intensive, making the identification of timesaving yet equally reliable methods a critical challenge for industry stakeholders. To address this, standardized reliability test protocols have been established by organizations such as the Institute for Interconnecting and Packaging Electronic Circuits (IPC) and JEDEC Solid State Technology Association (JEDEC). Among the various testing methodologies, the thermal cycling test (TCT) is one of the most widely employed due to its ability to simulate mechanical fatigue caused by temperature fluctuations, which is a dominant failure mechanism in multilayered electronic assemblies.

In our previous work, we investigated the impact of reflow treatments—which are commonly performed before TCT—on reliability outcomes [1]. Additionally, to reduce variability caused by pre-test environmental factors, we examined the role of pre-test baking process and experimentally evaluated how its application influences TCT results using two identical packaging substrates with differing interconnection reliability [2].

Building upon these foundational investigations, the present study explores failure detection methods based on increases in electrical resistance, comparing AC and DC measurements, and evaluating their effectiveness in terms of shortening overall test duration. This approach aims to identify an efficient yet reliable failure detection method that aligns with the accelerating pace of next-generation substrate development.

II. Experimental Section

A. Two distinct substrates

A 45 mm x 45 mm substrate featuring six daisy chain regions arranged along its diagonal was employed in this study, as illustrated in Fig. 1(a). Each daisy chain region includes a three-layer stacked micro-via structure on both sides of the substrates electrically interconnected through plated through-holes (PTHs) to form a daisy chain array, as shown in Fig. 1(b). The position of the 1st, 2nd and 3rd microvia layers are indicated in Fig. 1(c). Each daisy chain comprises a total of 98 such arrays and the diameter of microvia is 70/60 μm.

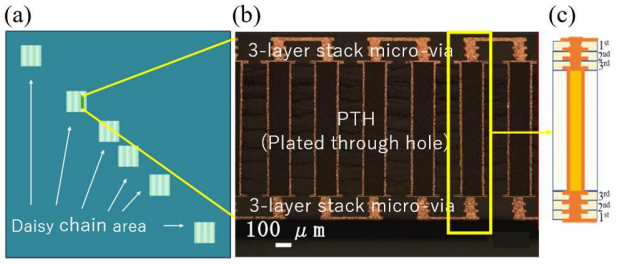

Fig. 1 Substrate design: (a) top view and (b) cross-section view of the daisy chain region, and (c) positions of the 1st, 2nd and 3rd microvia layers.

Two distinct substrates were fabricated with identical circuit design and layered materials, differing in the manufacturing processes of their 1st and 3rd layer microvias used for interconnections. Substrate A exhibited a higher void fraction at these microvia bottoms than substrate B as the field-emission scanning electronic microscopy (FE-SEM) images shown in Figure 2.

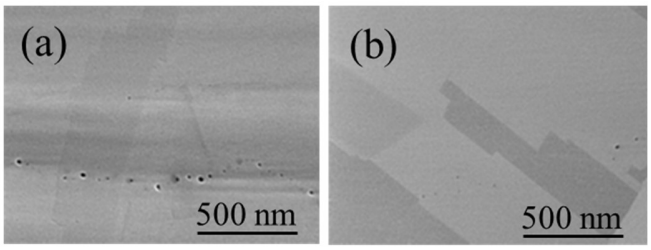

Fig. 2 FE-SEM images of the microvia bottom of the 1st and 3rd layer in (a) substrate A and (b) substrate B.

B. Initial electrical resistance measurement

The electrical resistance was measured using both AC and DC methods in the initial state. AC measurements were performed using a battery tester (MT3563A, Hioki E.E Corp.) with an alternating measurement current at a frequency of 1kHz, while DC measurements were conducted using a resistance meter (RM3545, Hioki E.E. Corp.) with a direct measurement current of 1 mA.

C. TCT

Six specimens, each of substrate A and substrate B were subjected to TCT evaluation using TCT reliability testers (TSA-101, ESPEC Corp.). The TCT condition followed JEDEC standard No. 22-A104E, Temperature Cycling Condition H, consisting of cycling exposure between -55°C for 15 minutes and 150°C for 15 minutes. For each substrate type, three specimens were evaluated under AC conditions using an AMR-280-UA system (Espec Corp.) for 1600

cycles at an AC frequency of 1kHz with a measuring current of 1mA. The remaining three specimens were evaluated under DC conditions using an AMR-280 (Espec Corp) for 1100 cycles, also with a measuring current of 1 mA. Electrical resistance measurements were conducted using the four-probe method. Both AC and DC tests were terminated when approximately two-thirds of circuits in Substrate A failed, providing sufficient data for subsequent Weibull analysis. The electrical resistance measurement interval is every one minute with a one ampere measurement current. A daisy chain circuit is "failed" when the electrical resistance value becomes more than 2 times higher than its initial value at the same temperature, and the number of cycles is recorded as the number of failed cycles. Figure 3 shows an example of the criteria used to judge failure.

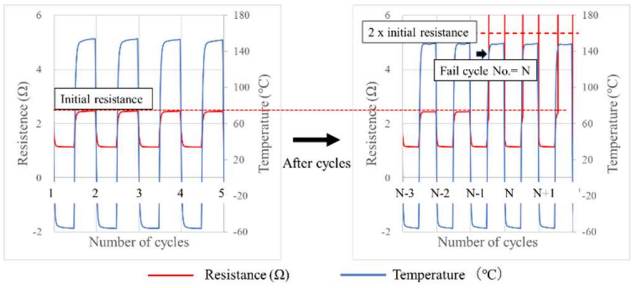

Fig. 3 Determination of failure cycles.

III. Results and Discussion

A. Initial electrical resistance measurement

The electrical resistance of the same specimens (comprising six daisy chain regions) of substrate A and substrate B, measured under ambient using both DC and AC measurement, is listed in Table 1. No significant difference in electrical resistance was observed between AC and DC measurement methods.

Table 1 Initial electrical resistance of substrates A and B.

		Measurement Method	
	Circuit No.	DC (Ω)	AC(Ω)
Substrate A	1	1.735	1.741
	2	1.755	1.761
	3	1.709	1.716
	4	1.685	1.692
	5	1.611	1.618
	6	1.434	1.441
Substrate B	1	1.485	1.490
	2	1.553	1.557
	3	1.594	1.598
	4	1.601	1.604
	5	1.573	1.576
	6	1.518	1.522

B. Test duration difference between DC and AC measurement

The number of failed cycles was analyzed using Weibull distribution plots, as presented in Figure 4. The cumulative failure rates were calculated using the median rank method, which estimates the unreliability based on the sequence of failure events. Both the AC and DC resistance measurement yielded consistent trends as shown in Figure(a) for AC and Figure 4(b) for DC, Substrate B demonstrated higher reliability than Substrate A under both measurement conditions. This suggests that the improved reliability of Substrate B is independent of the measurement method. Notably, a comparative analysis of the cycle counts corresponding to a cumulative failure rate of 10%(F(10%)) reveals a difference between AC and DC conditions. Specifically, the F(10%) value for the AC measurement occurred at a lower cycle count compared to the DC measurement, indicating that failures were detected slightly earlier under AC monitoring. For example, Substrate exhibited an F(10%) at 355 cycles under AC conditions, whereas under AC conditions, whereas under DC conditions, the same cumulative failure rate occurred at 448 cycles. Similarly, Substrate B showed an F(10%) of 890cycles with AC measurement, in contrast to 1131 cycles under DC. This trend implies that the AC measurement method may be more sensitive to early resistance changes in the daisy chain circuits during thermal cycling. Although the cause of this higher sensitivity remains unclear, it is worthwhile to investigate the underlying mechanism in future studies to better understand the impact of measurement mode on failure detection sensitivity.

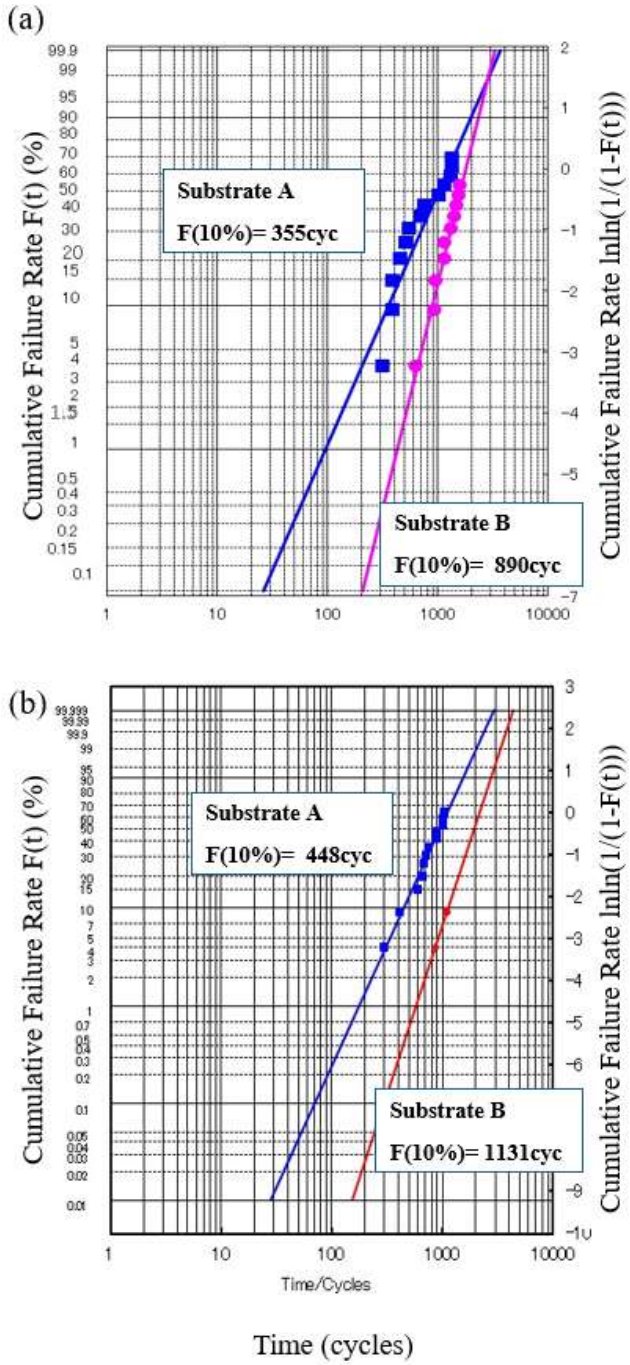

Fig. 4 Weibull plots of failed TCT cycles of (a) AC measurements and (b) DC measurements.

IV. Summary

This study evaluates the TCT reliability of two distinct packaging substrates that differ in their microvia formation processes. Initial electrical resistance measurements conducted under ambient conditions using both AC and DC methods showed no significant differences attributable to the measurement method. Weibull analysis of the failed cycles revealed that Substrate B exhibited higher reliability than Substrate A under both AC and DC monitoring. However, failures were detected earlier with AC measurements. Specifically, the F(10%) occurred approximately 20-25% earlier under AC monitoring compared to DC.

These findings indicate that AC-based resistance monitoring can reduce the required test duration by approximately 25% for both substrates, relative to DC-based measurements. Although the consistency of failure modes for the same substrate under different measurement methods (AC and DC) requires further confirmation, and the underlying mechanism by which AC exhibited higher sensitivity remains to be elucidated, this study suggests that switching from DC to AC electrical resistance measurements may significantly shorten reliability evaluation periods while maintaining assessment accuracy.

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