Electromigration Challenges in FCQFN Packaging: Impact of Solder Thickness and Shape on Reliability

Min-Yan Tsai[1], Shan-Bo Wang[1], Yung-Sheng Lin[1], Christophe Zinck[2], Antonio Zuccaro[3], G. Livio Gobbato[4], Chen-Chao Wang[1], and Chih-Pin Hung[1]
1. Advanced Semiconductor Engineering Inc. (ASEKH), Kaohsiung, Taiwan.
2. Advanced Semiconductor Engineering Inc. (ASEEU), Waterloo, Belgium.
3. STMicroelectronics, Catania, Italy.
4. STMicroelectronics, Agrate Brianza, Italy.
Email: BrianMY_Tsai@aseglobal.com

Abstract

A specially-designed flip-chip quad flat no-lead (FCQFN) package test vehicle featuring Cu pillar interconnects was investigated for the electromigration (EM) study to meet the high-reliability requirement for high-power automobile applications. The microstructure and electrical performance of these Cu pillar interconnects were examined, focusing on variations in plated solder thickness and interconnect geometry under extreme EM conditions. The interconnects were stressed at a current density of 20 kA/cm^2 at 180˚C environmental atmosphere, accompanied by *in-situ* electrical resistance monitoring. Variations in electrical resistance were correlated with the microstructural evolutions. The electrical resistance exhibited a 100% increase compared to the initial value, while the SnAg solder within the Cu pillar interconnects was entirely consumed and subsequently transformed into Sn-based intermetallic compounds (IMCs). Additionally, a polarity effect was observed in the Cu pillar interconnects, influenced by varying electron flow directions. To optimize the EM performance of the Cu pillar interconnects, the effects of plated solder thickness and interconnect geometry on EM behavior were systematically evaluated. It was found that a reduced solder volume contributed to a superior lifetime, attributed to the rapid formation of a complete IMCs structure from microstructural analyses. Furthermore, a specially designed modification to the Cu pillar interconnect structure demonstrated potential for enhancing EM performance based on both microstructural and simulation analyses. The results and findings presented in this study provide valuable design guidelines for FCQFN packages in the future, especially regarding enhancing interconnect reliability.

Key words

Electromigration Test, EM, FCQFN, Microstructure, Reliability, Solder Thickness

I. Introduction

The flip-chip quad flat no-lead (FCQFN) packaging has recently garnered significant attention in the field of electronic devices, particularly for high-power and automotive applications. This specialized packaging technique utilizes flip-chip solder interconnects bonded to copper lead frames, in contrast to traditional wire bonds. This approach not only enhances electrical performance by minimizing parasitic resistance and inductance, but also facilitates a more compact device design due to the absence of wire bonds, leading to improved heat dissipation. Moreover, the chip-to-package ratio of FCQFN technology is the closest to that of wafer-level chip-scale package (WLCSP), resulting in fewer defects during assembly and simplified manufacturing [1], [2]. However, the increasing demand for power load capacity and performance within the power management market for FCQFN devices raises significant reliability concerns, such as cracking and delamination under temperature cycling test (TCT), highly accelerated stress test (HAST), high temperature storage test (HTST), and most critically, electromigration (EM) [3], [4].

EM, triggered by the electron wind force, generally induces enhanced diffusion behavior of metal atoms along the direction of electron flow at a high operating temperature. Recent studies on fine-pitch and small line width copper redistribution layers (Cu RDLs) have been reported for a severe voiding issue as a result of the combinational thermal Joule heating effect and athermal electron wind force effect [5], [6]. In addition to the similar EM-induced void formation in Cu interconnects, the polarity effect has been identified, characterized by void formation on the cathode side and hillock formation on the anode side. This phenomenon has been investigated through *in-situ*

observations using scanning electron microscopy (SEM) in both Cu RDLs and Cu tall pillar/via interconnects [7]–[10]. Furthermore, numerical modeling incorporating microstructural characteristics has been explored to enhance the understanding of EM in Cu RDLs [11].

Although the EM-induced behavior observed in pure copper is characterized by enhanced diffusion, solder interconnects within WLCSP or FCQFN not only exhibit diffusion-control processes but are also predominantly influenced by diffusion-related interfacial reactions [12], [13]. The operating temperature and applied current density are critical parameters in evaluating the EM reliability. These driving forces promote increased interdiffusion across the solder/metallization interface and dissolution of the Under Bump Metallization (UBM) into the solder matrix. Several failure mechanisms have been identified for solder interconnects in various UBM/solder systems under high current stressing. These include the Joule heating-induced thermal degradation, severe voiding enhanced by current crowding, and the formation of intermetallic compounds (IMCs), all of which can significantly compromise interconnect reliability and may ultimately result in device failure. Therefore, it is essential to conduct a comprehensive assessment of the EM reliability and failure mechanisms related to FCQFN packaging. Our laboratory has previously proposed a typical EM behavior and prediction model for the Cu pillar interconnects within the FCQFN package [3], [13]. In this study, the time-dependent microstructural characteristics will be investigated in detail. Furthermore, optimizing the design of copper pillar interconnects—through geometry modifications—is essential to ensure their performance and reliability in high-power applications.

II. Experimental Procedures

A. Test Vehicle and Electromigration Test

In this study, specially designed FCQFN package test vehicles featuring spherical Cu pillar interconnects with diameters of either 80 µm or 100 µm were investigated to evaluate the EM performance. The multi-layered Cu pillar interconnects were constructed with a Cu/Ni/Sn1.8Ag configuration and were bonded on an Ag-plated Cu alloy lead frame, as shown in Fig. 1. The thickness of the multi-layered UBMs were 30 µm for Cu pillar, 3 µm for Ni metallization, and varied thickness of 27 µm, 37 µm, and 47 µm for plated Sn1.8Ag alloy. The incorporation of the Ag intermediate layer was specifically aimed at enhancing the quality of flip-chip bonding between Cu pillar interconnects and Cu alloy lead frames. Following the reflow process, the FCQFN package was subsequently mounted onto a printed circuit board (PCB) using SAC305 solder through surface mount technology (SMT). The PCB was specially designed to connect the MIRA test system (Qualitau Inc.) for board-level EM testing.

The EM experiment was conducted at 1–1.6 A, corresponding to approximately 20 kA/cm^2, and at 180˚C in an environmental chamber, as presented in Table I. To assess the EM reliability of the interconnects, the variation in electrical resistance during the current stressing was monitored *in-situ*, using a Kelvin structure to enhance measurement accuracy. The temperature change of the Cu pillar interconnects, resulting from the thermal Joule heating effect, was estimated using a temperature coefficient of resistance (TCR) method from the MIRA tester. The EM test was conducted until a 100% increase in electrical resistance compared to the initial value of the as-fabricated interconnect.

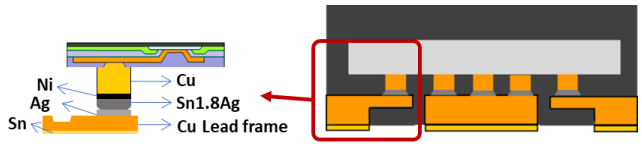

Fig. 1. Schematic diagram of the FCQFN package and Cu pillar interconnects used in this study

Table I. Cu pillar interconnects of the FCQFN package and EM test conditions in this study

Diameter (µm)	Sn1.8Ag Thickness (µm)	Sche-matic	Temp. (˚C)	Current (A)	Current Density (kA/cm^2)
80	27		180	1	20
80	37		180	1	20
80	47		180	1	20
100	37		180	1.6	20

B. Microstructures Analysis

The microstructures of the Cu pillar interconnects were investigated using a scanning electron microscope (SEM), complemented by energy-dispersive X-ray spectroscopy (EDS) for the characterization of IMCs. The analysis focused on Cu pillar interconnects that exhibited electrical resistance increases of 10%, 50%, and 100% compared to the initial resistance of the as-fabricated interconnect. Proposed mechanisms were correlated with the resistance changes and their relationship to the evolving microstructures.

C. Finite Element Method Analysis

A 3D finite element method (FEM) model was employed using COMSOL Multiphysics® to analyze the phenomena observed in the microstructure of the Cu pillar interconnects within the FCQFN package. Electro-thermal-mechanical coupling simulations was conducted to assess temperature and stress, aiding in the evaluation of the steady state during the initial phase of the EM experiment.

III. Results and Discussion

A. Microstructures Analysis

Fig. 2 shows the microstructures of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnect with an 80 µm diameter after SMT. Notably, the Cu pillar interconnect exhibits a conical shape, contrasting with the typical bow shape observed in most Cu pillar interconnects. This difference can be attributed to the asymmetrical solder reaction that occurs between the 80 µm diameter Cu pillar interconnect and the 100 µm diameter plated Ag intermediate layer on lead during the reflow process. The as-fabricated interconnect exhibited a thin IMC of Ni_3Sn_4-based at the Cu pillar/Ni/Sn1.8Ag interface, along with a scallop-type Ag_3Sn at the Sn1.8Ag/Ag/Cu lead frame interface. A rapid depletion of the plated Ag intermediate layer was contrasted with the remaining Ni metallization, which can be attributed to the differing dissolution and reaction rate of Ag or Ni atoms in the SnAg solder. Additionally, the microstructure and EDS analysis of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnect with a 100 µm diameter are shown in Fig. 3. The bow shape of this Cu pillar interconnect indicates a symmetrical solder reaction between the 100 µm diameter Cu pillar interconnect and plated Ag intermediate layer during the reflow process. The distribution of each element, as shown in the EDS mapping, reveals a similar morphology of IMCs as observed in the Cu pillar interconnects with an 80 µm diameter.

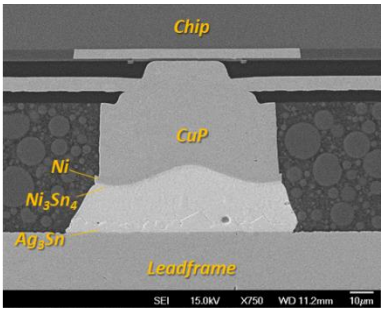

Fig. 2. Microstructure of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnect with an 80 µm diameter after SMT.

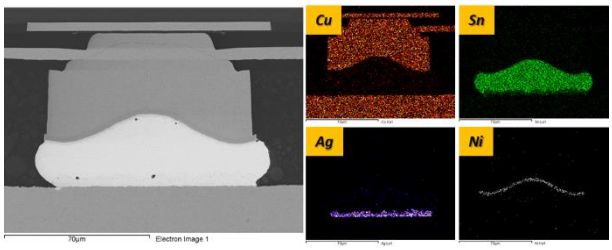

Fig. 3. Microstructure and EDS analysis of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnect with a 100 µm diameter after SMT.

After the EM test, the microstructures were influenced by the electron flow and elevated temperatures, resulting in distinct electrical resistance responses during the test. Fig. 4 shows the microstructures of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnect with an 80 µm diameter after continuous stressing with electron flow direction from the chip to the lead frame (downstream electron flow direction). This interconnect was subjected to a current density of 20 kA/cm² at 180˚C, with varying resistance increases compared to the initial value of the as-fabricated interconnect. The Sn1.8Ag solder gradually transformed into $(Cu,Ni)_3Sn$, $(Cu,Ni)_6Sn_5$, $(Ni,Cu)_3Sn_4$, and Ag_3Sn IMCs, which contributed to a rapid increase in resistance recorded during the early-stage of the EM test at a 10% resistance increase. Significant cracks appeared when the resistance increased by 50%, coincided with substantial IMCs formation and associated volume shrinkage. When the resistance reached a 100% increase, the Sn1.8Ag solder had completely transformed into IMCs, revealing pronounced void formation. It's worth noting that the formation of Kirkendall voids occurs in the regions of $(Cu,Ni)_3Sn$ on the Cu pillar side and Cu_3Sn on the lead frame side, respectively. The fracture morphology, characterized by the presence of numerous tiny voids, can significantly deteriorate mechanical properties.

The microstructures of Cu pillar interconnects demonstrated divergent behaviors depending on the direction of electron flow, as observed in our previous study [3]. Fig. 5 shows the microstructure of the Cu pillar interconnects with an 80 µm diameter after an electron flow direction from the lead frame to the chip (upstream electron flow direction), as well as current-bypass with pure 180˚C aging, within the same FCQFN package shown in Fig. 4 (b). In the case of the interconnects with upstream electron flow direction, the Ni layer maintained its original shape, showing only slight consumption when compared to interconnects with downstream electron flow direction. Meanwhile, the $(Ni,Cu)_3Sn_4$ IMC was formed near the Ni UBM on the Cu pillar. Conversely, the interconnect with the downstream electron flow direction exhibited the $(Ni,Cu)_3Sn_4$ IMC near the Cu alloy lead frame side, rather than adjacent to the Ni UBM. A typical polarity effect that occurred during the EM test was proposed to explain the difference in IMC types formed at the interfaces. The current-bypass interconnects experienced only inter-diffusion driven by thermal aging. It's worth noting that the microstructure of current-bypass interconnects was similar to the interconnects with an upstream electron flow direction. Overall, the total IMC thickness in interconnects with upstream electron flow was slightly greater than that in the current-bypass interconnects.

Fig. 6. shows a summary of microstructures of Cu pillar interconnects with an 80 µm diameter after the EM test under a 20 kA/cm^2 at 180˚C. The observed 100% increase in resistance was associated with significant voids formation in each Cu pillar interconnect, which can be partially attributed to the loss of brittle intermetallic compounds (IMCs) during

the cross-sectional samples preparation. Notably, clear morphological variations were observed over time in relation to the increasing resistance, which was accompanied by changes in the volume of IMCs, the presence of cracks, and the formation of Kirkendall voids. The effects of polarity and void formation are detrimental to interconnects, ultimately compromising the overall reliability of the package.

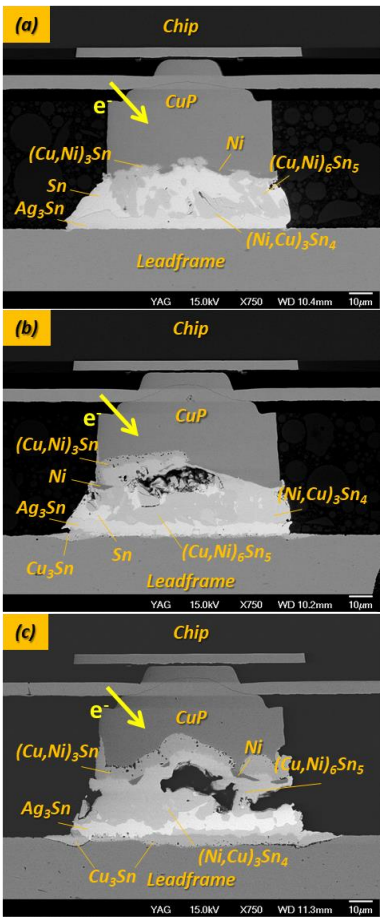

Fig. 4. Microstructure of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnects with an 80 µm diameter after downstream electron flow direction continuous stressing at 20 kA/cm^2 and 180˚C: (a) 10% resistance increase; (b) 50% resistance increase; (c) 100% resistance increase.

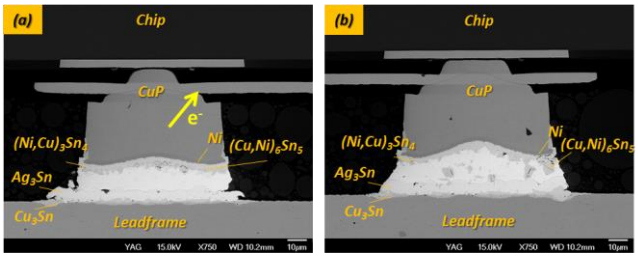

Fig. 5. Microstructure of other Cu pillar interconnects within the same FCQFN package as Fig. 4 (b): (a) interconnect with upstream electron flow direction; (b) current-bypass interconnect under pure 180˚C aging.

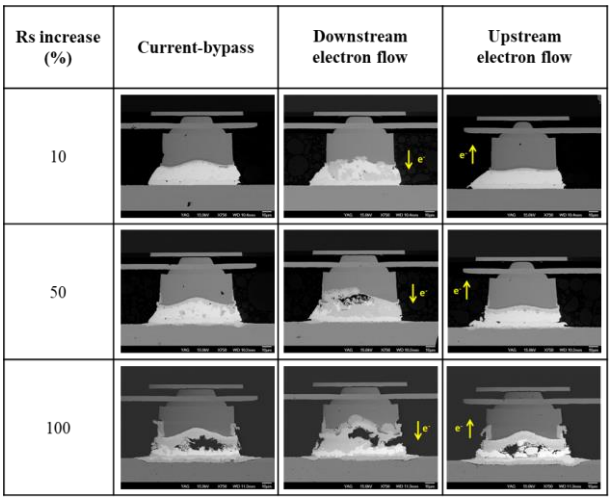

Fig. 6. Summary of the microstructure of the Cu/Ni/37 µm Sn1.8Ag/Ag/lead frame Cu pillar interconnects with an 80 µm diameter after EM test under a 20 kA/cm^2 and 180˚C.

B. Solder Thickness Analysis

In order to evaluate the impact of solder thickness on EM performance, the Cu pillar interconnects with various solder thicknesses were compared in different FCQFN packages. Fig. 7 shows the log-normal distribution of time to failure (TTF) for Cu pillar interconnects with solder thickness of 27 µm, 37 µm, and 47 µm after the EM test under a 20 kA/cm^2 at 180 ˚C. Fig. 8 shows the corresponding microstructure of the Cu pillar interconnects associated with the initial failure shown in Fig. 7. Notably, substantial voids in the Cu pillar interconnects were observed in the microstructure images during sample preparation, as depicted in Fig. 6. The mean time to failure (MTTF) for Cu interconnects with a solder thickness of 27 µm was longer compared to those with solder thicknesses of 37 µm and 47 µm, based on a 10% increase in resistance, as shown in Fig. 7 (a). The microstructure of Cu pillar interconnects with a solder thickness of 27 µm exhibited the least residual solder volume after the EM test, as shown in Fig. 8 (a) to (c). This observation suggests that the rapid formation of a complete IMC structure is beneficial for enhancing EM performance. It is believed that a fully developed IMC structure in the Cu pillar interconnect contributes to enhanced resistance against EM and immortality [3]. Regardless of solder volume, all interconnects exhibited a similar failure mode, as indicated by the log-normal distribution following the EM tests.

However, a different slope was observed in the log-normal distribution of TTF for Cu pillar interconnects with a solder thickness of 47 µm, compared to those with thicknesses of 27 µm and 37 µm, based on a 50% increase in resistance, as shown in Fig. 7 (b). This observation suggests a variation in the failure mode during prolonged continuous current stressing, transitioning from a 10% to a 50% resistance increase. The microstructure of Cu pillar interconnects with

solder thickness of 47 µm exhibited a consecutive growth of voids at the interface between the solder and the Cu/Ni pillar, as shown in Fig. 8 (f). This distinct failure mode resulted from a significant flux of Sn from the solder, attributed to the larger solder volume in the Cu pillar interconnects with 47 µm solder thickness. The large-volume Sn atoms reacted with Cu atoms to form IMCs, leading to volume shrinkage. Variability in atomic flux delayed the timely replenishment of voids, contributing to voids growth. Consecutive voids formation is detrimental to interconnects and can eventually lead to open-circuit failure under prolonged electrical stressing.

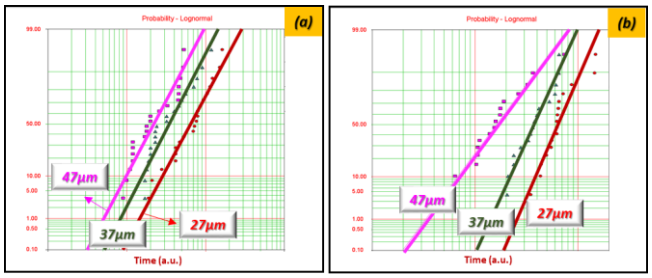

Fig. 7. Log-normal distribution of TTF for the Cu pillar interconnects with solder thicknesses of 27 µm, 37 µm, and 47 µm after the EM test under a 20 kA/cm^2 at 180˚C: (a) 10% resistance increase; (b) 50% resistance increase.

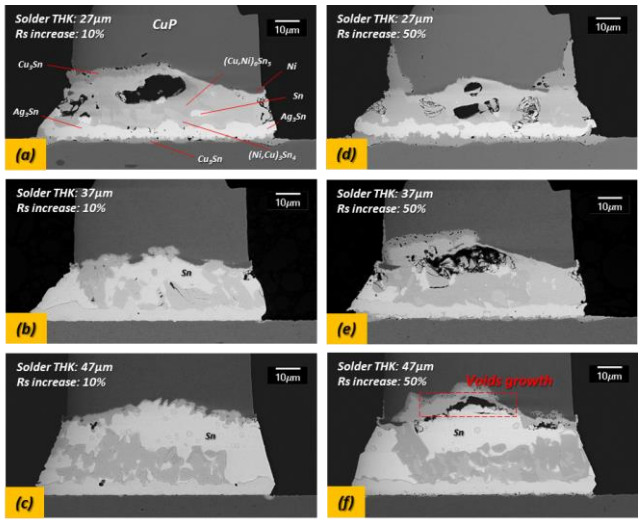

Fig. 8. Microstructure of Cu pillar interconnects after continuous stressing under downstream electron flow at 20 kA/cm^2 and 180˚C: (a) solder thickness: 27 µm, 10% Rs increase; (b) solder thickness: 37 µm, 10% Rs increase; (c) solder thickness: 47 µm, 10% Rs increase; (d) solder thickness: 27 µm, 50% Rs increase; (e) solder thickness: 37 µm, 50% Rs increase; (f) solder thickness: 47 µm, 50% Rs increase.

C. Interconnects Geometry Analysis

In general, the EM performance of interconnects with different diameters tends to be similar when subjected to the same EM test conditions, as predicted by Black's equation and theoretical principles. However, after conducting the EM test under a 20 kA/cm^2 at 180℃, the log-normal distribution slope of the TTF for Cu pillar interconnects with an 80 µm diameter was steeper than that of the 100 µm diameter interconnects, as shown in Fig. 9 (a). A better convergence of the TTF within the distribution is an idea characteristic in statistics. Notably, both early and late failures in the log-normal distribution of TTF showed that the 80 µm diameter Cu pillar interconnects performed slightly better than their 100 µm counterparts. In the previous chapter, it was noted that the 80 µm Cu pillar interconnects exhibited a conical shape, whereas the 100 µm interconnects had a bow shape. Fig. 9 (b) presents the microstructure associated with the early failure of the bow-shaped Cu pillar interconnects. A crack was observed in the lower-right area of the Cu pillar interconnect, located between the solder and the Ag_3Sn layer. Fig. 9 (c) provides a magnified view of the area highlighted in Fig. 9 (b).

An electro-thermal-mechanical coupling simulation was performed to analyze temperature and stress in order to evaluate the steady state of the EM experiment during its initial phase. Fig. 10 shows the temperature and stress contour of the Cu pillar interconnects with the same diameter, comparing bow-shaped and conical-shaped interconnects, under a current density of 20 kA/cm^2 at 180 ℃. The maximum temperature of the solder in both types of Cu pillar interconnects was nearly identical. However, the maximum stress (red points) experienced by the solder in the bow-shaped Cu pillar interconnects was 2 times greater than that in the conical-shaped interconnects. This maximum stress value corresponds closely with the microstructure depicted in Fig. 9 (b). These findings suggest that the conical-shape interconnects exhibit better EM performance due to the lower stress observed during the EM testing.

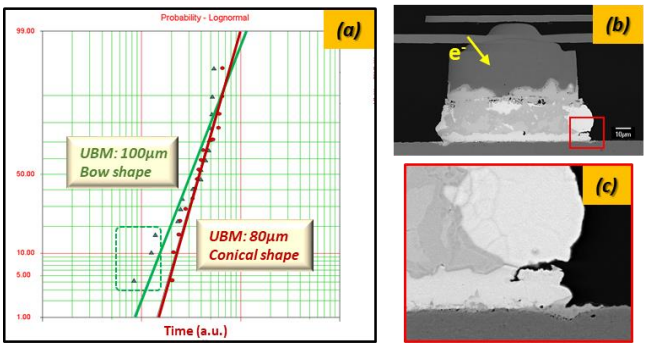

Fig. 9. (a) Log-normal distribution of TTF for the Cu pillar interconnects with bow and conical shape under a 20 kA/cm^2 at 180 ˚C; (b) Microstructure of early failure in the bow-shaped Cu pillar interconnect; (c) Magnified view of the red zone in (b).

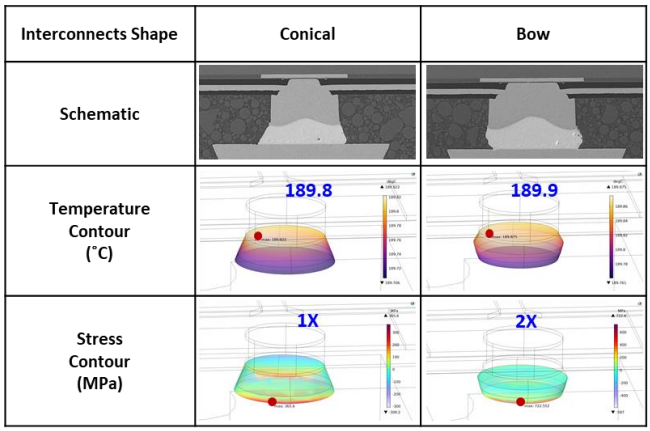

Fig. 10. FEM analysis of the Cu pillar interconnects with conical and bow shape under a 20 kA/cm^2 and 180 ˚C. Red points represent the maximum temperature and the maximum stress within the SnAg and Ag_3Sn regions.

IV. Conclusions

This study investigates the EM behavior and failure mechanisms of FCQFN Cu pillar interconnects used in high-power devices under extreme conditions. Interconnects with different diameters and varying Sn1.8Ag thicknesses were investigated to compare their EM performance. Electrical resistance responses observed during the EM tests were interpreted through detailed microstructural analyses. The solder gradually transformed into IMCs and eventually fully converted into IMCs upon a 100% resistance increase, accompanying the development of significant cracks and Kirkendall voids.

The influence of structural factors on the EM performance of Cu pillar interconnects was investigated, with particular emphasis on solder thickness and interconnect shape. Cu pillar interconnects featuring a 27 µm solder thickness exhibited the least residual solder volume after EM test, indicating a superior lifetime due to the rapid formation of a complete IMCs structure. In contrast, those with a 47 µm solder thickness experienced consecutive void growth at the interface between the solder and the Cu/Ni pillar, which adversely affected their EM behavior. Additionally, conical-shaped Cu pillar interconnects demonstrated better EM performance compared to their bow-shape counterparts—a difference attributed to variations in stress distribution as revealed by simulation results. These findings underscore the importance of optimizing both solder volume and interconnect geometry in the design of FCQFN Cu pillar interconnects, especially under extreme EM conditions.

Acknowledgment

The authors would like to acknowledge the fabrication of the FCQFN test vehicles by ASEKH product engineering and manufacturing teams and the failure analysis support by Corporation R&D lab, respectively.

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