FOWLP Automotive Grade Reliability Challenges and Solutions for Application Specific Environment

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Abstract

Fan Out Wafer Level Package (FOWLP) developed in this work passed all standard industrial/automotive grade 1 reliability qualification requirements. Development studies included Design of Experiments (DOE) variables like; die/package ratio, package designs, dielectric materials, and solder alloys. To emulate product reliability in the field, application-level temperature cycling (AL-TC) was done where the test devices were mounted on a translation board (TLB). The TLB stack up and routing were like a typical customer board design. For AL-TC different performance was observed in the DOE legs. For some DOE legs reliability was passed for automotive grade 1. For other DOE legs open and leakage fails were observed after AL-TC reliability. Modelling confirmed the failure location to be coincident with the highest die peel stress location in the package. The failure mode was Back End of Line (BEOL) delamination under the die bond pad which was related to high die peel stress. The failure root cause was attributed to stress induced by one of the package dielectric materials having a high Coefficient of Thermal Expansion (CTE) and high storage modulus at -40°C, which is the maximum stress point in the thermal shock cycle. The same failure mode was not observed in daisy chain design-based board level temperature cycling reliability.

Key words: Automotive grade product reliability, fan out wafer level package, chip package integration

I. Introduction

FOWLP have found rapid adoption in the industry over the last decade. Different FOWLP flavors are available in the industry [1-4]. The FOWLP option choice for the application depends on its I/O pitch and I/O density (I/O per mm2) requirement. Applications of FOWLP range from relatively low I/O density products like Codec, Wi-Fi, to high I/O density products like mobile phone application processors to ultra-high I/O density products for high performance computing, GPU applications. FOWLP test devices in this work are used for developing packages for microcontrollers for industrial and automotive applications. Package design considerations such as system level product application, customer printed circuit board routing and cost competitiveness, can result in a product package design reliability issue. In addition to reliability on component level (using stand-alone products) and reliability on board level (using daisy chains), the impact of the application environment on component reliability should also be considered (test products mounted in the application environment) [5]. For this purpose the test products were mounted on a TLB, which was similar to the end customer field application design. The selected TLB was meant to address the failure modes induced at the interconnection between the PCB and the test device, like BEOL cracks influenced by test device design, the BEOL structure and rerouting. Failures in the interconnection between the TLB and the test device were prevented as much as possible by optimizing the PCB design as their occurrence was not the intention of this test. Post reliability stress, devices were tested at room, hot, cold temperatures for opens, shorts, leakage fails and parametric shifts. Thermomechanical Analysis and Dynamic mechanical analysis were used to characterize the TLB package material properties. For comparison, board level reliability (BLR) using daisy chain design was also done.

II. Experimental Section

FOWLPs were fabricated using the die first, die face down process. Different DOE variables were applied during package development. Die/package ratio, die thickness were varied to optimize in process FOWLP wafer warpage [6]. Different solder alloy materials were evaluated for board level reliability assessment. In our earlier work it was

reported that the usage of stiff solder alloy significantly improved the board level reliability performance [7]. However, using a stiffer solder alloy increases the stress on the package and die interconnect layers. This stress increase can induce package and die interconnect related failures [8, 10]. The focus of the current report is application-level temperature cycling reliability, where a functional test device was assembled on a TLB and subjected to air-to-air temperature shock cycling of -40°C to +125°C. Two FOWLP package designs were evaluated in the current study. Figure 1 shows top view schematics of the designs 1 and 2. Both designs have same package size = 7mm x7mm, solder ball pitch = 0.4mm and solder ball map. Design 1 and design 2 have die sizes of 4.5mm x4.5mm and 4.2mm x 4.2mm respectively. Due to the slightly smaller size in design 2, the solder ball sits on top of die edge. Fig. 2 is a cross section of design 1, where the solder ball is horizontally offset from the silicon/epoxy mold compound (EMC) interface. Fig. 3 is a cross section of design 2, where the solder ball is horizontally not offset from the silicon/EMC interface. The packages were surface mount on an 8-layer

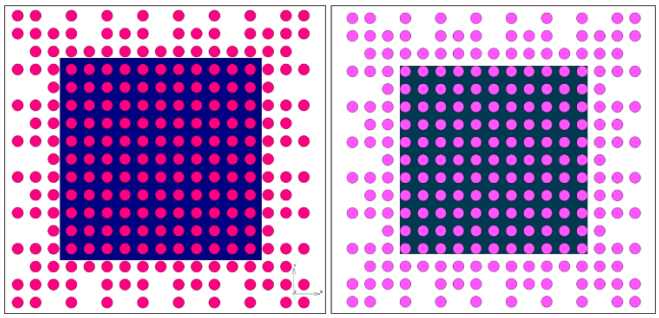

Fig. 1: FOWLP designs schematic. Design 1 (left) and design 2 (right).

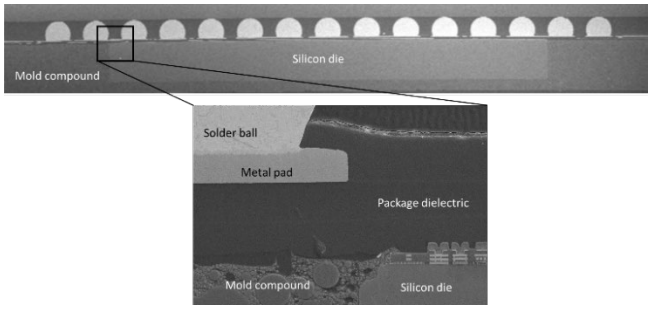

Fig. 2. FOWLP cross section for design 1 (top). Magnified view of solder ball that is horizontally offset from the silicon/EMC interface (bottom).

TLB (see Fig. 4). Fig. 5 is cross section schematic of the TLB. Before assembly on the TLB the packages undergo MSL1 preconditioning (85°C/85%RH/168h + 2X reflow). The package/TLB were subjected to temperature shock cycling reliability (-40°C/+125°C, 4 shock cycles/hour).

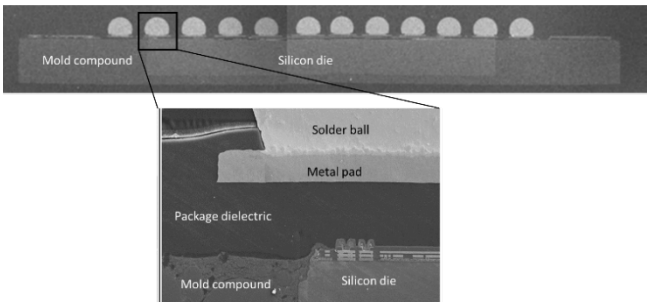

Fig. 3. FOWLP cross section for design 2 (top). Magnified view of solder ball that is horizontally not offset from silicon/EMC interface (bottom).

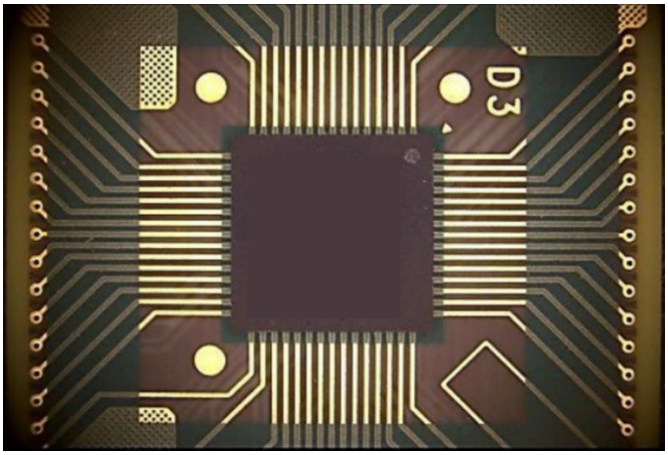

Fig. 4. Package component assembled on TLB

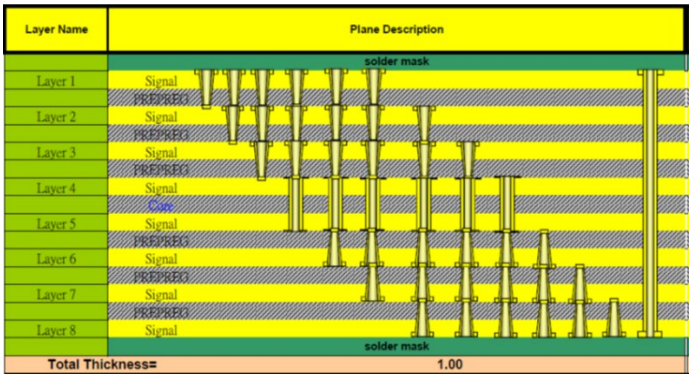

Fig. 5. Cross section schematic of TLB.

III. RESULTS AND DISCUSSION

A. Material Characterization

To assess the thermomechanical properties of the materials under concern, Thermomechanical analysis (TMA) and Dynamic Mechanical Analysis (DMA) have been conducted:

- TMA measures linear changes in the dimensions of a sample as a function of time, temperature, and force in a controlled atmosphere. This analysis is used to measure

the thermal expansion (CTE) and glass transition temperature (Tg).

- DMA measures the modulus (stiffness) and damping (energy dissipation) properties of materials as the materials are deformed under a cyclic stress. This analysis can be used to assess the viscoelastic properties of a polymeric material as a function of frequency (multi-frequency test). The material behavior can also be well approximated by a linear elastic model (single frequency test). This approximation has been used to describe the two dielectric materials under analysis. Material data was provided by the suppliers.

The data showed in Fig.6 are resulting from TMA and DMA (single frequency) tests, run from -50°C to 200°C. The temperature range is aligned with the temperatures experienced by the materials during its service life. Two dielectric materials, dielectric 1 and dielectric 2 were characterized. Dielectric 2 has a lower coefficient of thermal expansion (CTE) than dielectric 1. A lower dielectric CTE will lead to a lower CTE mismatch with the silicon (CTE = 2.5 ppm/°C), resulting in lower fatigue stress during the thermal shock reliability. Dielectric 2 also has a lower storage modulus at lower temperatures compared to dielectric 1.

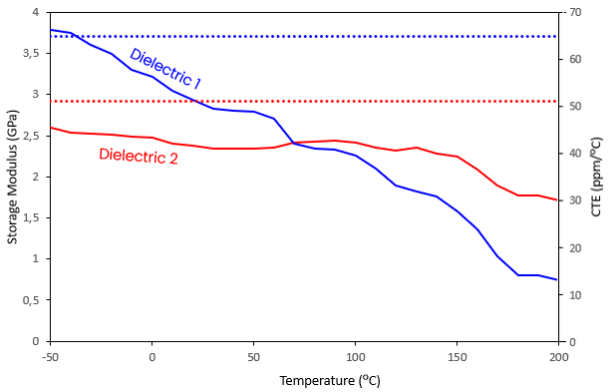

Fig. 6. Storage modulus vs temperature (full line) and CTE vs temperature (dotted line) for FOWLP dielectrics 1 (blue) and 2 (red)

B. Modelling

The next phase of our analysis involves conducting detailed thermo-mechanical simulations using Finite Element Analysis (FEA) for the FOWLP. These simulations aim to accurately capture the stress distribution within the package by incorporating precise details of the Redistribution Layer (RDL) layout and stack-up. Starting from the product's original design file, all geometric details of the RDL structure are resolved to ensure sufficient detail in the simulation model (see Fig. 7). A continuous two-dimensional (2D) mesh is generated for the geometry, with each RDL trace represented by at least two elements across its width. The final three-dimensional (3D) mesh is created using an extrusion technique, resulting in a structure predominantly composed of linear hexahedrons. These hexahedrons are defined with at least two elements across the thickness of each layer, ensuring that the RDL stack achieves a minimum thickness of eight elements. Linear hexahedrons are particularly advantageous due to their computational efficiency, requiring fewer resources thus enabling faster processing compared to higher-order elements. They provide high accuracy when aligned with regular geometries, are compatible with extrusion techniques, and effectively model thin layers while offering better numerical stability and reduced noise. These benefits make them ideal for layered structures such as circuit boards and/or microelectronic packages. However creating high-quality hexagonal meshes

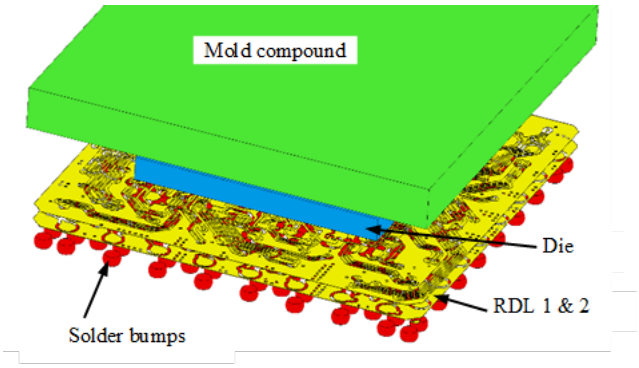

Fig. 7. Exploded view of the simulation model of the FOWLP showing the over-molded die, the double RDL structure, and the solder bumps. The passivation material that embeds the RDL, as well as the PCB, are omitted in the plot for enhanced visibility.

for irregular geometries can present challenges. The material models used in the simulations are temperature-dependent and account for plasticity or viscoelasticity where applicable. Incorporating viscoelastic materials into the model allows for realistic representation of time-dependent behavior, such as creep, stress relaxation, and dynamic loading. These materials enable simulations to analyze the effects of thermal and environmental factors, providing insights into long-term failure modes such as fatigue and degradation. Additionally, viscoelastic models support transient simulations that optimize designs for enhanced reliability and performance. This comprehensive approach ensures accurate predictions of material behavior under real-world conditions. The material properties used in the simulation are summarized in Table 1. The simulation model assumes a stress-free state at the solder solidification temperature of approximately 220 °C. The temperature is then reduced in equal steps of about 15 °C until it reaches -40 °C. At this lowest temperature, the peel stress at the die surfaces is plotted (see Fig. 8) for design 2, as it corresponds to the highest stress levels. Analysis

Table 1. Summary of properties used in the simulation model. The mold compound glass transition temperature is 160 °C. The properties of the dielectrics are discussed in the previous section.

	E (GPa)	CTE (ppm/°C)	Remark
Solder	50	17.2	Plastic model
PCB	17	19.6	Temperature dependent
Silicon	169	2.5	-
Copper	105	17.7	Plastic model
Mold compound	29	7.5 - 30	Visco-elastic

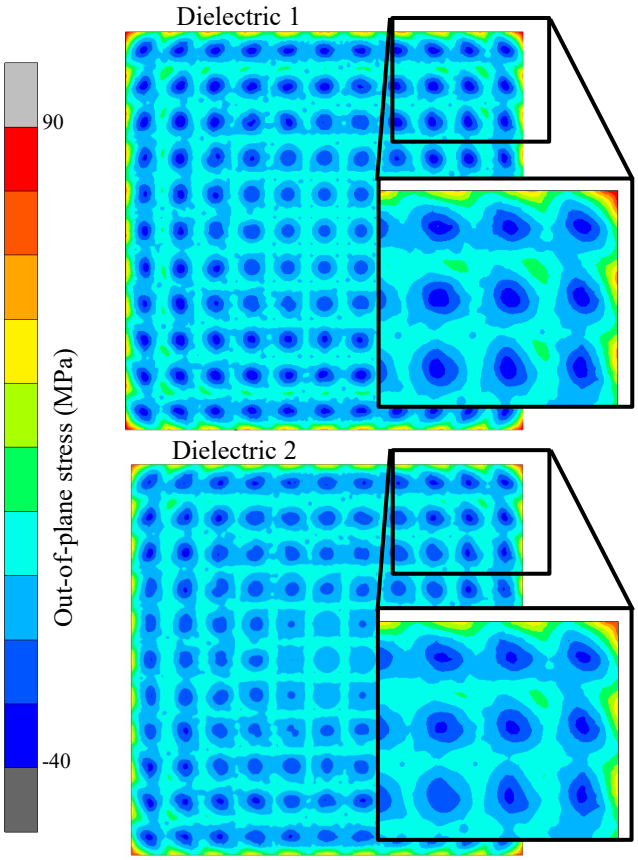

Fig. 8. Peel stress at die-to-RDL interface at T=-40 °C for dielectric 1 and 2. Insets show magnification at the corners.

reveals that the stress beneath the bumps is compressive, while tensile forces act on the die surface periphery. The highest stress levels are observed at the die edge, coinciding with regions prone to stress uplift in general. This stress distribution aligns with the observed failure mode, characterized by delamination of the BEOL layers (discussed in detail in the next reliability stress section). Comparative analysis shows that dielectric 2 generates slightly lower stress levels than dielectric 1, suggesting improved performance under these conditions. For design 1, the maximum die peel stress is 45% lower than design 2.

By employing the detailed simulations presented above, a deeper understanding of stress behavior within the FOWLP is achieved, enabling the optimization of designs and materials to enhance the reliability and overall performance of these advanced electronic packages.

A. Reliability Stress

Both dielectric 1 and dielectric 2 were evaluated for AL-TC reliability. Design 1 passed reliability up to 1500c, with zero fails, with both the dielectrics. For design 2, fails were observed with dielectric 1. First failures were observed at 600c. Failure rate increased modestly from 2% at 600c to 6% at 1500c. Electrical curve trace analysis confirmed the failure to be located inside the die. Physical failure analysis starting from solder ball/TLB cross section, followed by step-by-step delayering of the package layers showed no physical damage to the package structure. FIB cross section under the die pad showed BEOL crack (see Fig. 9). Detailed analysis showed the crack propagation direction to be from inside active die area towards the die seal ring. Failed die pads were located along all the die edges, which is indicative of an intrinsic issue in the die and not an assembly process induced failure. This failure mode is consistent with the modelling prediction of highest die peel stress at the die edge region (see fig. 8). However, when dielectric 2 is used, the peel stress is reduced in comparison to dielectric 1 (see fig. 8). The stress reduction is because at -40°C dielectric 2 has a lower CTE and storage modulus in comparison to dielectric 1. As a result, no failures are observed for packages with dielectric 2 till AL-TC 1500 cycles. For design 1, no AL-TC failures were reported till 1500 cycles, with both dielectric 1 and dielectric 2. This is because for design 1, the solder ball is horizontally offset from silicon die/EMC interface, which leads to a 45% reduction in die peel stress in comparison to design 2. For both FOWLP designs the silicon dies have peripheral I/O layout, where the die I/Os are along the die periphery. For design 2 the solder ball is horizontally not offset from the die edge and the solder ball is positioned on top of the die I/O aluminum pad. FOWLP has the following package layers: dielectric 1/metal 1/dielectric 2/metal 2/dielectric 3. The solder ball is separated from the die I/O pads by three dielectric layers and yet the stress transferred from the solder ball to the die during AL-TC thermal shock cycling has a strong dependence on the horizontal offset of the solder ball. This is indicative of careful consideration that is required during the design and material selection of FOWLP test products. Fig. 10 shows BL-TC reliability comparison for dielectric 1 and dielectric 2. Both dielectrics show statistically similar performance and pass qualification requirement. Fig. 11 shows cross sections from early and late reliability cycle failures. The failure is bulk solder failure for

both early and late reliability cycle samples. Daisy chain units based BLR do not show the failure mode seen in AL-

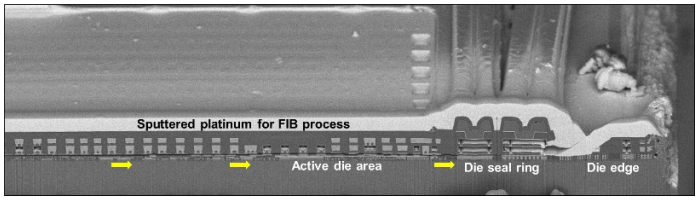

Fig. 9. Focused Ion Beam (FIB) cross section image from underneath an open failing die pad. Yellow arrows show the BEOL crack propagation direction from the active die area towards die seal ring, which caused the open failure. No crack is visible at die edge.

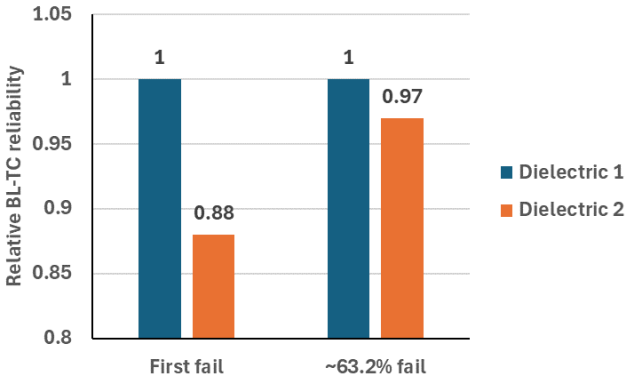

Fig. 10: Relative BL-TC reliability with the two dielectrics

TC reliability. Thus, functional product reliability in an application environment, induces unique failure mode which was the primary objective of this work. Fig. 12 shows cross section of a FOWLP on a TLB after AL-TC 1500c, which passed all functional tests. Cross sections revealed no physical damage or degradation in the package. Fig. 13 is a die surface image from sample that passed AL-TC 1500c. All package layers have been removed. Probe mark and dielectric 1 via impression on die pad, aluminum, copper metal grain structure are visible. No die passivation damage can be seen. The post stress construction analysis on the sample highlight the robustness of the package even after 1500c, AL-TC stress testing. Table 2 summarizes the packages AL-TC, BL-TC reliability results.

IV. CONCLUSION

FOWLP reliability for industrial/automotive grade 1 is passed on test products on TLB that mimics the end customer field application design. Successful chip package integration across all the package interconnect levels (TLB/solder ball, solder ball/package, package/die) is demonstrated by employing a comprehensive material selection, modelling, characterization, and reliability assessment approach. It is shown that test product reliability in an application specific

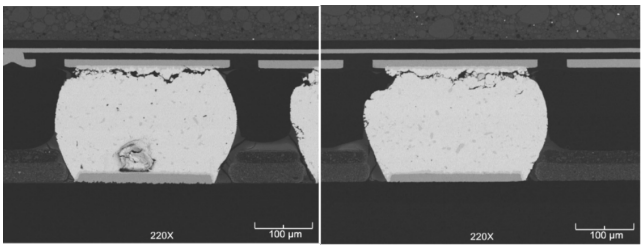

Fig. 11: Cross sections from early and late failure solder joints from BL-TC reliability test

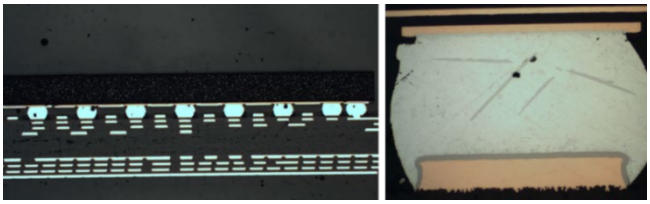

Fig. 12. FOWLP on 8-layer translation board (TLB) after AL-TC 1500c, which passed electrical tests. No physical damage can be seen for the package.

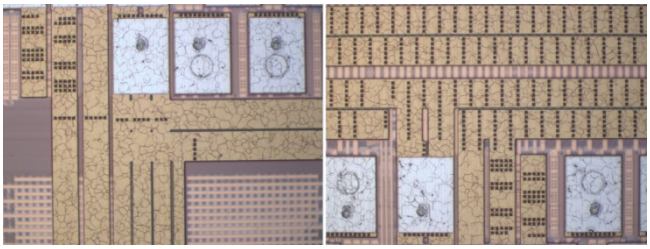

Fig. 13: Post 1500c AL-TC die surface after all package layers have been removed. No die passivation damage is visible.

Table 2. AL-TC, BL-TC reliability summary for auto grade 1 qualification

Package	Dielectric	AL-TC	BL-TC
Design 1	Dielectric 1	Pass	Pass
Design 1	Dielectric 2	Pass	Pass
Design 2	Dielectric 1	Fail	Pass
Design 2	Dielectric 2	Pass	Pass

environment can induce failure modes that are generally not observable with standard component level (using stand-alone products) and board level reliability (using daisy chains) tests.

References

[1] M. Brunnbauer et al, “Embedded wafer-level ball grid array (eWLB)”, Proc of 8th Electronic Packaging Tech. Conf., 10-12, Dec 2006, Singapore, pp 1-5.

[2] R. Huemoeller, “Silicon wafer integrated fan out technology”, Chip Scale Review, Mar/Apr issue 2015.

[3] C-F. Tseng et al, “InFO (wafer-level integrated fan out) technology”, IEEE 66th Elect. Comp. and Tech. Conf. (ECTC), 31 May – 3 June 2016, Las Vegas, NV, USA, pp. 1-6.

[4] Y.C Hu et al, “CoWoS architecture evolution for next generation HPC on 2.5D system in package”, IEEE 73rd Elect. Comp. and Tech. Conf. (ECTC), 30 May – 2 June 2023, Orlando, FL, USA, pp. 1022-1026.

[5] Rocou et al, “Effect of PCB stack-up on Temperature Cycling Reliability of WLCSP”, IEEE 7th Electronic System-Integration Technology Conference (ESTC), 18-21 September 2018, Dresden, Germany

[6] G. Sharma et al, “Development of Wafer Level Package Platform for High reliability Crossover MCUs”, Proc. 56th International Symposium on Microelectronics, October 2-5, 2023, San Deigo, CA, USA

[7] G. Sharma et al, “Advanced fan out wafer level package development for small form factor and high performance microcontroller applications”, Proc International Wafer Level Packaging Conference, 22-24 October, 2019, San Jose, CA, USA

[8] C.K. Yu et al, “A unique failure mechanism induced by chip to board interaction on fan-out wafer level package”, IEEE International eliability Physics Symposium (IRPS), 2-6 Apr 2017, Monterey, CA, USA

[9] P.H. Tsao et al, “Board Level Reliability Enhancement of WLCSP with Large Chip Size”, IEEE 68th Elect. Comp. and Tech. Conf. (ECTC), May 29 – June 1, 2018, San Diego, CA, USA, pp. 1200-1205.

[10] W. Lin et al, “SACQ Solder Board Level Reliability Evaluation and Life Prediction Model for Wafer Level Packages’, IEEE 67th Elect. Comp. and Tech. Conf. (ECTC), 30 May – June 2, 2017, Lake Buena Vista, FL, USA, pp 1058-1064.