Simplification of Via-first TSV and Backside Interconnect Process for Large-Scale Superconducting Quantum Annealing Circuits

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Abstract

We proposed a simplified through-silicon via (TSV) and backside interconnect process to suppress cavity resonance in superconducting quantum annealing circuits. The conventional process consisted of 13 steps, but in the new process, it was reduced to 11 steps by forming TSVs first, then creating the backside interconnect, and finally thinning the wafer to expose the TSVs. The new process comprised the following steps: (a) deep silicon etching using the Bosch process, (b) hole cleaning to remove the photoresist and fluoropolymer residues, (c) CF_4 plasma treatment to reduce sidewall scallop, (d) barrier/seed-layer deposition, (e) copper electroplating for TSV filling, (f) backside chemical mechanical polishing (CMP), (g) formation of the superconducting backside interconnect (Ti-Nb-Ti layer), (h) deposition of a backside protection layer, (i) direct Si/Cu grinding, (j) frontside CMP, and (k) fabrication of the quantum annealing circuit. Using this process, we fabricated TSVs (diameter at backside, 60 μm; depth, 395 μm) with superconducting backside interconnects in a 100-mm high-resistivity silicon wafer. Furthermore, we evaluated the effect of TSVs on cavity resonance through high-frequency measurements of samples with and without TSVs. The results demonstrate that the TSVs and backside interconnect of new process effectively suppress cavity resonance.

Key words

superconducting quantum annealing circuit, via-first, through-silicon via, TSV, cavity resonance

I. Introduction

A combinatorial optimization problem is the act of trying to find out the best solution from a finite set of possible combinations under various constraints. Quantum annealing is an effective approach for solving such problems [1,2]. In quantum annealing, the combinatorial optimization problem is mapped to an Ising model, and its cost function is minimized by introducing quantum fluctuations.

To achieve practical quantum annealing, a high-quality, large-scale quantum annealing machine is essential. NEC Corporation and AIST are collaboratively developing large-scale quantum annealing machines based on superconducting parametrons [3,4]. Figure 1 shows a schematic of the superconducting quantum annealing machine and the equivalent circuit of a superconducting parametron. This system offers strong noise resistance, long coherence time, and high scalability due to the superconducting elements. However, as the quantum annealing circuit chip increases in size and operates at higher frequencies (10–20 GHz), cavity resonance can occur within the silicon chip, potentially leading to circuit malfunctions (Fig. 2). To address this problem, we previously developed a via-first through-silicon via (TSV) and backside interconnect process to suppress cavity resonance (Fig. 3) [5]. Although effective, the process involves 13 fabrication steps, making it complex.

In the present study, we developed a simplified TSV and backside interconnect process. This process involves forming TSVs first, followed by forming a backside interconnect and thinning the wafer to expose the TSVs. This sequence eliminates the need for a surface-protection layer. The proposed method comprises 11 fabrication steps. Using this process, we fabricated TSVs (diameter at backside, 60 μm; depth, 395 μm) with superconducting backside interconnects in a 100-mm high-resistivity silicon wafer. We

evaluated the effectiveness of the TSVs in suppressing cavity resonance through high-frequency measurements conducted on samples with and without TSVs. The results demonstrate that cavity resonance can be suppressed by the TSVs and backside interconnects formed using this process.

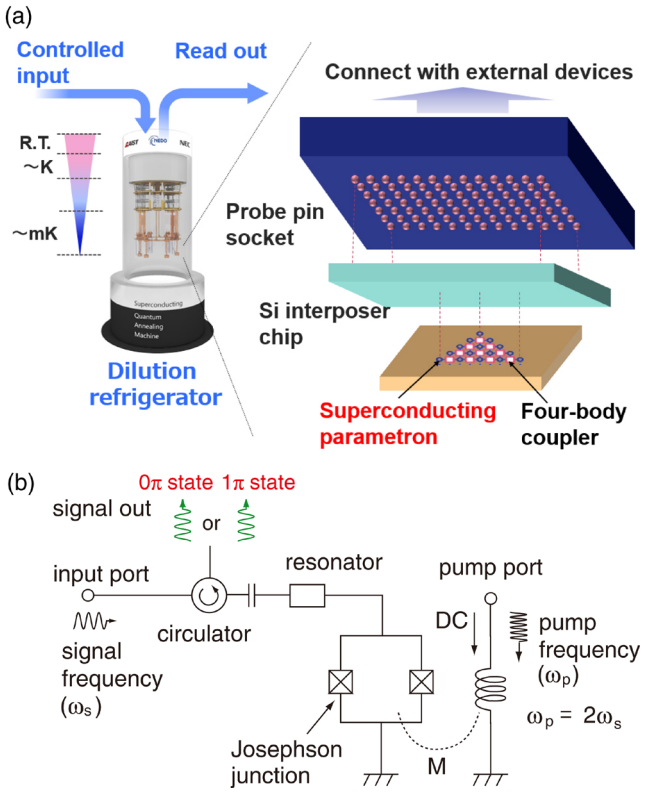

Figure 1: (a) Schematic of the large-scale superconducting quantum annealing machine. In this system, a large-scale superconducting parametron chip is stacked on a silicon interposer and probe pin socket, which is then placed into a dilution refrigerator. (b) Equivalent circuit of a superconducting parametron.

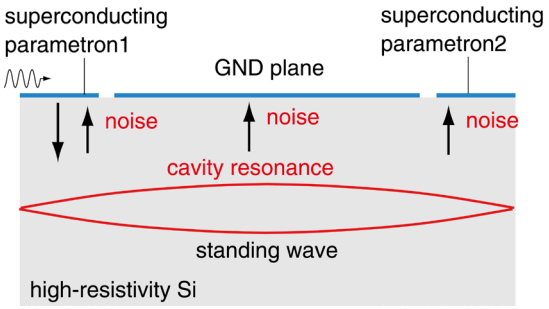

Figure 2: Diagram of cavity resonance. When the chip size is large and the input signal frequency is high, the input signal generates a standing wave inside the Si substrate, which generates noise.

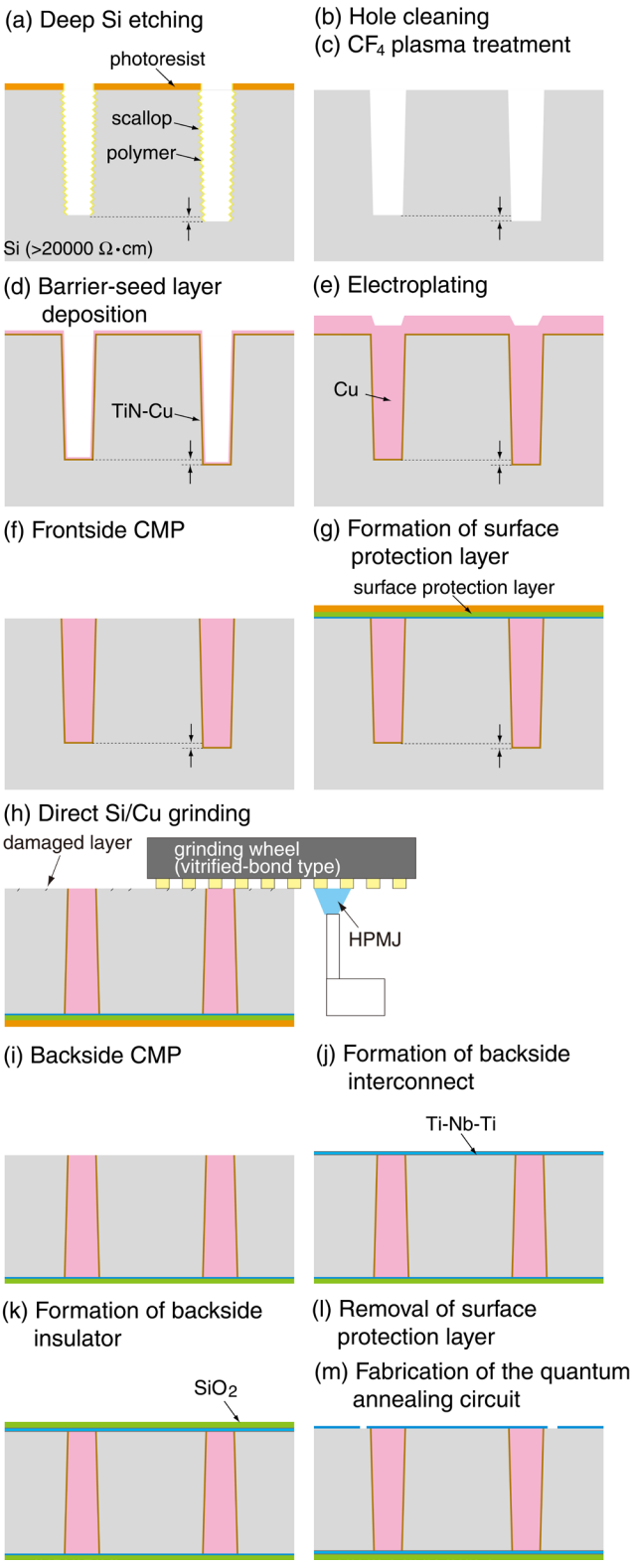

Figure 3: Flow of via-first TSV and backside interconnect process to suppress cavity resonance. This process consists of 13 steps.

II. Simplified TSV and backside interconnect process to suppress the cavity resonance

Figure 4 outlines the flow of the simplified TSV and backside interconnect process to suppress the cavity resonance of superconducting quantum annealing circuits. The wafer was a high-resistivity Si wafer (diameter, 100 mm; resistivity, >20,000 Ω·cm). The need for a surface-protection layer was eliminated by forming TSVs first, then creating the backside interconnect, and finally thinning the wafer to expose the TSVs. The proposed process comprises 11 fabrication steps. First, photolithography was performed by using a positive-tone photoresist PMER P-CY1000 (Tokyo Ohka Kogyo Co., Ltd.), and deep Si etching was performed using the Bosch process with an etching system (DPX-Predeus, SPP Technologies Co., Ltd.). The etching time per cycle was reduced to decrease the size of the scallops. In addition, to suppress the decrease in etching speed and mask selectivity at the bottom of the hole, we ramped the parameters (etching time, deposition time, and coil power). The resulting vias had a diameter of 60 µm and a depth of 400–410 µm. The holes were cleaned with a sulfuric acid-hydrogen peroxide mixture, megasonic cleaning with ammonia–hydrogen peroxide mixture, dilute hydrogen fluoride, and megasonic cleaning with deionized water. Sidewall scallops were subsequently reduced by CF_4 plasma treatment. TiN and Cu films were then deposited. For conformal deposition, the TiN film was deposited at 200 °C by atomic layer deposition using $Ti[N(CH_3)_2]_4$, yielding a film thickness of approximately 100 nm. The Cu film was deposited by long-throw sputtering with a surface thickness of approximately 4000 nm. Copper electroplating was performed using a face-up electroplating system (4C204, Tosetz Inc.) with an additive (INTERLINK 9200, DuPont); the leveler, suppressor, and accelerator were maintained at 3.5, 6, and 6.5 mL/L, respectively. Backside chemical mechanical polishing (CMP) was used to remove Cu and TiN. A Ti-Nb-Ti layer was then deposited as the backside interconnect, with layer thicknesses of 30, 200, and 30 nm, respectively. A SiO_2 layer was deposited as a backside insulator via chemical vapor deposition using tetraethyl orthosilicate and O_2 gas at 100 °C. Direct Si/Cu grinding was performed using a fully automatic wafer grinder (GNX200BH, Okamoto Machine Tools Co., Ltd.) with a vitrified bond grinding wheel, which was cleaned during grinding using a high-pressure microjet. The in-situ cleaning of the grinding wheel and the inelastic porous structure of the grinding wheel suppressed Cu burning and smearing. Frontside CMP was performed to remove the damaged layer generated by direct Si/Cu grinding. The final TSV depth after frontside CMP was approximately 395 µm. After completing the TSV and backside interconnect steps, the quantum annealing circuit was fabricated.

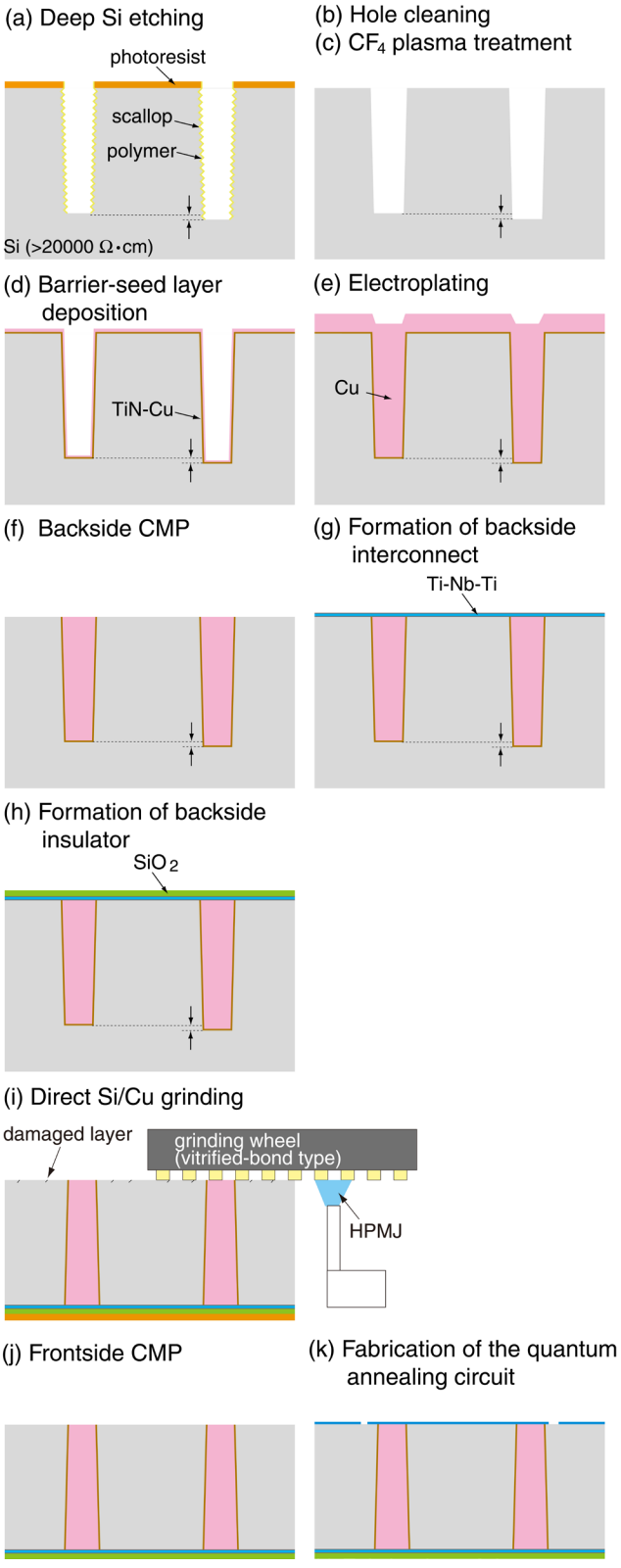

Figure 4: Flow of simplified TSV and backside interconnect process to suppress cavity resonance. This process consists of 11 steps.

Figure 5 shows a cross-sectional SEM image and optical micrographs of the wafer fabricated using the new process described in Fig. 4. TSVs with a backside diameter of 60 µm and a depth of 395 µm were formed, and a Ti-Nb-Ti backside interconnect was formed on the back surface.

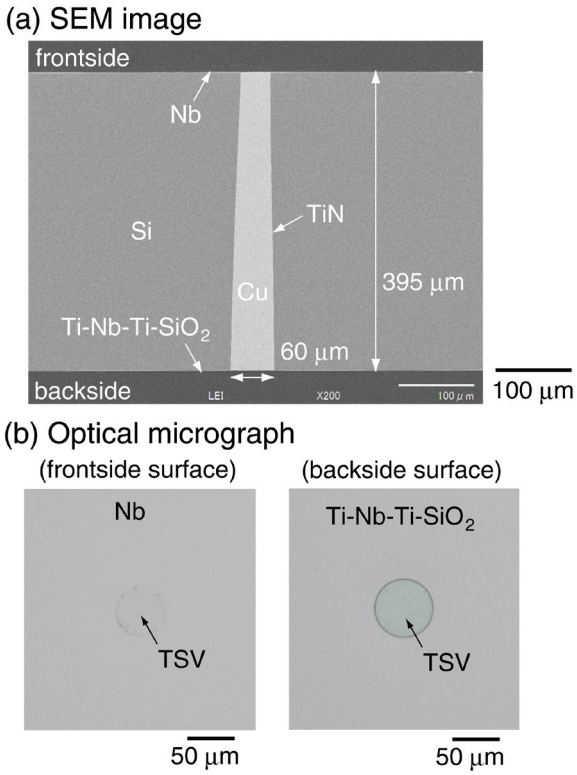

Figure 5: (a) cross-sectional SEM image and (b) optical micrographs of the wafer fabricated using the new process.

III. Effect of TSV and backside interconnect on cavity resonance

To evaluate the effect of TSVs and backside interconnects formed by new process (Fig. 4), we prepared and measured through-pattern chips with and without TSVs, using TSV pitches of 350, 700, and 1400 µm (Fig. 6). Each chip had dimensions of 10 × 10 × 0.395 mm. The frequency dependence of the S-parameters (S11 and S21) for each sample was measured at 4 K using a network analyzer.

Figure 7 shows the S11 and S21 measurement results. In the absence of TSVs, cavity resonance was observed, with large resonances at 14.4 and 18.6 GHz, which were close to the operating frequencies of the quantum annealing circuit (10 and 20 GHz). These resonances corresponded to elevated S11 values and could affect the operation of quantum annealing circuits substantially. In contrast, no cavity resonance was detected in samples containing TSVs. This result was similar to that of the sample with TSVs and backside interconnect formed by the conventional process shown in Fig. 3 [5]. These results demonstrate that cavity resonance can be suppressed by TSVs and backside interconnect formed using the new process, as well as TSVs and backside interconnect formed using the conventional process.

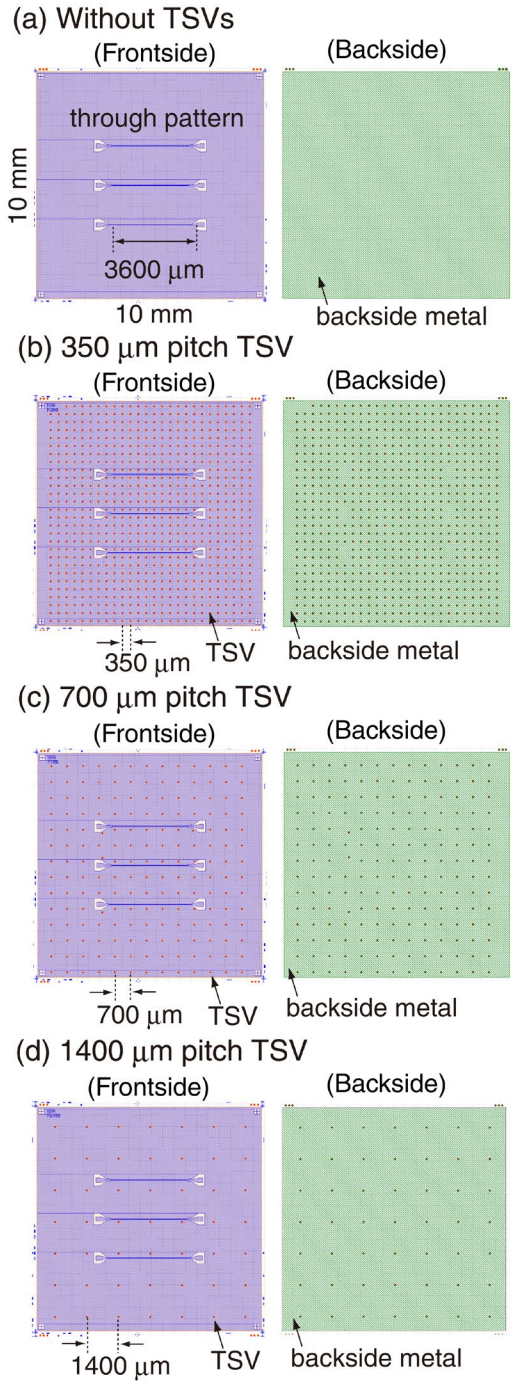

Figure 6: Illustration of some through-pattern chips. Through-pattern chips without TSVs and with 350-, 700-, and 1400-µm-pitch TSVs were prepared.

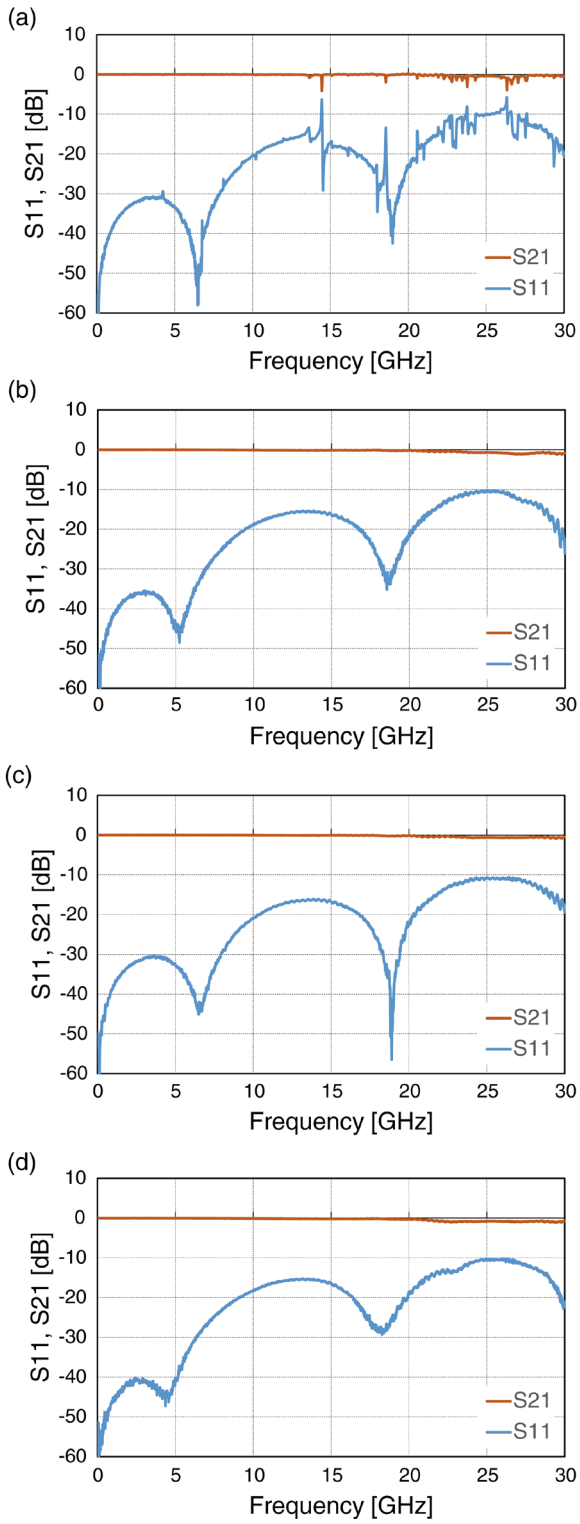

Figure 7: Measurement results for S11 and S21 for samples (a) without TSVs and with (b) 350-µm-pitch TSVs, (c) 700-µm-pitch TSVs, and (d) 1400-µm-pitch TSVs. TSVs and backside interconnect were fabricated by the new process shown in Fig. 4.

IV. Conclusion

We developed a simplified TSV and backside interconnect process. The conventional process consisted of 13 steps, but in the new process, it was reduced to 11 steps by forming TSVs first, then creating the backside interconnect, and finally thinning the wafer to expose the TSVs. The new process comprises the following steps: (a) deep Si etching using the Bosch process, (b) hole cleaning to remove the photoresist and fluoropolymer, (c) CF_4 plasma treatment to reduce sidewall scalloping, (d) barrier/seed-layer deposition, (e) electroplating for Cu filling, (f) backside CMP, (g) formation of a superconducting backside interconnect (Ti-Nb-Ti layer), (h) formation of a backside protection layer, (i) direct Si/Cu grinding, (j) frontside CMP, and (k) fabrication of the quantum annealing circuit.

Using this process, we fabricated TSVs (diameter at backside, 60 µm; depth, 395 µm) with superconducting backside interconnects in a 100-mm high-resistivity Si wafer. We also investigated the suppression effect of TSVs on cavity resonance using high-frequency measurements of samples with and without TSVs. The results demonstrated that cavity resonance was suppressed by the TSV and backside interconnect of new process.

This new process contributes to the development of large-scale superconducting quantum annealing circuits with 100 or more qubits.

Acknowledgment

This study was (partly) based on the results obtained from project JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO), Japan. The authors thank Mr. Mitsui and Mr. Nakai of Okamoto Machine Tools Co., Ltd. for their technical support.

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