Novel Optical Bumps using Graded Index Couplers for Flip-Chip Photonic Packaging

Drew Weninger[1,*], Christian Duessel[2], Samuel Serna[3], Lionel Kimerling[2], and Anuradha Agarwal[1]
[1]Materials Research Laboratory, Massachusetts Institute of Technology
77 Massachusetts Ave, Cambridge, MA 02139 USA
[2]Department of Materials Science and Engineering, Massachusetts Institute of Technology
77 Massachusetts Ave, Cambridge, MA 02139 USA
[3]Department of Physics, Photonics, and Optical Engineering, Bridgewater State University
131 Summer St, Bridgewater, MA 02324 USA
*drewski@mit.edu

Abstract

A graded index optical coupler was designed to connect silicon oxynitride photonic waveguides on separate chips, or between a chip and an interposer, demonstrating a simulated coupling loss of 0.37 dB and 0.42 dB at 1550 nm and 1310 nm wavelength, respectively, for an 11 μm vertical chip-to-chip gap. A robust 1-dB lateral and vertical alignment tolerance of ± 2.66 μm and 2.45 μm, respectively, at 1550 nm wavelength were also demonstrated, allowing for high speed, automated pick-and-place die bonders to be used for passive assembly of photonic chips. In addition, the same coupling design was simultaneously used for fiber-to-chip coupling, showing the potential of the coupler to act as a universal photonic packaging interface. When simulating coupling to a standard flat-faceted SMF-28 fiber at 1550 nm and 1310 nm wavelength,coupling losses of 0.62 dB and 0.46 dB, respectively, were observed. The fiber-to-chip coupling simulations also demonstrated wide 1-dB alignment tolerances of ± 2.88 μm laterally and ± 2.58 μm vertically at 1550 nm wavelength. The device was also ultra-broadband, demonstrating a simulated 1-dB wavelength tolerance of over 1400 nm for both fiber-to-chip and flip-chip optical coupling, showing low loss across nearly the entire near infrared spectrum. Alongside simulations, CMOS foundry compatible fabrication processes were established to deposit, pattern, and etch greater than 10 μm thick silicon oxynitride graded index lenses on silicon and glass substrates. The simulation and fabrication results, combined with a relatively compact footprint allowing for pitches down to 20 μm, may enable Petabyte per second optical I/O - a critical need for data center co-packaged optics based Ethernet switch systems within the next decade.

Key words

silicon photonics, photonic packaging, edge coupling, chip-to-chip coupling, flip-chip assembly, co-packaged optics

I. Introduction

Silicon photonic integrated circuits (Si-PICs) have seen significant advancement over the past 40 years, highlighted by their rise to dominance as data center interconnects [1]. However, the scaling of optical input/output (I/O) remains a significant manufacturing challenge, underscored photonic packaging, assembly, and testing occupying 70-80% of the total cost of Si-PIC manufacturing [2]. One of the primary barriers to optical I/O scaling is the use of active alignment and bonding of V-groove based single mode fiber (SMF) arrays to Si-PICs using UV-curable epoxies, increasing cost and limiting throughput. Not only are current optical packaging methods costly, but they are severely limited in terms of pitch - SMF arrays operating near datacom (1310 nm) or telecom (1550 nm) wavelengths have minimum pitches of 127 μm, meaning a maximum density of only 8 fibers/mm is possible.

The aforementioned assembly challenge is especially pertinent to co-packaged optics (CPO) systems. These systems

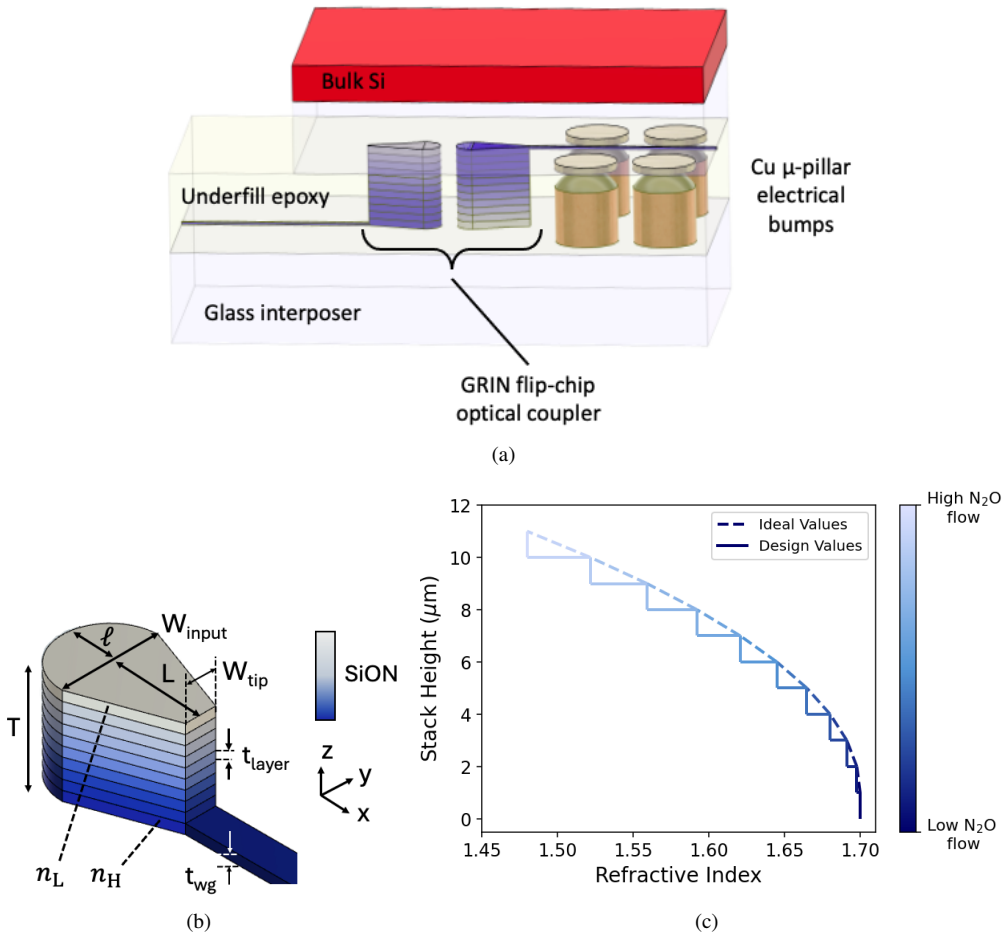


Figure 1: In (a) a 3D schematic representing how a pair of GRIN lenses, one on the chip and one on the interposer (or another chip), can be used for inter-chip optical coupling alongside Cu μ-pillar electrical bumps. In (b) a 3D view of a single GRIN coupler showing all the relevant design parameters. In (c) the parabolic refractive index profile of the SiON layers is shown along the stack height of the GRIN coupler.

include the state-of-the-art Ethernet switch packages used in data centers, where PICs and electronic application specific integrated circuits (ASICs) are packaged on the same substrate. Historically, these switch packages have met bandwidth demand by doubling total bandwidth capacity every two years, currently reaching bandwidth capacities of 102.4 Tbps per package [3]. Going forward, these CPO systems may require $> 10^3$ SMFs to scale to Petabyte per second (Pbps) package I/O data rates by 2035 as required by current CPO trends [4]. Thus, integrated silicon photonic packaging and assembly represents a critical bottleneck in the continued exponential increase of performance in cloud-based digital infrastructure.

In light of these challenges, we have developed [5] and patented [6] an optical coupling solution based on integrated graded index (GRIN) lenses which can be used for flip-chip (i.e. chip-to-chip) connections, analogous to the electrical solder joint. A schematic showing how this coupler can be incorporated into a Si-PIC back-end-of-line (BEOL) is shown in Fig. 1(a). Through the flip-chip design with a tight lateral pitch (potentially < 20 μm), this strategy enables optical fan-out and passive assembly using automated pick-and-place technology. Moreover, this optical coupling solution can be simultaneously used for fiber-to-chip coupling and packaged alongside electrical BEOL interconnects. First, this study focused on the design of the GRIN coupler, with simulations evaluating the fiber-to-chip and chip-to-chip coupling loss, 1-dB and 3-dB misalignment tolerances, and 1-dB wavelength tolerance. Following simulation, complementary-metal-oxide-semiconductor (CMOS) foundry compatible processes including deposition, patterning, and etching were optimized to successfully fabricate integrated silicon oxynitride (SiON) GRIN lenses > 10 μm thick on both glass and silicon substrates.

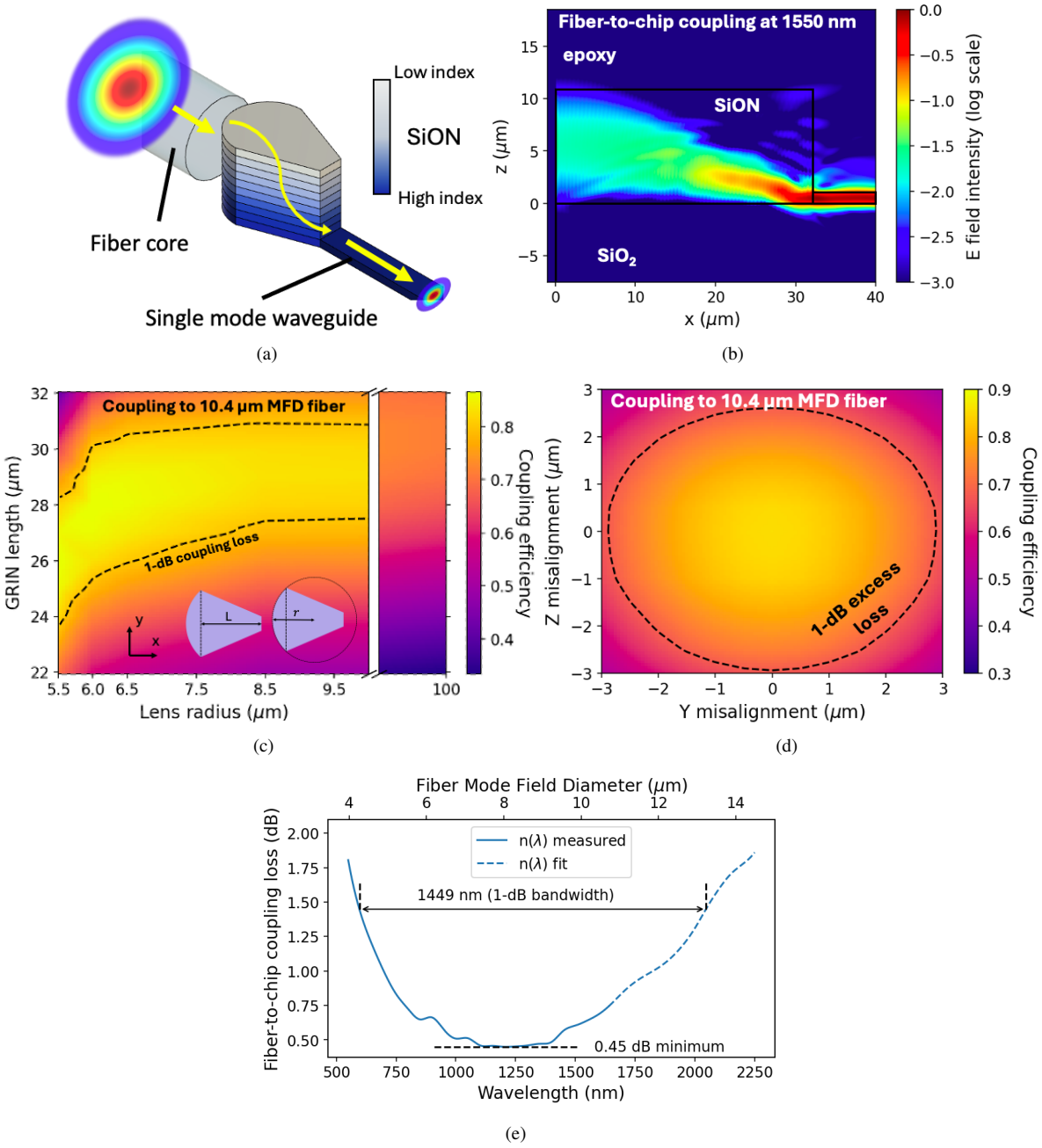


Figure 2: In (a) a conceptual diagram showing the modal transformation from the 10.4 μm wide SMF mode to the single mode SiON waveguide, with (b) showing the simulated cross sectional electric field intensity at 1550 nm wavelength for the TE mode on a logarithmic scale. In (c) coupling efficiency is shown as r and L are swept. The dotted lines indicate 1-dB total coupling loss contours. In (d) coupling efficiency is shown as a function of lateral (Y) and vertical (Z) fiber misalignment. The dotted lines in this case represent 1-dB excess loss from the minimum simulated coupling loss with zero misalignment. In (e) the coupling loss is shown as a function of wavelength for simulations where the refractive index (as a function of wavelength) of each SiON layer was imported from measured ellipsometry data for PECVD SiON films. The dotted section of the line indicates regions where a fit was used for refractive index, because the ellipsometer measurements did not extend past 1600 nm wavelength.

II. Device Design and Simulation Setup

The proposed coupler [5] involves using SiON layers with a parabolic GRIN profile to vertically focus an incoming optical mode from either an SMF or a GRIN on another chip into an output waveguide. In the lateral direction, a 2D lens and

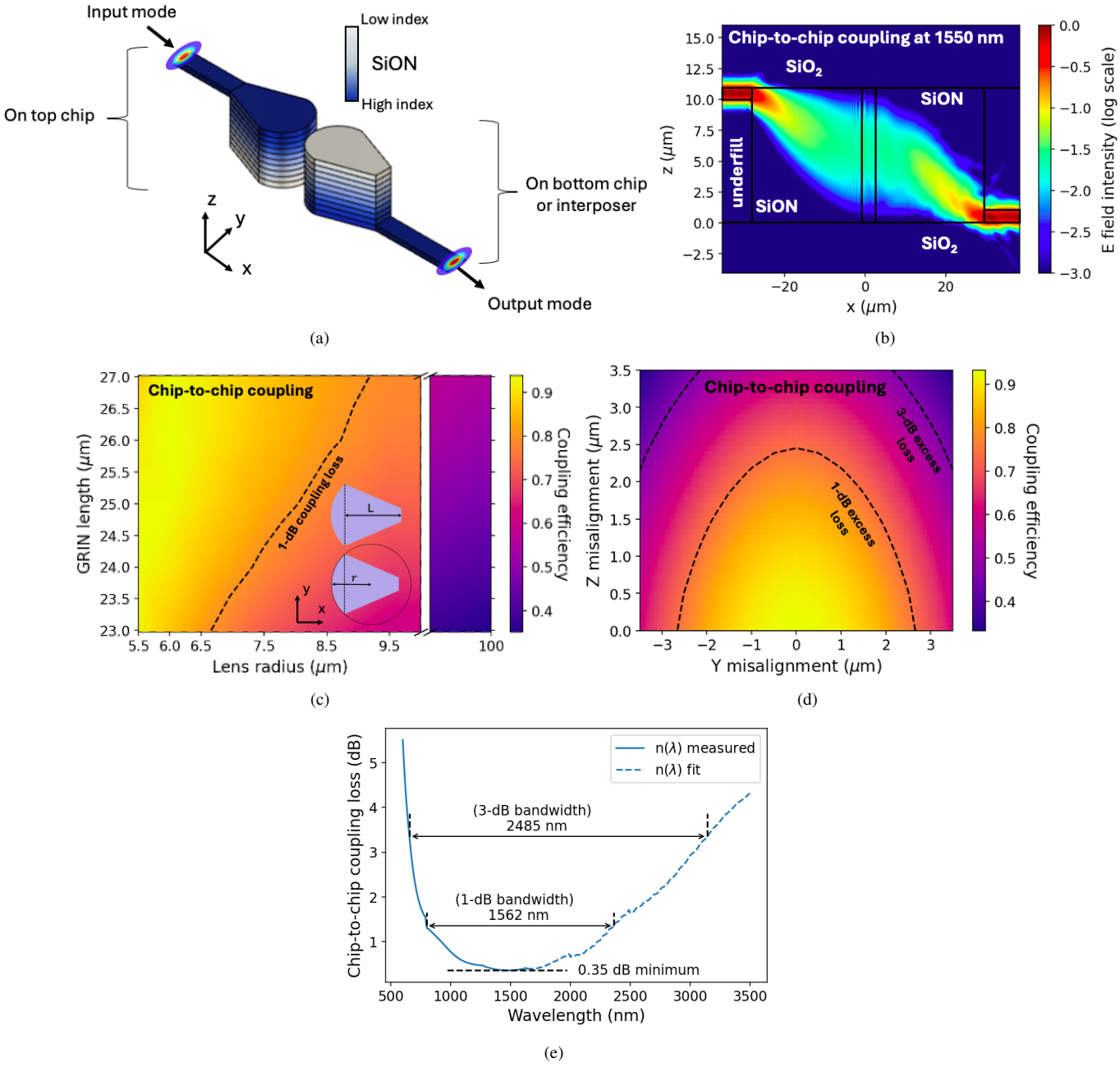


Figure 3: In (a) a conceptual diagram showing how a pair of GRIN lenses can be used for flip-chip optical coupling between two single mode SiON waveguides, with (b) showing the simulated cross sectional electric field intensity at 1550 nm wavelength for the TE mode on a logarithmic scale. In (c) coupling efficiency is shown as r and L are swept. The dotted lines indicate 1-dB total coupling loss contours. In (d) coupling efficiency is shown as a function of lateral (Y) and vertical (Z) chip misalignment. The dotted lines in this case represent 1-dB and 3-dB excess loss from the minimum simulated coupling loss with zero misalignment. In (e) the coupling loss is shown as a function of wavelength for 3D-FDTD simulations where the refractive index (as a function of wavelength) of each SiON layer was imported from measured ellipsometry data for PECVD SiON films, as in Fig. 2(e).

taper combination is used to horizontally focus the mode. The design of a single coupler is shown in Fig. 1(b) with relevant parameters to be optimized. The SiON layers are deposited using plasma enhanced chemical vapor deposition (PECVD) where the refractive index of the film can be tailored from silicon dioxide (SiO_2, n = 1.444) to silicon nitride (SiN_x, n >

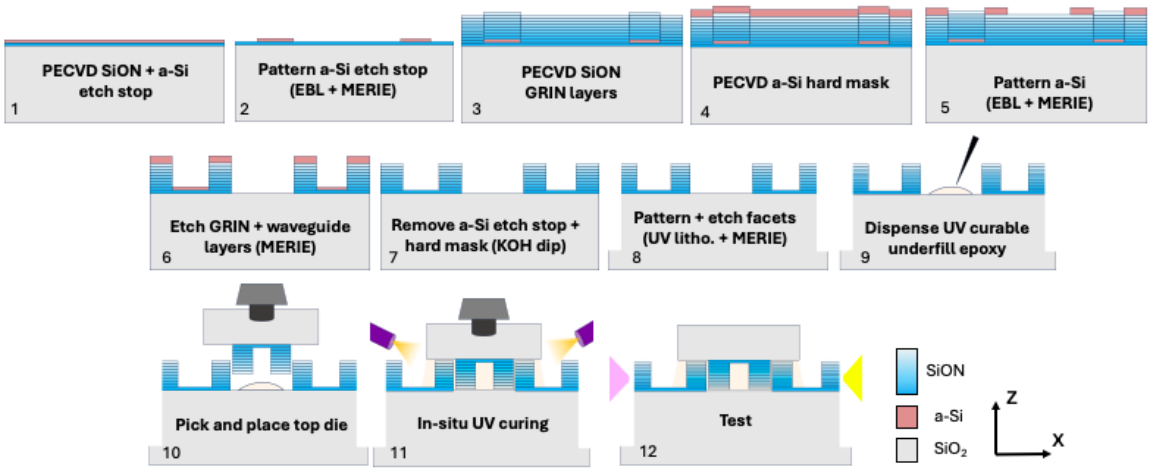


Figure 4: The full fabrication process flow is shown, starting from a bare glass or silicon substrate with a BOX layer and proceeding until PIC testing. The fabrication progress reported in this study includes data through step 7 of the above sequence. The edge facet etching, flip-chip bonding, and PIC testing processes (steps 8-12), including achieving sub-micron UV-curable epoxy bondline thicknesses, were demonstrated in [7] and can be applied here as well.

2) by adjusting the nitrous oxide (N_2O) flow rate during deposition [8]. The design of this coupler is distinct from previous GRIN couplers [9] in that it enables inter-chip coupling in addition to fiber-to-chip coupling, allowing for passive flip-chip assembly. Thus, this design provides a universal method for coupling into Si based waveguides from fiber-to-chip, chip-to-chip, surface mounted III-V source-to-chip, etc.

The design methodology involves optimizing the fiber-to-chip GRIN coupler which can then be simultaneously used for chip-to-chip optical coupling with little modification. The first step was to select the input mode field diameter (MFD_i) of the injected beam, and the refractive index (n_{wg}) and thickness (t_{wg}) of the output waveguides being coupled into. A flat facet, SMF-28 fiber with a 10.4 μm MFD was assumed, and waveguides with n_{wg} = 1.7 and t_{wg} = 1 μm were chosen based on prior data for depositing and patterning ammonia (NH_3) free SiON films using PECVD [9]. Note that this prior data also indicated that n_L = 1.48 should be used in place of SiO_2 (n_{SiO2} = 1.444 at 1550 nm) for PECVD SiON films in the limit that N_2O flow becomes large. With these selections, all remaining parameters become constrained including the GRIN thickness (T), GRIN width (W_{input}), number of layers (N), GRIN tip width (W_{tip}), output waveguide width (W_{wg}), and layer refractive indices, except the GRIN 2D lens radius of curvature (r) and GRIN taper length (L).

In particular, T and W_{input} were constrained to be approximately equal to MFD_i while W_{wg} and W_{tip} were constrained to the maximum waveguide width possible for the selections of n_{wg} and t_{wg}. To determine this maximum waveguide width, 2D Finite-Difference Eigenmode (FDE) simulations were executed which swept waveguide width assuming a cross section described by n_{wg} and t_{wg}, and surrounded by material with a refractive index equal to n_{SiO2}. Furthermore, N was constrained by t_{wg} and T such that the thickness of each layer in the GRIN was equal to t_{wg}. This constraint provides a reasonable minimum number of layers that should be used in the GRIN coupler which can always be increased for more advanced and optimized deposition processes. Finally, the coupler refractive index profile was parabolic from n_L to n_H, as shown in Fig. 1(c), using the following equation:

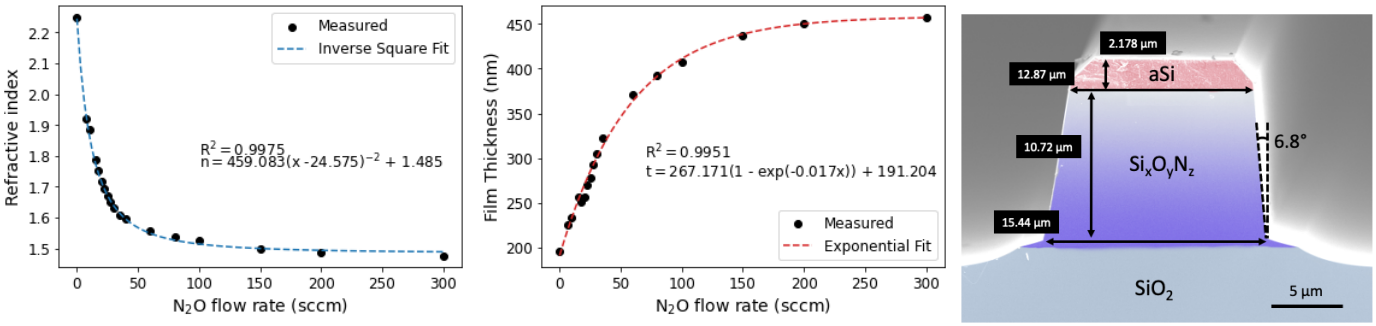
$$n(z) = n_H\left(1 - \frac{\alpha^2 z^2}{2}\right) \quad (1)$$

$$\alpha^2 = \frac{2\left(1 - \frac{n_L}{n_H}\right)}{T^2} \quad (2)$$

The parabolic refractive index profile is necessary in order create the vertical lensing effect predicted by Fermat's Principle and the ray equation [10]. From Fig. 1(c), the continuous parabolic refractive index change (i.e. the ideal case) is achieved using a stepped index profile where each layer's refractive index is controlled using progressively higher N_2O

Table 1: Summary of the design selections, constraints, and variables to be swept over

	Selections			Constraints							Variables	
Parameter	MFD_i	n_{wg}	t_{wg}	T	W_{input}	N	W_{tip}	W_{wg}	n_i	n_f	r	L
Value	10.4 μm	1.7	1 μm	11 μm	11 μm	11	1.2 μm	1.2 μm	1.48	1.7	5.5-100 μm	22-32 μm



(a) (b) (c)

Figure 5: In (a) the PECVD SiON film refractive index as a function of the N_2O flow rate during deposition is shown with an inverse square fit to the data. Similar data, but for film thickness versus N_2O flow rate and with an exponential fit, can be found in (b). In (c) a false colored cross sectional SEM image of a dummy GRIN lens structure is shown before removal of the aSi hard mask.

flow rates as stack height increases. To obtain the horizontal lensing effect from the physical lens etched into the GRIN coupler facet, an equation for the lens surface (ℓ) needed to be developed as a function of r. The lens surface is constrained such that it must intersect exactly at the edge of the GRIN at the points $(0, \frac{W_{input}}{2})$ and $(0, \frac{-W_{input}}{2})$ according to the coordinate system in Fig. 1(b) (assuming $(x,y) = (0,0)$ is at the center of the input of the GRIN coupler). The equation of ℓ is then:

$$\ell = r - \sqrt{r^2 - \left(\frac{W_{input}}{2}\right)^2} \tag{3}$$

From these relationships, it is clear that the minimum r value that can be used is $\frac{W_{input}}{2}$ and as $r \to \infty$ that $\ell \to 0$ and the GRIN becomes flat faceted. This fact was used to establish bounds for sweeping the value of r during simulations to be 5.5-100 μm. Finally, the focal length of an asymmetric GRIN lens with a parabolic refractive index profile can be approximated as $\frac{\pi}{2\alpha}$, which is one quarter the period of the ray oscillation as described in [10]. For the refractive index profile described by Table 1, this indicates $\alpha \approx 0.051\ \mu m^{-2}$ and the focal length for a flat faceted GRIN is approximately 30 μm. This fact was used to establish bounds for sweeping the value of L during simulations to be 22-32 μm, centered slightly below 30 μm, since the lens section also contributes to vertical focusing.

With these selections and constraints, r and L were swept over using 3D Finite-Difference Time-Domain (FDTD) simulations to optimize the design for maximum fiber-to-chip and chip-to-chip coupling efficiency. Simulations were also performed to determine the maximum allowable 1-dB excess loss misalignment tolerance for pick-and-place operations, as well as the 1-dB excess loss wavelength tolerance (a useful metric when applying the coupler in wavelength division multiplexing operations).

III. Simulation Results

A conceptual diagram, alongside a cross sectional figure showing the simulated modal transformation on a logarithmic scale from the SMF to the single mode SiON waveguide, can be found in Fig. 2(a) and 2(b), respectively. The simulated results for transverse electric (TE) mode fiber-to-chip coupling efficiency, shown in Fig. 2(c), demonstrated that for a lens radius of 5.5 μm and length of 26 μm, the coupling efficiency was 86.6% (0.62 dB loss) at 1550 nm wavelength and 89.9% (0.46 dB loss) at 1310 nm wavelength. Also, a fabrication tolerance of $> \pm 1$ μm for r and L was observed before a 1 dB excess loss penalty was incurred, as shown in Fig. 2(c) also. In terms of the tolerance to fiber misalignment, the 1-dB lateral alignment tolerance was $\pm$ 2.88 μm as shown in Fig. 2(d). The vertical alignment tolerance depends on the direction of misalignment, since the GRIN lens refractive index profile is asymmetric. The 1-dB vertical alignment tolerance when the fiber is shifted in the negative Z direction is 2.99 μm and in the positive Z direction it is 2.58 μm, also shown in Fig. 2(d). In addition, when the refractive index of each SiON layer in the simulation as a function of wavelength was imported using measured ellipsometry data (described later in Section IV.) for optimized N_2O flow rates, the fiber-to-chip coupling demonstrated a 1-dB wavelength tolerance (i.e. 1-dB bandwidth) exceeding 1400 nm (from 597 nm to 2046 nm) as shown in Fig. 2(e). Note that to perform this simulation, the SMF MFD was also varied as a function of wavelength from 530 nm to 2250 nm, as shown in Fig. 2(e), based on MFD data for commercially available SMFs [20].

Likewise, a similar conceptual diagram and simulated modal transformation can be found in Fig. 3(a) and 3(b), respectively, for chip-to-interposer or chip-to-chip optical coupling. Moreover, for TE mode chip-to-chip coupling, the optimized r and L were determined to be 6 μm and 26 μm, respectively, as shown in Fig. 3(c). This data also demon-

Table 2: Summary of recent examples of chip-to-chip optical coupling schemes. This list does not include all chip-to-chip coupling schemes and is only meant to yield a general idea of competing designs and performance. The shaded cells indicate studies where only simulation results were reported. Reported coupling loss values are for 1550 nm wavelength except in [11] and [12] where coupling loss was measured at 850 nm and 1310 nm wavelength (as indicated by the 1-dB bandwidth column).

Package	**Coupler**	**Coupling Loss (dB)**	**1-dB Align. Tol. (μm)**		**1-dB Bandwidth (nm)**	**LxW (μm)**	**Ref.**
			Lateral	**Vertical**			
InP to SOI	Edge	0.25	± 0.7	± 0.5	120 (1510-1630)	75x0.4	[13]
InP to SOI	Edge	0.9	± 1.7	± 0.5	120 (1510-1630)	250x0.4	[13]
SOI to SOI	PWB	1.6	/	/	> 300 (1280-1580)	2 (W)	[14]
SOI to polymer	Evanescent	1.25/0.5 (TE/TM) < 0.5 (TE/TM)	± 2 /	/	± 60 (1310) ± 70 (1550)	1500x6.5	[12]
Polymer to polymer	Free form	0.22 (TE) 0.25 (TM)	± 1.3	35	± 200 (850)	10x30	[11]
SOI to polymer	Evanescent	0.2	> ± 5 ± 1.5° (yaw)	0.5	± 100 (1550)	200x15.3	[15]
SOI to IOX	Evanescent	< 1 (TE/TM)	± 4	3	± 30 (1550)	1500x12	[16]
Si_3N_4 to IOX	Evanescent	0.7	> ± 4	< 2	75 (1515-1590)	2000x11	[17]
Si_3N_4 to Si_3N_4	Evanescent	0.54	< ± 2	< 0.8	400 (1200-1600)	1000x3	[18]
SOI to SOI	Grating	0.94	/	/	21 (1539-1560)	20x20	[19]
SiN_x to SOI	Evanescent	0.39 (TE)	± 1.56	> 1.1	160 (1480-1640)	520x1	[7]
SiON to SiON	**GRIN**	0.37 (TE)	± **2.66**	**2.45** **11 (rise)**	1562 (798-2360)	**60.2x11**	**this work**

strated a > 92% coupling efficiency (< 0.37 dB loss) at 1550 nm wavelength and 90.8% coupling efficiency (0.42 dB loss) at 1310 nm wavelength between waveguides separated by an 11 μm vertical gap. The 1-dB excess loss lateral and vertical alignment tolerances for the chip-to-chip coupling scenario, shown in Fig. 3(d), were determined to be > ± 2.66 μm and 2.45 μm, respectively. Finally, like the fiber-to-chip case, the chip-to-chip coupling data also demonstrated a 1-dB wavelength tolerance (i.e. 1-dB bandwidth) exceeding 1400 nm (from 798-2360 nm).

IV. Fabrication

Prior work demonstrated successful fabrication of GRIN fiber-to-chip couplers with 2D lenses and showed coupling losses of 0.4 dB from 1530-1625 nm for connecting to a fiber with a 6.8 μm MFD [9]. In terms of fabrication, this work adds to the prior work by increasing the GRIN stack thickness from 6 μm to 11 μm to couple light from flat-faceted, SMF-28 fibers with a 10.4 μm MFD. In addition, the fabrication of GRIN lenses on glass substrates was explored as this is useful to the development of high performance substrates with integrated silicon based waveguides [21]. A similar process to [9] was used as a starting point, with the exception of electron beam lithography (EBL) in place of i-line lithography. This was not done due to small features - the smallest feature size of the GRIN lens design is > 1 μm - but rather the lack of access to a repeatable process for patterning 1 μm features using the UV photolithography tools within the available cleanroom facilities. A step by step schematic showing the full process flow for the GRIN coupler fabrication, including edge facet formation, flip-chip die bonding, and PIC testing, can be found in Fig. 4.

Process development involved first establishing PECVD processes for depositing SiON films with a controllable refractive index from 1.45 to > 2.0 at 1550 nm wavelength. This was accomplished by using SiH_4, NH_3, and N_2O precursors and varying the N_2O flow rate for each layer using a Samco PD220NL tool. The Samco PD220NL tool cannot reach high enough plasma densities to dissociate N_2; therefore, NH_3 needed to be added as a precursor. The refractive index and thickness of the films were measured using a Semilab SE-2000 spectroscopic ellipsometer. The resultant data for refractive index and thickness as a function of N_2O flow rate can be found in Fig. 5(a) and 5(b), respectively.

As alluded to in Section III., the refractive index data was also used to simulate fiber-to-chip and chip-to-chip coupling where n(λ) for the SiON layers was updated using the measured refractive index data from ellipsometry. By using the measured refractive index data, a more accurate model can be obtained for wavelengths extending beyond the 1250-1650 nm regime and even into the visible, where refractive index has a stronger dependence on wavelength. As mentioned in Sec-

tion III., the resultant data for fiber-to-chip and chip-to-chip wavelength dependence using the measured n(λ) is shown in Fig. 2(e) and 3(e). The dotted line section on these plots signifies that n(λ) for each SiON layer was implemented using the Cauchy parameters from the fitted ellipsometry measurements, since the ellipsometry tool used cannot record data for $\lambda > 1600$ nm.

The next process step to address was the deposition, patterning, and etching of the amorphous silicon (aSi) films used as an etch stop for the waveguide layer (steps 1-2 in Fig. 4) and as a hard mask for defining the > 10 μm thick GRIN structure (step 4-6 in Fig. 4). The aSi etch stop protocol built off of the protocol established in [7] for the EBL of thin SOI and SiN_x-on-glass films using a diluted AZ nLOF 2020 photoresist. In this case, the material stack used for initial process development was 400 nm PECVD aSi on 700 nm PECVD SiON on a 3 μm buried oxide (BOX) on bulk Si. The resulting process could then be translated to glass substrates using the EBL discharging protocol outline in [7]. The primary changes to the EBL process were to the photoresist thickness after spinning, which was increased to approximately 800 nm, and to the etching process, which was switched to a magnetically enhanced reactive ion etching (MERIE) process with a chlorine/hydrogen bromide (Cl_2/HBr) gas chemistry. For the aSi hard mask, the thickness needed to be increased in order to define the nearly twice as thick GRIN stack which increased from 6 μm to 11 μm. Therefore, processes were successfully established for patterning and etching a 4 μm thick PECVD aSi hard mask both on Si with a 3 μm BOX and on fused silica substrates. The 4 μm aSi hard mask process was the same as the aSi etch stop process, except that the PECVD step was 80 minutes instead of 8 min, the EBL step used a 4 μm undiluted AZ nLOF 2035 resist, and the MERIE step had a longer time. Finally, to etch through all the SiON layers of the GRIN, a 91 minute MERIE step using a CHF_3/Ar gas chemistry was used. For the etching steps, the sample could remain inside the Applied Materials Precision 5000 RF generated, MERIE tool and merely switch chambers depending on whether a chlorine or fluorine based chemistry was being used.

All in all, with the 4 μm PECVD aSi hard mask, GRIN structures > 10 μm thick were successfully formed with a sidewall slope of 83.2°. The false colored cross sectional SEM image shown in Fig. 5(c), which was from a dose test sample used to optimize the EBL process, shows an example of a fabricated GRIN structure. Note that this image is not for the optimized dose, which showed a final accuracy of < 100 nm to the design value according to the width of the top of the GRIN. It is important to note that all developed processes involved temperatures < 350°C using standard, CMOS foundry compatible toolsets, allowing for simple integration into BEOL process flows similar to electrical bump integration.

V. Discussion

The device presented in this work was the first proposal using GRIN couplers for flip-chip optical connections and described a scalable method for fabrication of such structures. In comparing this device to other inter-chip couplers shown in Table 2, the GRIN chip-to-chip coupler displayed a maximum simulated coupling efficiency of > 92% (< 0.37 dB loss), which was competitive to other inter-chip designs demonstrating sub-dB performance. Moreover, the simulated chip-to-chip lateral alignment tolerance of > ± 2.5 μm is not only wide enough to use automated pick-and-place die bonders for passive assembly in high volume manufacturing [22], but is also on par with inter-chip evanescent, grating, free form, and edge coupling designs. Also, the less than 65 μm length and 11 μm width of this design makes it a compact option for coupling over significant vertical chip-to-chip gap sizes > 11 μm. For example, other inter-chip designs may require > 1 mm in length to achieve a < ± 2 μm vertical chip-to-chip distance [17].

Furthermore, with the ability to be placed at a 20 μm lateral pitch and form 2D arrays, this coupler provides a path for high density optical connectivity. A 20 μm pitch equates to 50 connections/mm, which is a > 5 times improvement compared to the maximum SMF density of 8 connections/mm resulting from the 125 μm fiber cladding. Another noteworthy aspect of the this coupler is the exceptionally large 1-dB bandwidth of > 1400 nm for both fiber-to-chip and chip-to-chip coupling, limited effectively only by the transparency of the material. This wide wavelength window is in part due to the fact that the vertical focal length of the GRIN lens ($\frac{\pi}{2\alpha}$) has little wavelength dependence as described by 2. The lateral focal length also has little wavelength dependence since it primarily acts to assist the GRIN lateral taper. This indicates the GRIN coupler could be used for WDM schemes across the near-IR spectrum. The simulated data and above advantages indicate that this GRIN coupler design can support optical fan- out for Pbps I/O with a sub-dB total coupling loss contribution.

In terms of fabrication, the data presented here showed that controlling the refractive index of PECVD SiON films across the range needed by the GRIN coupler (1.45 to > 2) using N_2O flow rate is a feasible strategy. In addition, the feasibility of patterning and etching GRIN lens structures > 10 μm thick with > 10 SiON layers was established using thick PECVD aSi hard masks, EBL, and MERIE processes. The significant minimum feature size of 1 μm indicates that i-line photolithography could be used in place of EBL for patterning as well. The presented fabrication flow was executed on both Si substrates with a 3 μm BOX and fused silica substrates, indicating the feasibility for implementation on two common interposer materials for high performance applications. In future studies, the fabrication work presented here will be combined with the edge facet dry etching techniques, flip-chip PIC bonding processes, and PIC testing strategies established in [7] to bring the GRIN fiber-to-chip and chip-to-chip coupling designs to fruition.

VI. Conclusion

A graded index chip-to-chip and fiber-to-chip coupler was designed and simulated using standard microelectronic foundry materials and processes. The coupler showed low losses of less than 1 dB, broadband performance with a bandwidth greater than 360 nm, and alignment tolerant operation of greater than ± 2 μm, allowing for pick-and-place die bonders to be used for chip assembly. Fabrication processes were successfully established for forming integrated graded index couplers which allow the coupler to be made twice as thick and be made on silicon and glass substrates. This work highlights the potential for this coupler as a universal interface for high volume manufacturing of photonic integrated circuits.

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