The Ideal Switch® with Advanced Glass Packaging

Aric Shorey, Jeff Baloun and Mark Walker
Menlo Microsystems
49 Discovery Suite 150
Irvine, CA 92618
Ph: +1-949-771-0277; Email: aric.shorey@menlomicro.com

Abstract

There has been a lot of work done over the past decade showing the advantages of using glass-based packaging for many microelectronics applications. Much of this work has been motivated by advantages provided by the material properties of glass. As an insulator, packaging enables devices with low electrical loss relative to semiconducting materials, such as silicon, as the operational frequency increases. Furthermore, the manufacturing processes for glass substrates provide numerous other potential benefits. Some glasses, such as fused silica (FS) offer extremely low loss tangent making it well suited for high frequency applications to minimize electrical loss in the system. Other glass types, such as those used for Display applications, are alkali free, have a coefficient of thermal expansion (CTE) close to Si and are fabricated in both thin and large (e.g. panel) form factors. This provides excellent opportunities for process cost savings for large substrates and interposers, while also maintaining excellent electrical performance. With all of these potential advantages in enhanced microelectronic performance, there have been numerous efforts to establish the manufacture of glass-based devices, but supply chain readiness has hampered the development of a robust supply of these solutions. Menlo Microsystems has established a glass device based supply chain to enable the volume manufacture of the Ideal Switch® technology. Below we describe the device and discuss some of the work Menlo has done to transition into production and packaging of the glass Ideal Switch.

Key words

Glass, MEMS switch, Ideal Switch®, through glass via (TGV).

I. Introduction

There has been a lot of progress in establishing glass-based microelectronics solutions over the past several years. [1-6] The advantages of glass-based solutions have been well documented. These advantages include low electrical loss, ability to provide thin and large format (panel-based) solutions by leveraging capabilities enabled by the Display industry, as well as ability to tailor material properties by adjusting the glass composition. Furthermore, there have been numerous demonstrators and prototype devices that have been fabricated showing the performance advantages provided by glass-based devices. However, there have been some hurdles to overcome to transition proof of concept devices into volume manufacturing environments.

Menlo Microsystems has introduced a glass-based MEMS switch that utilizes through glass via (TGV) technology and transitioned into volume production. Created in the R&D labs at GE, advanced metallurgy solutions combined with utilization of glass packaging, has enabled the creation of the highly reliable, efficient and compact Ideal Switch®. It is the world's smallest, most reliable, and efficient micro-mechanical switch that can be used for numerous applications, including power. Several advantages are gained by taking advantage of the low electrical loss of glass and hermetic TGV. The TGV technology enables >60% smaller package size relative to wirebond. Fabricating the device in glass (fused silica), reduces parasitics by >75%. Furthermore, devices have a wide operational bandwidth from DC to > 50 GHz. The small form factor means you can have dozens of switches in a package millimeters in size that give reliable performance over billions of cycles.

To enable the volume manufacture of this device Menlo has driven advancements in the glass supply chain, leveraging mostly standard semiconductor manufacturing processes, on glass substrates (with and without TGV). This includes establishing hermetic TGV, multi-layer plated and deposited structures, hermetic wafer level glass to glass bonding, post-bond die singulation and device packaging in multiple formats. These devices pass standard JEDEC reliability testing and have operational lifetime in excess of 3 billion cycles.[7] Here, we discuss a number of advanced packaging processes employed by Menlo in the manufacturing process in a volume manufacturing environment as well as key performance metrics of the Ideal Switch®.

II. The Ideal Switch® - Glass Based MEMS Device

A. The Ideal Switch®

Menlo Microsystems has introduced a glass-based MEMS switch that utilizes glass packaging and through glass via (TGV) technology (see Fig. 1). Created in the R&D labs at GE, these MEMS solutions combined with utilization of glass packaging, has enabled the creation of the highly reliable Ideal Switch®. It is the world's smallest, most reliable, and efficient micro-mechanical switch that can be used for numerous applications, including power. The combination of glass, an excellent electrical insulator, and metal, an excellent electrical conductor, in a MEMS device platform enables next generation DC to RF switching technology. This electrostatically actuated cantilever-based MEMS device represents an important advancement in MEMS switching technology. Key innovations in cantilever metallurgy (Fig.2) result in structures that give increased strength, creep resistance and stable contact resistance that enables long life performance along with the PVD, electroplating and etch processing on glass substrates that enables the combined benefits of metal fabrication on fully insulating glass substrates. The alloy's composition was engineered to maintain both grain stability and minimal strain rate for typical MEMS loads. [6] The plot demonstrates the ability of the Ni alloy to withstand higher temperature and stresses than more typical Au alloys. Functionally, this leads to longer life performance.

The TGV technology utilized in Menlo's design, demonstrates the realization of the promised advantages provided by glass packaging solutions. [8] Namely:

- >60% smaller package size relative to wirebond.(die size as low as 2.5 mm)
- >75% reduction in parasitics and
- Devices with a wide operational bandwidth - from DC to > 50 GHz.

Devices can have dozens of switches in a small form factor that give reliable performance over billions of cycles. This results in a revolutionary switch device with broad market application for RF, Power, IoT, among others.

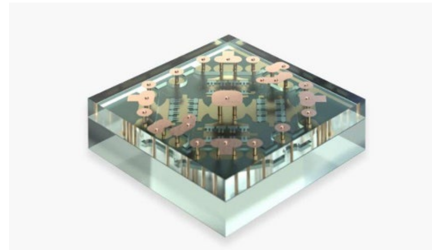


Fig. 1: 2-layer all glass design of Menlo Ideal Switch

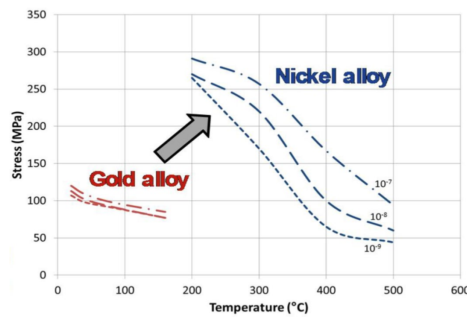


Fig. 2: Strain rate curves as a function of applied stress (derived from load time data).

B. Manufacturing Overview

The Ideal Switches are manufactured on 200 mm wafers made of FS glass. As mentioned above, the motivation for using FS is due to its extremely low loss tangent that results in low loss and low parasitic capacitance. The devices are manufactured in the following way:

- MEMS devices are fabricated on a 200 x 0.5 mm FS wafers
- A separate 200x0.3 mm thick "Cap wafer" is fabricated with through glass vias (TGV) to provide electrical interconnect to connect the signal pathways and drive the device control.
- These two wafers are wafer to wafer Au compression bonded with micron-level precision
- The wafers are then given an RDL, diced, tested, and packaged

Very few of the glass based processes needed to achieve the above manufacturing process were available for volume manufacture as Menlo set up the production process. As such, Menlo and its partners have solved a number of manufacturing challenges to enable the volume manufacture process available today. Below we summarize a few of these challenges faced across the entire manufacturing process by being a pioneer in glass device manufacture. Not only is volume manufacture of complex glass devices possible, but Menlo is poised to build upon this know-how to drive glass device manufacturing forward.

III. Manufacturing Challenges Lead to Opportunity

Menlo has faced and addressed a number of technical challenges as it built up the manufacturing process with partners. While many of the building blocks were in place, assembling the full process flow did come with some hurdles to overcome. Below we discuss a few of these and highlight the approaches Menlo has used to enable solutions suitable for volume production.

A. Through Glass Vias (TGV) and Surface Quality

The interest in using glass as a microelectronic substrate is not new and has been of interest for decades. In some ways, the emergence of through glass via (TGV) technology more than a decade ago was the start of people looking more seriously for packaging on large area interposers and substrates. Since that time, TGV technology has continued to develop. [9-10]

While there has been much discussion in the literature about TGV fabrication and metallization, there has been less discussion about how the manufacturing process can impact the wafer quality. There are several manufacturing processes for glass wafers. Wafers can be sliced, ground and polished from bulk glass boule, much like a Si wafer, or they can be formed in large sheets by the well-known float process or Corning's fusion forming process [9] for example. If the wafer manufacturing process utilizes grind and polish operations, there can be interactions with the TGV process that need to be well-managed.

The process to fabricate TGV often utilizes a laser and etch process. [11] If the wafers have not been sufficiently polished, the etch process will leave small pits on the surface that can lead to subsequent electrical shorts or opens in the device. Depending on the quality of the polish, the number of these pits can range from 100s to 10ks of pits on a surface after etching. This can be particularly problematic if the pits grow in diameter and depth after etch process and become filled with metal after the via metallization process. Figure 3 shows an image of a wafer after TGV wafer with particularly high number of pits, that was not a well-polished surface.

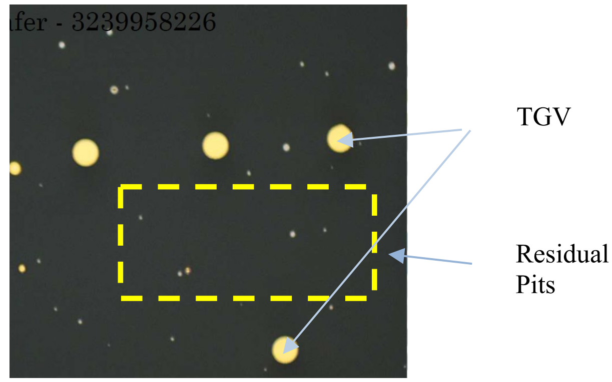


Fig. 3 – Residual pits on a inadequately polished wafer after etch can be filled with metal after TGV fabrication and impact performance.

The phenomenon of sub-surface damage (SSD) in glass is well-known in the fabrication of optics and work in laser optics highlighted the fact that etching can uncover this damage. [12] Since the TGV process incorporates an etch step in it manufacturing process, it is important that the final polish step during wafer fabrication is sufficient to remove the SSD from the grind and pre-polish steps. Menlo has worked with the supply chain to continue to improve the wafer fabrication to avoid downstream surface defects like the ones shown in Fig 3.

B. Dicing/Singulation Glass

Since the early days of trying to use glass as a microelectronics substrate, there has been a concern that glass cannot be effectively singulated due to challenges seen when attempts were made to singulate using the same process as used with silicon or organic substrates. Glass dicing, glass partial dicing and glass wafer singulation can and continues to use the very same equipment and process methodology as today's typical volume production semiconductor materials with tool adjustments for material type. Process variables such as feed-speed, spindle speed, kerf widths, dicing wheel grit and bond selections should be cornered to the glass type and thickness being used in your specific product. Menlo collaborated with its back-end supplier (UNISEM-MALAYSIA) and used dicing saw tool and consumable materials vendor (DISCO) to select the best fit for wheel grit and initial target process speeds for its Fused Silica 800um thick wafer stacks.

As a brittle material, glass has the potential for scratches, fractures, chipping, and delamination, much like silicon. It becomes critical to invest in the process cornering of ~~a~~ saw that captures the product characteristics such as glass type, product structure such as stacked glass or single plane substrate and thickness. Menlo uses a stacked glass structure with Au thermocompression bonding (TCB) to provide a hermetic seal. The risk of the potential impact of micro-cracking, chipping into the TCB bond seal potentially creating a fine leak consequence that your final test may not be able to identify is of real concern.

To protect from a fine leak event aggravated by the saw singulation process and provide a backbone test infrastructure, Menlo does a partial cut whose depth just surpasses the metal seal and uses its maximum Kerf width blade. This process reduces the depth of cut and associated stress on the saw cut itself, exposes the seal metal prior to full device singulation and allows the ability to place a glass wafer on a 8” wafer sort chuck for thermal and room temperature gang probe testing. Each device with the exposed seal metal can now validate hermetic compliance with correct yield mapping.

Once the wafer has been fully tested the wafer returns to the saw process for a full singulation and preparation for tape and reel (T&R) that would include device selection from the tested wafer and auto-inspection for potential saw defects.

Figure 4 shows examples of initial dicing operations. With a non-optimized process chip sizes in excess of 100 um was typical. However, the process was optimized with focus on the parameters such as:

- Kerf width
- Feed rate
- Blade type/wear rate

Through process optimization much better performance as shown in Fig. 5 was achieved. The average die chip size was reduced by > 2x from > 100 um to < 50 um. This reduced chip size, of course, has very important positive implications on the strength and reliability of the packaged die.

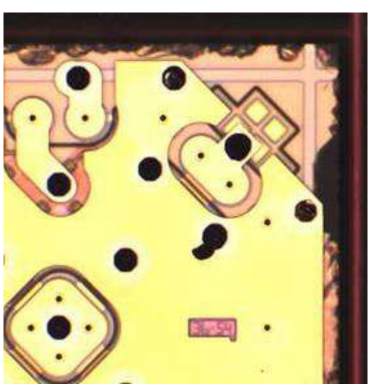


Fig 4: Singulated die with non-optimized dicing process. Chip size ~100 um was common.

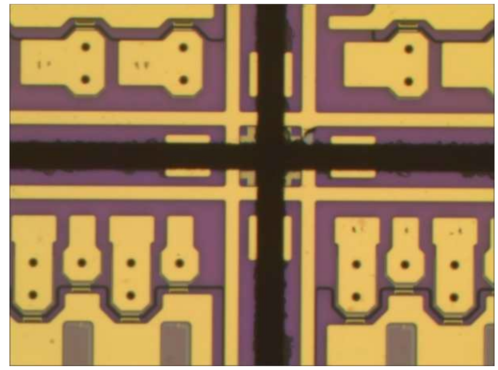
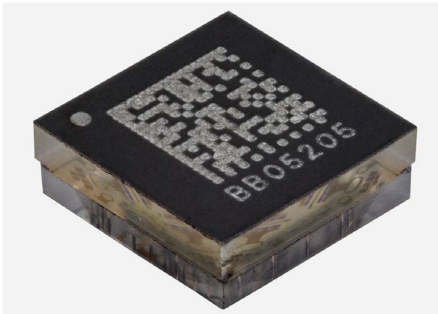


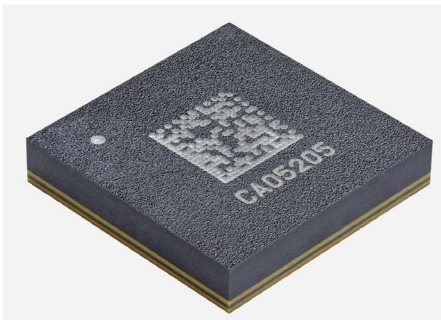
Fig. 5: Singulated Die with the optimized dicing process. Chip size reduced from an average of > 100 um to < 50 um.

C. Device Packaging

The investment in TGV technology has been significant with multiple materials and process investigated. The products demand for hermetic compliance throughout the Chip Scale Packaging (CSP) processing and Cap/MEMS integration remains an important technical focus today with improvement plans/roadmaps and continued investments required both inside Menlo and with its supply chain partners. The combined low RF and DC losses to drive next generation switch product capability along with the hermitic package need for the switch cycle life drove conflicting parameters. Performance drove the need for more and thicker via metallization while hermeticy drives the stresses between the metal and glass to the glass’s fracture point. The challenges created by significant mismatch of the coefficient of thermal expansion (CTE) of FS glass and the via metals can create an increased potential for via cracking, wafer warping and via hermetic breach. These are all design and manufacturing challenges from via shape, sidewall adhesion, via fill materials, via geometry and others that were developed, optimized and implemented in production. Menlo has worked with the supply chain and addressed the challenges and continues drive the production yield curve. Menlo has established processes for hermetic TGVs with substantially improved quality, wafer to wafer TCB with MEMS devices, partial and full singulation of bonded 200 mm FS wafers, device packaging and test. Menlo offers final tested products that meet JEDEC standards with multiple SMT packaging options as highlighted in Fig. 6.



Menlo MM5130 CSP MEMS Ideal Switch®. Die size 2.5x2.5 mm.



Menlo MM5600 family SiP MEMS integrated with driver. Package size 8x8 mm.

Fig. 6: Examples of Menlo final packaged glass die

IV. Discussion

In comparison to other interconnect technologies, the cost and yield loss of integration itself and the complexities and risks of supply chain logistics is high. So why select this interconnect solution and why continue to invest in this technology's maturity roadmap? The payback comes in the form of standardization. MEMS have had a long-standing reputation and consequence of non-standard form factors and test infrastructure that challenge established high volume microelectronics operations both in cost, efficiency, and tool sharing. Menlo's product portfolio, while being a 100% MEMS product line uses all standard test and volume package infrastructure found in OSAT operations. In addition, the package standardization aides EMS operations making it easier for reflow process profiling, tool integration and allowing acceptance of the product benefits without the penalty of non-standard form factors.

As in all early adoption of new methods and technical breakthroughs, volume acceptance and time will drive the cost model to its appropriate competitive position. As the demand for MEMSs products grows with requirements that form factor adhere to current volume infrastructures in both assembly and test, TGV and Hermetic TGV in a multitude of materials that include glass will be critical in the solution tree.

V. Conclusion

Menlo Microsystems has built upon the recent developments in TGV technology and solved many back-end challenges to enable volume production of the glass-based Ideal Switch®. Utilizing the properties of glass and novel metallurgical solutions enables the orders of magnitude improvement in performance relative to other switch technologies with respect to lifetime reliability, size reduction, power handling and low power consumption. Overcoming many of the challenges that have prohibited other groups from advancing from prototype to production fabrication has set the stage for future advancements in Menlo's glass-based device fabrication through packaging and SiP offerings.

Acknowledgment

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