Metastable Fine Grain Cu for Hybrid Bonding Applications

Pingping Ye, Jianwen Han, Stephan Braye, Abdelhamid ElSawy, Harshul Khanna, Veronica Hayes, Adam Letize, Kyle Whitten, Thomas Richardson, Elie Najjar
MacdermidAlpha
60 Parrott Drive
Shelton, CT, 06484, USA
Ph: 203-575-5718
Email: pingping.ye@macdermidalpha.com

Abstract
Utilizing metastable fine-grain copper offers an opportunity to implement low-thermal budget hybrid bonding techniques. We outline several methods for characterizing fine-grain structures and a screening process to refine these structures. Furthermore, we explore the differences in copper grain evolution between blanket and patterned wafers at room temperature. Finally, we introduce metastable fine-grain copper, which demonstrates stability for four weeks of self-annealing and maintains stability through annealing at 150°C for 2 hours, with grain growth occurring at 250°C. The capability to maintain fine-grain copper over an extended period presents a promising solution for low-thermal budget hybrid bonding.

Keywords
Fine grain Cu, metastable, hybrid bonding, WLP

I. Introduction

Wafer-level packaging (WLP) with heterogeneous integration boosts I/O counts while reducing footprint as feature and pitch sizes shrink [1]. Traditional methods like C4 bump, C2 bump, and micropillar with SnAg cap have advanced the field to include Cu-Cu direct bonding and hybrid bonding without solder cap, particularly for high-density 2.5D and 3D packaging [2]. Hybrid bonding (HB) integrates dielectric and metal bonds, bypassing under-bump metallization and underfill, facilitating direct connections, and enabling pitches below 10 μm, where electrical and thermomechanical limitations constrain solder. This approach, reminiscent of a monolithic package, significantly reduces latency and heat generation. Sony's adoption of Cu-Cu bonding in 2016 for image sensor applications marked a milestone, with subsequent advancements seen in AMD's 3D V-Cache device and Intel Foveros Direct technology [3,4,5]. However, current bonding techniques require high temperatures exceeding 300 °C. To address this, industry and academia are exploring innovative materials and techniques, focusing primarily on fine-grain and nanotwinned Cu (nt-Cu). Nanotwinned Cu offers the potential for lower bonding temperatures due to its (111) plane-dominated texture, enhancing atomic diffusivity and reducing the thermal budget [6-12]. Alternatively, fine-grain Cu provides another avenue for lowering the thermal budget. Metastable fine-grain Cu maintains stability during the queue time before bonding, with grain growth occurring during bonding. The energy released during grain growth at the bonding process promotes Cu interdiffusion, resulting in stronger bonding [9,13].

This paper presents various methods to characterize the Cu microstructure for Cu grain evolution with self-annealing and high-temperature annealing. We then discuss the fabrication of metastable fine-grain Cu on blanket and patterned wafers and propose a solution for a low thermal budget fine-grain process for hybrid bonding.

II. Material and methods

Plating chemical and apparatus

The basic makeup solution consists of copper sulfate, sulfuric acid, and hydrochloric acid for chloride ions. The plating bath includes makeup solutions and multiple proprietary organic additives. We utilize VSP Biologic Potentiostat to perform coupon-level testing with a mini-cell, water jacket, or beaker. A water bath controls the plating temperature at 25 °C. The anode is either an insoluble Titanium anode or a soluble Cu anode.

Grain size, microstructure, and mechanical characterization

In this section, we will briefly introduce several methods for grain size and grain microstructure characterization. The most direct method is electron backscattered diffraction (EBSD). Fig. 1 shows the EBSD grain map. Grains are usually determined with a 5° tolerance angle and a 5-pixel minimum requirement. The grain size can be calculated through the vendors' software. However, EBSD requires a smooth surface and is not widely available in academia and industry. Another direct method is the focus ion beam (FIB) images, as shown in Fig. 2. Different crystal orientations affect the number of secondary electrons escaping from the specimen, making the different grains appear with different contrast, offering a high spatial resolution. In the results and discussion, the FIB image is the primary method to characterize the grain size on the patterned wafer. Other indirect methods include X-ray diffraction (XRD) and sheet resistance. We use XRD (Bruker AXS, D8 discovered with VÅNTEC-500 area detector) and sheet resistance (Filmetrics, R50, 4-point probe) to characterize the grain size during our chemistry screening process. SIMS determines the impurity of plated Cu.

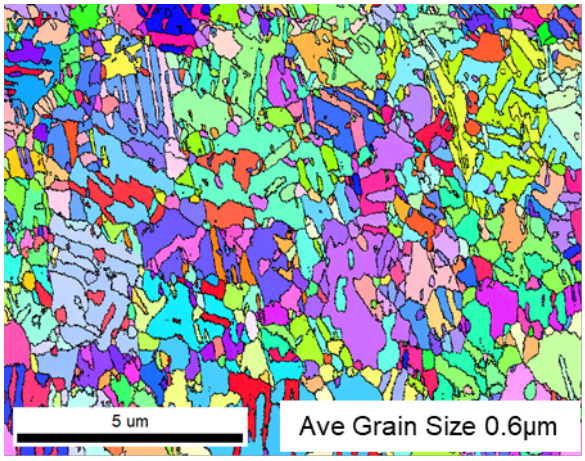

Fig. 1 EBSD grain maps

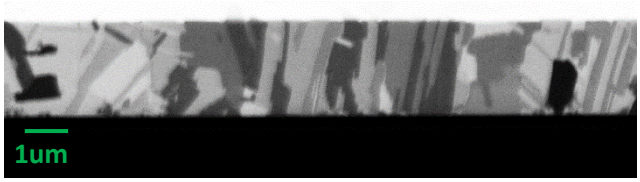

Fig. 2 FIB images showing the grain through the Cu film.

III. Results and Discussion

A. Fabrication of metastable FG on blanket wafer

In our chemistry screening process, we utilized XRD with a 2D detector to assess grain stability swiftly. Fig. 3 illustrates three XRD scans of distinct Cu deposits generated via electrodeposition with varying additives—processes A, B, and C—following a room temperature self-annealing period of two weeks. Without extensive data integration and analysis, these area detector frames provide a quick overview of Cu deposits' texture and grain size. The observed Debye rings exhibit smooth and continuous patterns for processes A and B, indicating that both deposits are polycrystalline and fine-grained. Conversely, the ring for process C appears continuous yet sporadic, suggesting that the deposit of C is polycrystalline but is large grain. Hence, based on the XRD results, we can infer that processes A and B can maintain a fine grain structure after two weeks of self-annealing, while process C does not exhibit this characteristic.

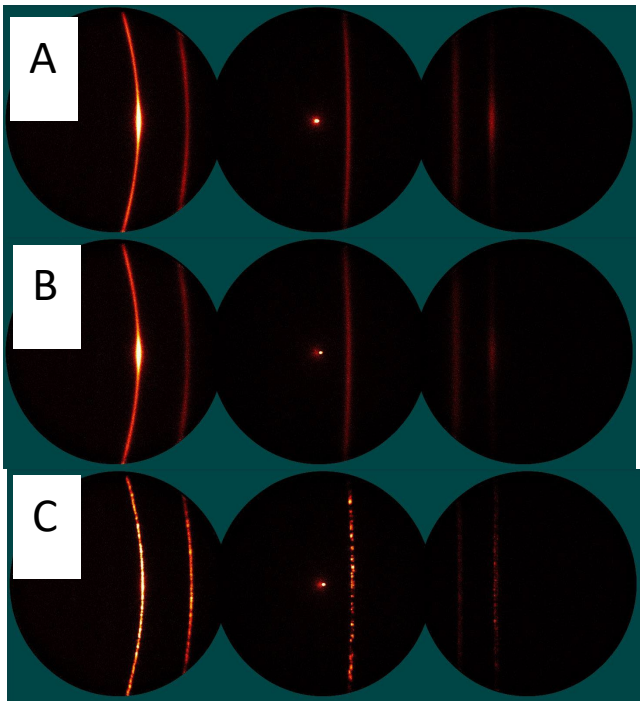

Fig. 3 2D XRD diffraction frame showing smaller grain of both process A and B compared with process C.

We utilized sheet resistance measurement as another means to assess grain stability. In Fig. 4, we observe the sheet resistance change over a 7-day room temperature self-annealing period for two electrodeposited Cu films labeled Cu film A and Cu film B plated on blanket wafer. In the case of Cu film A, the sheet resistance gradually decreases

throughout the seven days. Conversely, for Cu film B, there is a significant decrease in sheet resistance by the second day, followed by a stable level after that. This change in sheet resistance is due to changes in grain size and the number of grain boundaries. The increase in grain size, accompanied by a reduction in grain boundary density, increases the electron-free path, thereby reducing electron scattering and consequently lowering sheet resistance. The gradual reduction in sheet resistance observed for Cu film A suggests a slow evolution in grain size and a gradual recrystallization/growth process, indicating that Cu film A consists of metastable fine grains. In contrast, Cu film B exhibits a rapid rate of recrystallization/growth, achieving thermodynamic stability after just one day of self-annealing. Therefore, sheet resistance is another rapid and straightforward method for screening the chemistry involved in fine-grain processes.

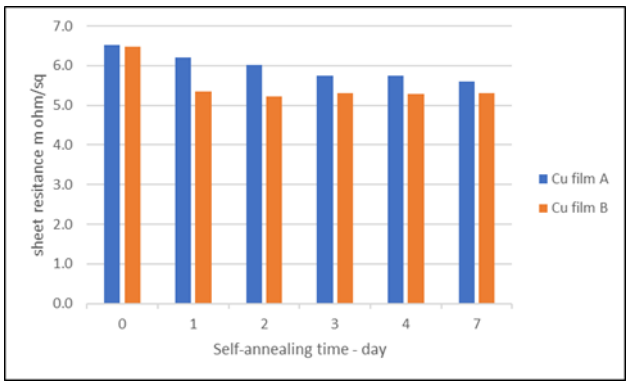

Fig. 4 Sheet resistance of Cu film A and B as a function of room temperature self-annealing time

The disparity of Cu grain evolution on a blanket and patterned wafer

Following the initial assessment of chemistry and process on the blanket wafer, the subsequent stage involves evaluating the stability of fine grain on the patterned wafer. Fig. 5 compares grain stability between processes A and B on the blanket and patterned wafers. In the case of Process A, the fine grain exhibits stability for two weeks of room temperature self-annealing on both types of wafers. Conversely, Process B demonstrates stable fine grain on the blanket wafer, but on the patterned wafer, grain growth occurs after three days of self-annealing, which falls short of the required duration for queue time before bonding. The industry consensus suggests that fine grain should remain stable for at least 2 to 3 weeks of self-annealing. The disparity in Cu grain structure evolution during self-annealing between the blanket and patterned wafers may

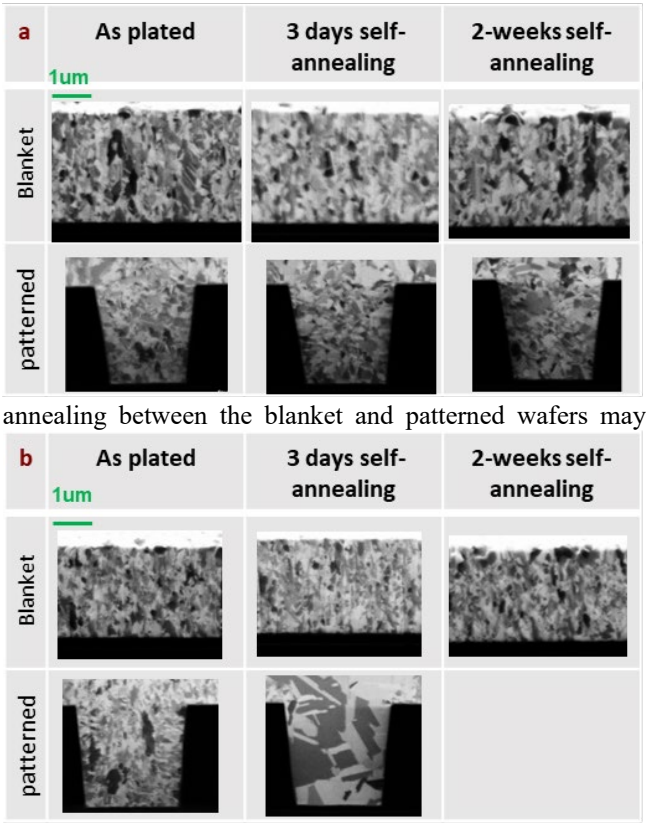

Fig. 5 comparison of grain stability between processes A and B on both the blanket and patterned wafers

stem from the additional external stress relieved with the patterned wafer for process B.

Recrystallization describes the spontaneous self-annealing of Cu films during storage at room temperature. Microstructural Evolution typically involves the movement of grain boundaries, and the equation determines the velocity of a grain boundary.

$$v = M * \Delta G \qquad (1)$$

M represents grain boundary mobility, and ΔG is the driving force [14]. Mobility M is thermally active and can be expressed by

$$M(T) = M(T0) * \frac{T0}{T} e^{-\frac{Ea}{K}\left(\frac{1}{T}-\frac{1}{T0}\right)} \qquad (2)$$

Assuming that mobility is only a thermally activated process and remains consistent between the blanket and patterned wafers, the discrepancy in grain growth rate is attributed to the additional driving force in the Cu coating with the patterned wafer. Not all the Cu structure evolution on the

blanket wafer can transfer to the patterned wafer.

Fabrication of metastable FG on patterned wafer

Hybrid bonding, occurring without external force, involves the thermal expansion of Cu during elevated temperature annealing to facilitate Cu interdiffusion [15]. The concept behind employing fine-grain Cu for low thermal budget hybrid bonding lies in utilizing the energy released during grain growth in the bonding process to promote Cu interdiffusion, thereby enhancing bonding strength. This energy can arise from grain boundary energy and stress changes resulting from grain growth [16,17]. The key criterion is to design metastable fine-grain Cu capable of maintaining its fine-grain structure at room temperature for at least 2 to 3 weeks while allowing grain growth at bonding temperatures, typically around 200 to 250°C. In specific device integration processes, the grains must remain stable at 150°C for 2 hours.

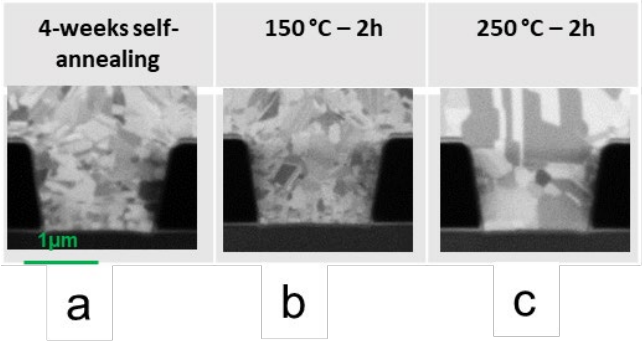

Fig. 6 Ion images of Cu grain, (a) 4 weeks self - annealing,

(b) 150 °C annealing for 2h, (c) 250 °C annealing for 2h

It is imperative to reduce the grain boundary velocity to ensure the stability of the metastable fine grain at room temperature for at least 2 to 3 weeks before bonding, as indicated in equation (1). The driving force ΔG, promoting the growth, originates from numerous factors such as grain boundaries, stacking faults, dislocation, surface energy, and elastic strain, with the opposite force due to the Zener pinning [17]. Our approach involves meticulous chemistry design to lower the driving force while relying less on Zener pinning to extend the self-annealing duration. Fig. 6 (a) illustrates our success in achieving grain stability even after four weeks of self-annealing, with a grain size of approximately 100 nm. Fig. 6 (b) further demonstrates that annealing at 150°C for 2 hours maintains similar grain characteristics to those observed after four weeks of self-annealing, indicating negligible grain growth due to limited grain boundary mobility.

Additionally, our investigation into grain growth during annealing at 250°C for 2 hours, depicted in Fig. 6 (c), reveals higher mobility at this elevated temperature, promoting significant grain growth. Compared to the four weeks of self-annealing, during which the Cu grain size remains around 100 nm, annealing at 250°C results in a much larger grain size. This anticipated strengthening of Cu bonding is attributed to the enhanced grain size resulting from reduced grain boundaries at the bonding annealing temperature.

III. Conclusion

We delineate various approaches for assessing fine-grain structures and detail the screening methodology to develop the metastable Cu fine-grain process. Additionally, we investigate how the geometry constraints from patterned wafers induce variances in copper grain evolution between uniform blanket wafers and patterned wafers under ambient conditions. We introduce metastable fine-grain copper, highlighting its stability over four weeks of self-annealing and its resilience during annealing at 150°C for 2 hours, with observable grain growth commencing at 250°C. These findings underscore its potential as a promising low-thermal budget hybrid bonding solution.

Acknowledgment

The authors thank our Marketing and Sales teams for discussing the fine-grain Cu for hybrid-bonding applications and providing customers' feedback. The authors also thank our Taiwan WLP application lab for their support and technical discussion.

References

[1] J. H. Lau, Semiconductor advanced packaging, Springer, 2021
[2] L. Mirkarimi and G. Gao, "Die-to-wafer hybrid bonding for 2.5D and 3D integration" Chip Scale Review, March and April 2020
[3] H. Tsugawa, H. Takahashi, T. Nomoto, et al., "3.2 Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology," IEDM, Dec. 2017.
[4] https://www.anandtech.com/show/16725/amd-demonstrates-stacked-vcache-technology-2-tbsec-for-15-gaming
[5] https://www.intel.com/content/www/us/en/newsroom/resources/lakefield.html
[6] J. Juang, C. Lu, K. Chen, C. Chen, P. Hus, C. Chen, K. Tu. "Copper to copper direct bonding on highly (111)-oriented nanotwinned copper in no-vacuum ambient." Scientific Reports 2018 8:13910
[7] Liu, C.M. et al. Low-temperature direct copper-to-copper bonding enabled by a creep on (111) surfaces of nanotwinned Cu Scientific Reports 5, 9734 (2015).
[8] P. Gondcharton, B. Imbert, L. Benaissa, V. Carron, M. Verdier, Kinetics of low-temperature direct copper-copper bonding. Microsystem Technologies. 21. 995-1001 (2015)
[9] L. Mirkarimi, C. Uzoh, D. Suwito, B. Lee, G. Fountain, T. Workman, J. Theil, and G. Gao, "The Influence of Cu Microstructure on Thermal Budget in Hybrid Bonding" ECTC 2022

[10] P. Ye, J. Han, S. Braye, K. Whitten, R. Hurtubise, T. Richardson, E. Najjar "Electrochemical plating of nanotwinned Cu for WLP applications" 2020 International Wafer Level Packaging Conference.
[11] J. Han, P. Ye, S. Braye, K. Whitten, C. Wang, D. Shaffer, A. Letize, B. Gokey, T. Richardson, E. Najjar, Electrochemical Plating System Development of Nanotwinned Cu for Multiple WLP Features, IMAPS 18th Conference, 2022
[12] P. Ye, J. Han, S. Braye, K. Whitten, V. Hayes, H. Khanna, A. Letize, T. Richardson, E. Najjar, "Transforming WLP Applications: Introducing Cutting-Edge Next-Generation Nanotwinned Copper," IMPAS, 56the International Symposium on Microelectronics, Oct 2-5, 2023.
[13] Y. Zhang, J. Wang, P. Dong, X. Zhang, W. Zhao, J. Liang, All Copper Is Not Created Equal – Examples of Grain Engineering in Plating, 2022 IEEE 72nd Electronic Components and Technology Conference.
[14] F.J. Humphreys and M. Hatherly, Recrystallization and related and related annealing phenomena, second edition, 2004
[15] 3D Microelectron IC Packaging: From Architectures to Applications, second edition, Springer
[16] J.M.E. Harper, C. Cabral, Jr., P.C. Andricacos, L. Gignac, I.C. Noyan, K.P. Rodbell, and C.K. Hu, Mechanisms for Microstructure Evolution in Electroplated Copper Thin Films near Room Temperature," Journal of Applied Physics, volume 86, number 5, 2516 – 2525, 1999.
[17] C. Detavernier; S. Rossnagel; C. Noyan; S. Guha; C. Cabral, Jr.; C. Lavoie, Thermodynamics, and kinetics of room-temperature microstructural evolution in copper film, J. Appl. Phys. 94, 2874–2881 (2003)