Advanced 3D Integrated Circuit Packaging: Metallurgical Improvement and FLOLA (Flux-Less Oxide-removal Laser Assembly) Process at a 9 ㎛-Pitch Micro-Bump

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Abstract

The study aimed to explore the thermal stability of the new bump metallurgy and evaluate the feasibility of flux-less bonding in 9 ㎛ pitch. A mechanical 3D-IC package structure was implemented to achieve this, connecting two chips vertically with a 9-micron bump pitch. The study used a diffusion barrier to suppress intermetallic compounds (IMCs) between the metal pillar "M" and the solder. A newly adopted Flux-Less oxide-removal Laser Assembly (FLOLA) was used to interconnect the top die to a 12-inch bottom wafer vertically at the wafer level process using neither fluxing nor cleaning. To verify the heat resistance property of diffusion barrier embedded micro-bumps, a high-temperature storage test (HTST) was conducted at 150 ℃ for 1000 hours and 180℃ for 500 hours, respectively. That samples were precisely grinded and polished to inspect cross-sections of solder joint, field-emission scanning electron microscopy (FE-SEM), energy dispersive X-ray spectroscopy (EDS), and plasma focused ion beam (PFIB) were used to characterize the behavior of IMC growth for iso-thermal aging time conditions. The reliability test result showed that diffusion barrier layer could suppress IMC growth effectively, and eliminate the void risk by volume shrinkage, shown like as a conventional nickel-solder(Ni-Sn) under bump metallurgy (UBM), completely.

Key words

Chiplet, Diffusion barrier, Fine-pitch micro-bump, Flux-less bonding, Heterogeneous integration, Intermetallic compound, 3D-IC.

I. Introduction

With the increasing demand for high-performance semiconductor devices for HPC and AI, chiplets and heterogeneous integration is beginning to attract much attention. This trend has drawn the technical requirements for advanced packaging technology to satisfy high I/O density and low latency needs. Even in such advanced package technologies, one of the core technologies must be advanced interconnection technologies such as hybrid copper bonding (HCB), providing electrical and thermal benefits such as reduced power consumption, enhanced thermal dissipation, and robust reliability in high I/O counts and fine pitches [1~2]. However, the broad adoption of HCB seems to have progressed slowly because of the difficulties in controlling copper dishing in chemical-mechanical polishing (CMP) and extremely sensitive void and particle control [3~4].

Meanwhile, micro-bump interconnection technologies, represented as mass reflow (MR), laser-assisted bonding (LAB), and thermal-compression bonding (TCB), have been widely used for flip-chip soldering bump may have limits to be applied to ultra-fine pitch micro-bumps under 10 ㎛ due to height variance of an electroplated micro-bump, a limited bonding alignment, and underfill void caused by either flux residue or extremely narrow die-to-substrate gap. However, a more fundamental difficulty lies ahead of the above-stated challenges in the micro-bump metallurgy itself. As bump pitch decreases, surface diffusion between solder and metal pillar becomes dominant due to the increased surface-to-

volume ratio. Therefore, intermetallic compounds (IMCs) grow faster than in wider pitches [5~7]. Additionally, IMC's brittle nature will deteriorate micro-bumps' durability and increase the risk of bump cracks in assembly processes or reliability testing. For these reasons, the applications of conventional micro-bumps have been inevitability limited to over 10 ㎛ pitch.

This paper explored the feasibility of 9 ㎛ pitch micro-bump technology through an embodiment of a mechanical 3D-IC package structures like logic-to-logic, memory-to-logic, and other 3D stacking combinations. Firstly, two types of micro-bumps (Ni-SnAg, M-SnAg) were patterned and electroplated with 9 ㎛ pitch on 12-inch Si wafers, respectively. A diffusion barrier material was layered between metal pillar "M" and SnAg solder to improve the thermal stability by suppressing IMC growth. Secondly, the 12-inch wafer was diced to 9.5 ㎜ x 9.5 ㎜ chips. The chips were soldered on another 12-inch Si wafer patterned with 9 ㎛ pitch bumps by a newly adopted bonding process, Flux-Less Oxide-removal Laser Assembly (FLOLA). In the FLOLA, plasma pre-treatment using Ar+H_2 mixed gas was performed to remove oxide from the surface of the solder, and neither a fluxing nor a cleaning process was used. Finally, an encapsulation was done to protect micro-bumps by underfill dispensing and gap-filling. All the processes were carried out in a wafer level. For comparison of Ni-SnAg and M-SnAg bumps, high storage temperature testing (HTST) was conducted at 150℃ for 1000hours and at 180℃ for 500hours, respectively.

II. Experimental Procedure

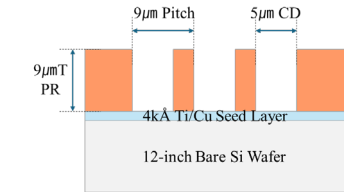
A. Test Vehicle

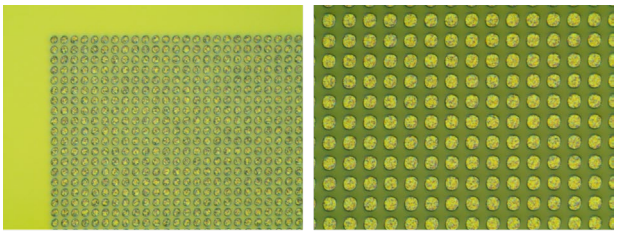
The test vehicle (TV) for 9 ㎛ pitch bumps was fabricated using conventional patterning and electroplating processes. Firstly, a photo-resist (PR) thickness of 9 ㎛ was coated on the 12-inch wafer that the Ti/Cu seed layer of 4kÅ formed in advance, and it was patterned by a photolithography process with a critical dimension (CD) of 5 ㎛. Secondly, electroplating (EP) was carried out with two types of micro-bumps, 6 ㎛ of which were of a total height. The details of TV are presented as TABLE I. A new diffusion barrier material was embedded to prevent the growth of IMC between SnAg solder and metal pillar "M," and it was designated to Leg2. Conventional Ni-SnAg micro-bumps were also electroplated on the same 12-inch wafer as Leg1 for a comparison of diffusion behavior. The measured bump pitch was 9.05 ㎛. Fig.1 (a) shows the top view of 9 ㎛ pitch micro-bumps after PR strip and seed etching. For same chips, a tilt-view of micro-bump arrays was observed by field emission scanning electron microscope (FE-SEM) as shown in Fig.1 (b).

B. Assembly Process Flow

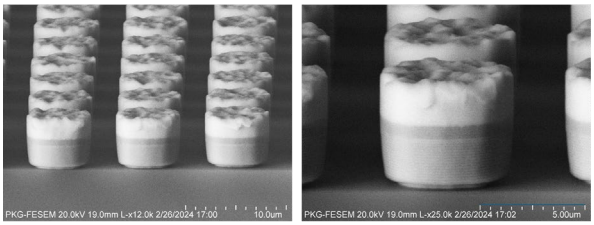
An overview of the assembly process flow was described in Fig.2. A 12-inch wafer after finishing bumping process was diced into 9.5 ㎜ x 9.5 ㎜ chips, and then soldered on the same 12-inch wafer by using the FLOLA process. FLOLA is a flux-less thermal-compression bonding process that uses an Ar+H_2 plasma treatment tool and a homogenized laser as heat sources. It requires neither an oxide removal fluxing nor a post-cleaning process for soldering. Additionally, FLOLA has a lower thermal expansion than the conventional TCB process and it was described in our previous work [8].

TABLE I. Test Vehicle Information

Process	Description	
Patterning		
Metallurgy	Ni-SnAg (Leg1)	M-SnAg (Leg2)
Pillar	Ni 4 ㎛	M 3 ㎛
Diffusion Barrier	N/A	1 ㎛
Solder	SnAg 2 ㎛	SnAg 2 ㎛
Total Height	6 ㎛	6 ㎛
Schematic		
Sample Size	50ea	50ea



(a) Top View



(b) Tilt view

Fig.1. 9 ㎛ pitch micro-bump array formed on 12-inch Si wafer. (a) Top view (optical microscope) (b) Tilt view (FE-SEM images)

After the soldering process, an underfill was dispensed to encapsulate a gap between the chips and a wafer. Underfill material's flowability was diversified into low, middle, and high levels to observe void behavior as a gap-filling property. TABLE II presents a scanning acoustic microscopy in C-mode (C-SAM) after curing at 175℃ for 2 hours. Pressurized oven wasn't selected to characterize its void trend clearly without pressurization benefits. As a result, void (white areas of CSAM images in TABLE II) decreased as increasing material's flowability, and "Underfill C" which had a lowest void area was selected as an encapsulation material for our reliability test.

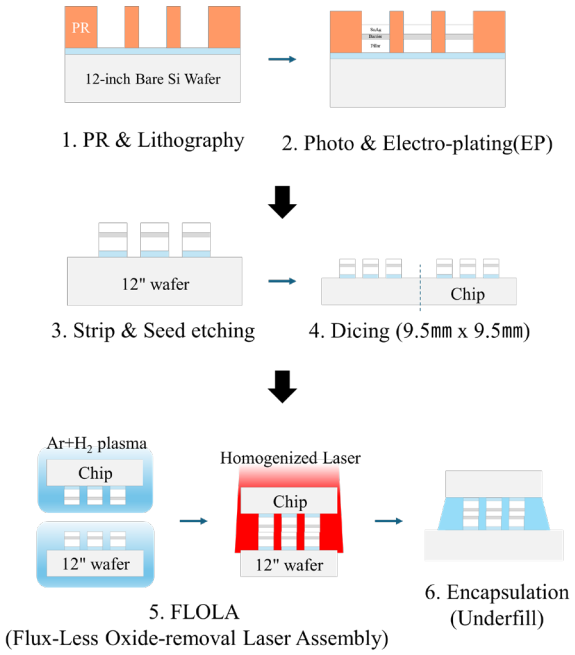


Fig.2. Assembly process flow.

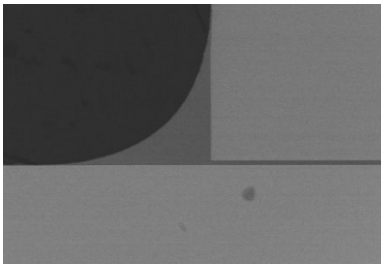
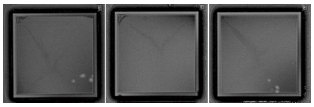


Fig.3. Cross-section image of a fillet

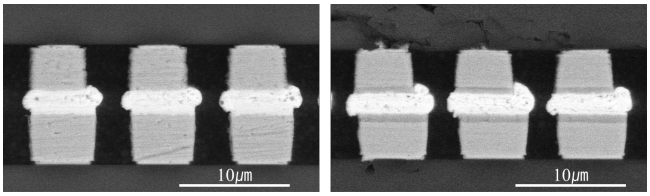
TABLE II. Void reduction as underfill flowaibility

Material (Flowability)	Representative Images (CSAM)	Void Area	Void (%)
Underfill A (Low)		289.7	2.4
Underfill B (Middle)		170.3	1.4
Underfill C (High)		65.2	0.5
Chip	9.5 ㎜ x 9.5 ㎜	12100	100.0

III. Result and Discussion

A. IMC growth comparison after assembly process

The samples were inspected through a destructive analysis with careful grinding and polishing to observe a cross-section of solder joint before reliability testing. Fig.4 presents cross-section images of micro-bumps after finishing assembly process. A few silica fillers come from underfill were stuck in relatively soft solder during grinding and polishing, and it is seen as some black dots in Fig.4 images. In both Leg1 and Leg2, the solder joints were formed well with neither non-wet nor short by precise bonding alignment control. But its lateral length between neighboring bumps' solders seems to be very tight to prevent short failure in mass production level. For these reasons, CD, solder height and other dimensions are required to be optimized necessarily with the controlling of bonding alignment precisely.



(a) Leg1 Ni-SnAg (b) Leg2 M-SnAg

Fig.4. Cross-section images of 9 ㎛ pitch micro-bumps. (a) Leg1 Ni-SnAg bumps, (b) Leg2 M-SnAg bumps with diffusion barrier embedded.

B. High Temperature Storage Test (HTST)

A high storage temperature test (HTST) was performed to observe the behavior of IMC. The test was conducted on both Leg1 and Leg2 samples for 1000 hours at 150°C, and 500

hours at 180℃ respectively. Reliability test conditions were described in TABLE III. In general, it is known that the condition of 180°C is much harsher than that of 150°C [9]. The cross-sections of solder joints for two legs were analyzed by FE-SEM, EDS, and PFIB after the destructive analysis by iso-thermal aging time (0~1000 hours) and temperature conditions (150°C and 180°C) respectively.

Fig.5 shows cross-sectional images by the aging time of Leg1(Ni-SnAg) and Leg2(M-SnAg), respectively. There is no significant difference in the appearance of the solder joints of Leg1 and Leg2 under the time zero condition. The difference between two legs becomes apparent after 1000 hours at 150°C. After 1000 hours, voids were examined in Leg1 but not in Leg2. At 180°C after 500 hours, the difference between the two becomes more pronounced. Some large voids were observed around solder of Leg1 and it may be caused by volume shrinkage of Ni-Sn IMC, resulted from Ni-Sn inter-diffusion. On the other hand, in the micro-bump of Leg2, the boundaries between the solder, the diffusion barrier, and the metal pillar "M" are still clear, and no voids were found. It has only slight boundary changes, which are presumed to be the result of solder-diffusion barrier reaction.

TABLE III. Reliaibility Test

Test Item	High storage temperature (HTS)	
Leg	Leg1	Leg2
Metallurgy	Ni-SnAg	M-SnAg
Temperature	150℃, 180℃	
Time	0~1000 hours	

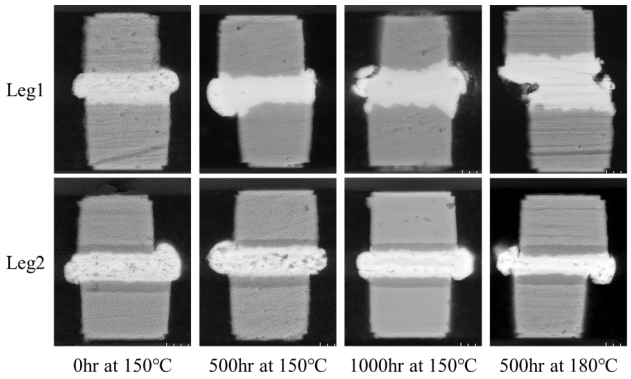


Fig.5. FE-SEM images as time and temperature of Leg1 Ni-SnAg and Leg2 M-SnAg.

An in-depth destructive analysis was conducted to examine its diffusion behavior in detail. Firstly, a top die was grinded in parallel to a chip surface. Secondly, the cross-section surface of a bump was vertically milled by Xe plasma additionally. Fig.6 shows PFIB-prepared cross-sections of micro-bumps and EDS line scan results. The IMC thickness at time-zero condition was roughly 0.36~0.76 ㎛ in Leg1 and it's more than twice thicker than 0.23~0.24 ㎛ in Leg2. Ag agglomeration (blue arrow in Fig.6 (c)) was seen in Leg2's solder joint area and is commonly inspected in SnAg solder [10].

Fig.7 is EDS line scan analysis result. In a comparison of Fig.7 (a) and (b), Sn's atomic composition decreased and Ni increased after aging of 500 hours at 180°C. Furthermore, the Ni-Sn ratio is maintained uniformly in a joint area. It indicates that all the solder is consumed completely by Ni-Sn inter-diffusion and it transformed to Ni_3Sn_4. Meanwhile, Fig.7 (c) and (d) show the trend of M-SnAg IMC. Sn's atomic composition decreased with the increase of both diffusion barrier (DB) and metal pillar "M" materials similar to that of Leg1, and it also means that all the solders in the joint gap were consumed at all. However, as seen in Fig.6, any voids by volume shrinkage weren't inspected in Leg2 different from Leg1. As a result, Leg1's IMC area seems to be expanded by continuous IMC growing vertically, while Leg2's IMC area seems to be suppressed under the limited area that diffusion barrier had defined. It implies that the diffusion barrier effectively inhibits the growth of IMC even under harsh conditions, such as 500 hours at 180℃.

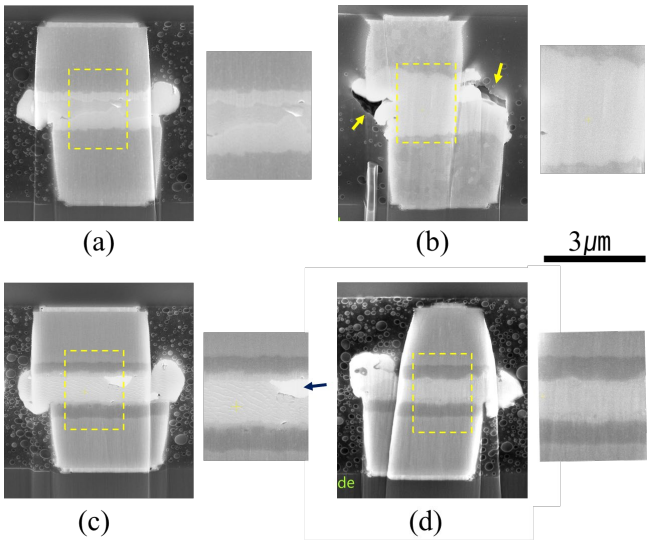


Fig.6. PFIB prepared cross-sections. (a) Leg1 (Ni-SnAg) time-zero, (b) Leg1 (Ni-SnAg) 500hours at 180℃, (c) Leg2 (M-SnAg) time-zero, (d) Leg2 (M-SnAg) 500hours at 180℃.

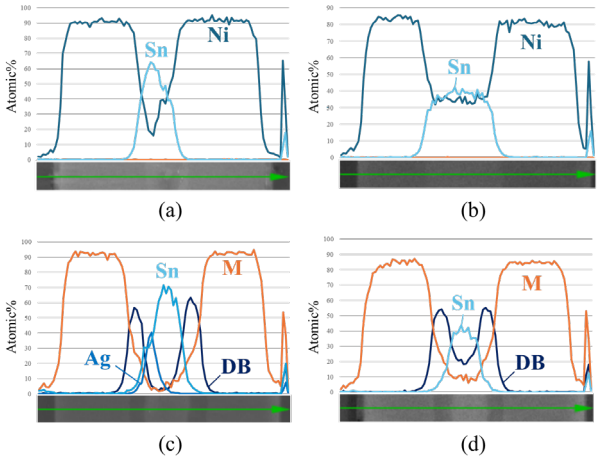


Fig.7. EDS Line-scan analysis result. (a) Leg1 (Ni-SnAg) time-zero, (b) Leg1 (Ni-SnAg) 500hours at 180℃, (c) Leg2 (M-SnAg) time-zero, (d) Leg2 (M-SnAg) 500hours at 180℃.

The amount of solder would decrease naturally as its pitch is scaled, in addition to it, a surface diffusion becomes dominant factor by increased surface-to-volume ratio. As a result, the solder in extremely fine pitch may be consumed completely and earlier than in wider pitches. Similarly, the time taken for all solders to transformed into IMC, will be also affected by either solder joint's pad-to-pad distance or IMC growth rate resulted from its bump metallurgy, because the pad-to-pad gap may be extremely narrow in a 9 ㎛ pitch bump, so the diffusion characteristics of components constituting the bump material may more directly affect the degree of IMC formation in the solder joint. Therefore, it is very important for understanding the relationships between joint gap and its bump metallurgy.

IV. Conclusion

Since the development of copper pillar, micro-bumps had played significant roles in the electrical interconnection of flip-chip packages. Today, its scope of application is wide, from tiny controllers of 3 ㎜ x 3 ㎜ size to mobile application processors, application-specific integrated circuits (ASICs), and even high-bandwidth memory (HBM), and those various bump metallurgies have been optimized to meet various technical requirements of the industry, such as high I/O counts and low latency with the electrical, mechanical, and thermal reliabilities. Therefore, improving and expanding this micro-bump technology must be an effective approach in the respect of utilizing those abundant infrastructure and stable production lines worldwide.

In our study on a 9 ㎛ pitch, we presented those improving and extending of micro-bump technology with new bump metallurgy, FLOLA process, and optimized gap-filling material. Our results showed superior thermal stability compared to existing Ni-Sn micro-bumps. No voids were found in the iso-thermal aging test for 500 hours at 180℃, and the IMC's growth was suppressed effectively by the diffusion barrier. The risk of flux residue was eliminated through FLOLA process completely, and the void decreased as improving the flowability of underfill materials.

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