Numerical Simulation on Stress on C4 Bump Distribution of Silicon Interposer

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Abstract
2.5D advanced packaging has become a major technological highlight in the development trend of semiconductor packaging from 2D to 3D. Various advanced CPUs/GPUs and high bandwidth memory (HBM) are integrated through 2.5D advanced packaging. The interconnection is achieved through the micro bumps of the chip and high-density BEOL layers on the frontside of the interposer, then by the through silicon vias (TSVs) connecting the upper and lower layers, and is finally soldered onto a traditional 2D packaging substrate through C4 (Controlled Collapsed Chip Connection) bumps. With the increasing demand for performance, 2.5D packaging requires more and more integrated chips with larger areas. There is a significant mismatch in the CTE (thermal expansion coefficient) between the silicon interposer and the substrate. Therefore, the effects will be significantly amplified, leading to reliability failure and even inability to proceed with the following packaging processes. Prospective finite element analysis (FEA) can be conducted on the shape and layout of C4 bumps to analyze their effect on mechanical stress buffering on the total package. Finally, based on these simulation results, the optimal combination is recommended so that the layout and shape of the C4 bumps can provide effective assistance for the overall stress buffering of the package.

Key words
C4 BUMP, FINITE ELEMENT ANALYSIS, SI INTERPOSER, STRESS, THERMAL EXPANSION COEFFICIENT

INTRODUCTION
With the continuous growth of performance requirements for electronic products, the demand for advanced semiconductor devices that can achieve high-performance computing applications is increasing. Following the paces of Moore's Law is becoming costly, advanced packaging can enhance chip performance by improving packaging methods without shrinking process nodes. With the support of emerging industries such as artificial intelligence (AI), autonomous driving, and the Internet of Things, advanced packaging technology can provide corresponding solutions. In recent years, 2.5D packaging technology has made significant progress, reducing the data transmission distance and time of chips, significantly reducing power consumption at a faster speed, which is in line with the industry [1].

Therefore, more integrations for chip types and sizes in 2.5D packaging, accompanied by a significant enlargement in the size of silicon interposers, is essential in fabrication. There is a significant mismatch in the CTE (coefficient of thermal expansion) between the encapsulation packaging material, silicon chips, silicon interposer, and substrate. During processing and final product application use, the impact caused by this mismatch will be significantly amplified, which may result in the inability to proceed with the packaging process and ultimately lead to reliability failure.

This phenomenon has attracted widespread attention. Many studies have been conducted from the packaging material perspective. Material properties of organic substrate were found as dominant, especially during the wafer packaging process. Using underfill material of low CTE and low storage modulus was effective in reducing warpage for wafer level assembly, while that of low CTE and high storage modulus was effective in reducing the strain of Cu pillar and solder. Meanwhile, material properties of underfill (UF) material had little impact on warpage change of fully assembled test vehicle [2]. High glass transition temperature (Tg) underfill, as well as a low modulus and low CTE substrate can mitigate the package warpage and stress development at the interface between interposer and underfill. Also, a larger Cu volume TSV interposer and thick substrate can lessen the warpage of the package and stress at the interface. Effect of glass CTE is also investigated. If glass CTE is increased from 3.2ppm to 5.7ppm, interposer warpage value is reduced, and variation could be reduced about 100um at Si removal process [3, 4].

In addition, corresponding process or structure adjustments can be made to mitigate stress and warping during the process. Interposers warpage alleviation on passivation film tuning can be achieved from film composition change or film thickness adjustment. By tuning the passivation film into compressive behavior, interposer warpage can be reduced [5]. Passivation film thickness is another important factor for warpage reduction, the thicker the film, the smaller the warpage was measured. By combining these two approaches, warpage can be minimized to desirable level with reasonable film thickness thanks to the contribution of composition tuning of passivation films including silicon nitride and silicon oxide.

Lower thermal stress and lower residual stress during the last solder ball process results in the lower warpage for the assembled 2.5D package [6]. The initial warpage difference between the organic substrate and the assembled 2.5D package with C4 bumps has significant effects on the warpage control of the final assembled BGA package, the warpage after reflow was reduced to 75% of that using SAC305 instead of Sn-57Bi solder. The full assembly was successfully processed using conventional assembly equipment and processes [7]. Ring type framework can also be designed to solve the warpage issue and improve the flatness of interposers [8].

Our research has been conducted on the manufacturability of 2.5D package and the impact of chip thickness during processing [9], but no research has been conducted on the interconnections of 2.5D package. After the completion of silicon interposer treatment, the package is soldered onto the substrate through flip chip process. The connection "Controlled Collapsed Chip Connection", abbreviated as C4, can make targeted adjustments. Therefore, in this work, we used Finite Element Analysis (FEA) simulation to study the layout of C4 bumps, and designed the shape, rotation angle, and dielectric layer of the bumps accordingly. It is anticipated to reduce stress as much as possible through changes in the layout.

EXPERIMENTAL METHODS

A. Test Package Structure

Fig.1 illustrates the structure of 2.5D package. A typical 2.5D structure includes multiple chiplets, as well as underfill and organic packaging materials that encapsulate around the chiplets. The chiplets are interconnected with the interposer, and the materials of the interposer generally include silicon, RDL, and embedded silicon bridge structures. In this study, only the interposer of silicon material is considered. Silicon interposer is finally interconnected with the substrate through the C4 structure. It can be seen that there are organic materials, inorganic materials, and metal bumps in this structure. Due to the mismatch of CTE, the composite of these materials experiences stress and strain, ultimately affecting the reliability of the overall structure.

The 2.5D package sets and package size are shown in Table I. In this package, a test vehicle is built for simulation. The dimensions of Chip A, Chip B, and Chip C are 12.5*15mm, 5*5.5mm, and 5*3mm, respectively. The size of the interposer is 24*16mm. This is a typical 2.5D structure as chip A can be considered as an SOC, Chip B is a typical size of I/O die, and Chip C is dummy silicon material that fills other blank areas to ensure the overall strength of the structure. The interposer size is about 400mm2 and can be a representative for 2.5D C4 bump distribution study.

Generally, Fig.2 is a typical C4 bump structure in 2.5D. The C4 bump is composed of Cu, Ni, Sn, or SnAg through electroplating deposition, which leads the power or signal to the substrate. The C4 bump plays a bridging role and is prone to failure during product use, as shown in Figure 3. Structural stress causes the C4 bump to break. PI material can be used as a buffer layer under C4 bump to reduce stress effects during use. Based on the above information, corresponding designs can be made for the layout of C4. Firstly, from the perspective of the coating area of the PI layer, the larger the area, the greater the stress on the entire surface. The purpose of the PI layer itself is only to reduce the stress in the interconnected area. Therefore, different conditions are set in this area for corresponding research. Secondly, the interposer package is subjected to tensile and shear stresses during use, resulting in corresponding strains. If in the direction of equivalent stress in tension and shear, C4 bump relies on changes in the size and shape to amplify the effective length in the direction of equivalent stress, thereby increasing C4's ability to resist stress, significantly reducing strain, and increasing fatigue life. Therefore, according to this perspective, the experiment was designed using fully circular and elliptical C4 bumps as comparative conditions. Finally, regarding the rotation angle, based on the dimensions selected in this work, different rotation angles are set, including all C4 bumps facing the same direction, and C4 bumps arranged according to the principle of symmetry and diverging in all directions, for relevant study. For the elliptical C4, two conditions are designed as a supplement, considering that the long side of the ellipse is in parallel with or perpendicular to the long side of the interposer. As shown in Figure 5 and Table II, DOE-1 and DOE-3 are circular C4 arranged on the interposer, with the difference being whether they are fully covered by PI or not. DOE X-1-angle (X refers to the Arabic number 1, 2 or 3) corresponds to elliptical dimensions (80*105um) arranged in the same direction, while DOE X-2-X and DOE X-3-X are two other types of ellipses (60*140um and 87.5*96um) with the same area as other DOEs.

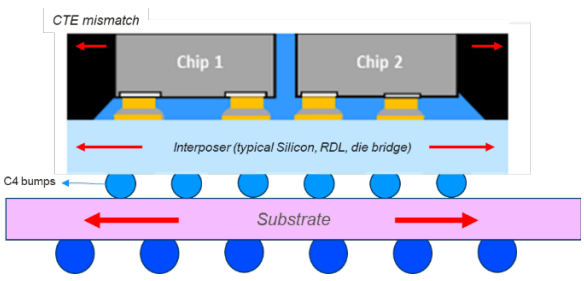


Fig.1 2.5D package structure

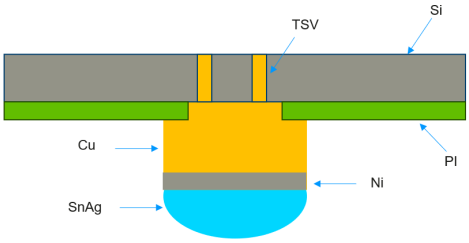


Fig.2 Typical cross sectional C4 bump structure

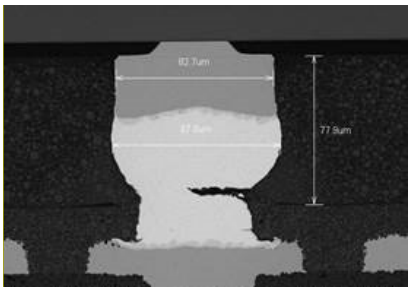


Fig.3 C4 cracking during reliability test

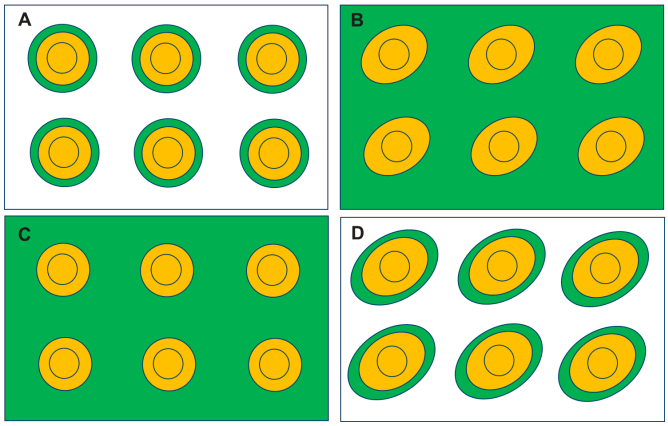


Fig.4 C4 bump layout structure
(A - round C4 with isolated PI coverage, B - elliptical C4 with full PI covergae, C - round C4 with full PI coverage, D - elliptical C4 with isolated PI covergae)

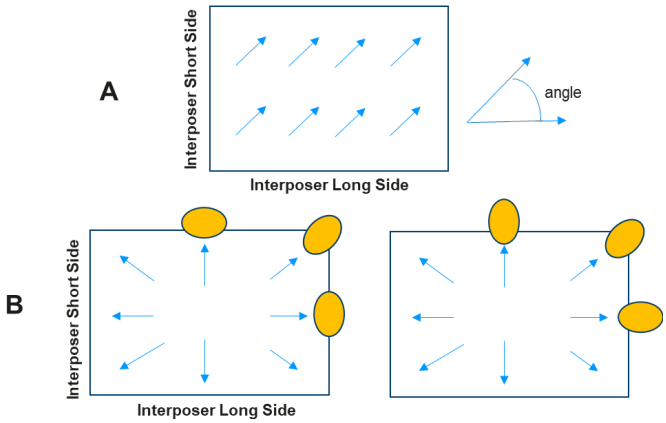


Fig.5 C4 bump directions
(A is for DOE X-X-angle, B is for DOE X-X-1 and DOE X-X-2)

Table I
The chiplet sets, package size in this evaluation

Chiplet	Size / mm
Chip A	12.5*15
Chip B	5*5.5
Chip C	5*3
Interposer	24*16
2.5D Package	34*34

Table II
DOE of C4 structure

#	C4		Full PI	Isolated PI	Same Directions	Flush to long side	Perpendicular to long side	DOE
	Round	Ellipse						
1	√		√					DOE-1
2		√	√		√			DOE-2-1-angle
		√	√			√		DOE2-1-1
		√	√				√	DOE2-1-2
3		√	√		√			DOE-2-2-angle
		√	√			√		DOE2-2-1
		√	√				√	DOE2-2-2
4		√	√		√			DOE-2-3-angle
		√	√			√		DOE-2-3-1
		√	√				√	DOE-2-3-2
5	√			√				DOE-3
6		√		√	√			DOE-3-1-angle
		√		√		√		DOE-3-1-1
		√		√			√	DOE-3-1-2
7		√		√	√			DOE-3-2-angle
		√		√		√		DOE3-2-1
		√		√			√	DOE3-2-2
8		√		√	√			DOE-3-3-angle
		√		√		√		DOE-3-3-1
		√		√			√	DOE-3-3-2

Table III
Material properties of 2.5D package

Materials			Interposer	UBM/Pillar	SR	Core	PI	Solder
Item		Unit	Si	Copper	AUS308	R1515E	Polyimide	Solder
Tg		C	NA	NA	100	270	230	NA
CTE	α1	ppm/C	2.8	17	60	9	65	21.7
	α2	ppm/C			130	---		
Young's modulus	25C	GPa	131	121	4.1	33	3.5	43
	260C	GPa			0.18	---		

B. Simulation Work Description

After the completion of the 2.5D AB1 structure on substrate, there is a reliability risk due to the mismatch in thermal expansion coefficient of the material. A finite element analysis was conducted on the interaction stress of the chip packaging using the universal finite element software Ansys with Statics module.

It is anticipated that by the optimization of the arrangement and layout of C4, corresponding stress can be dispersed and offset to counteract the stress generated during the package use. The simulation DOE mainly focuses on C4 shape and angle on the PI on the interposer back. The modeling optimization includes Top Die, EMC, and Underfill. The material prpperties are shown in Table III. Metal Ni in C4 bumps is not included in order to simplify the structure. To ensure simulation accuracy, Boolean operations are performed

within the interposer and TSVs are embedded. Select the temperature 175℃ during reflow process as the stress-free temperature, and then extract the stress at room temperature. The geometry and meshes are shown in Figure 6.

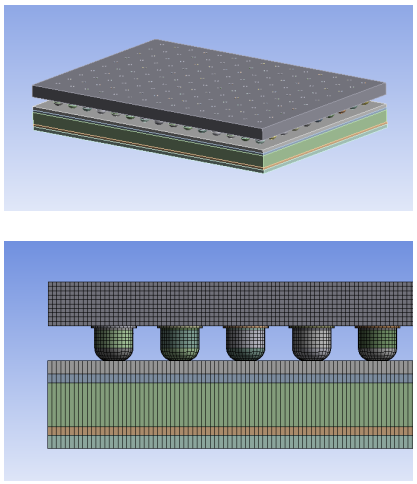
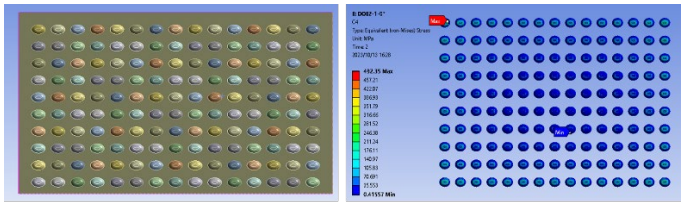


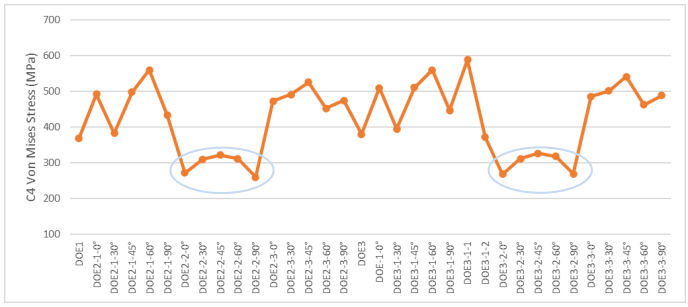
Fig. 6. Geometry and meshes

RESULTS AND DISCUSSION

A. C4 stress analysis on same direction



(a)



(b)

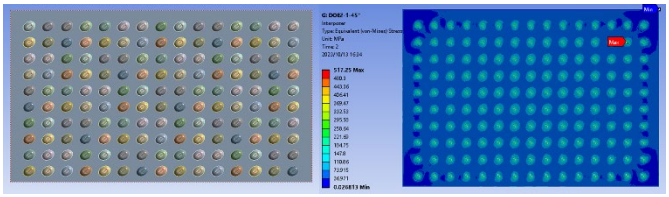
Fig. 7. C4 stress distribution on same direction

Based on the above discussion, as the examples in Fig.4 and Fig.5, different rotation angles of C4 are set on the interposer. At the same time, focus on observing the influence of three sizes of ellipses on stress. For elliptical C4, it is set the same rotation angle at this point. Then, simulate and summerize the stress of maximum C4 stress distribution on same direction. Figure 7 (a) is an example of stress analysis during the simulation process, and (b) shows the statistical stress values.

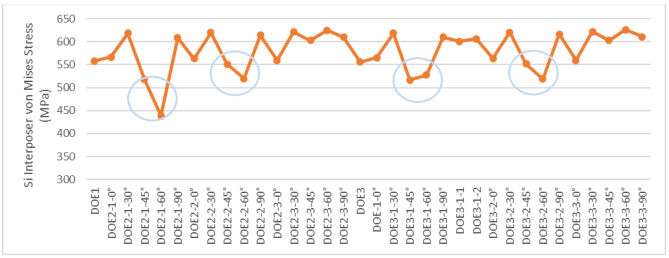
From the results, it can be seen that there is a very significant decrease in C4 stress for DOE2-2 and DOE3-2 with various directions. Only the combination of DOE X-2 has a significant effect on reducing stress, correspondingly, the angles of DOEX-1 and DOEX-3 did not reduce the stress.

Therefore, the size setting of the ellipse shape has a particularly significant impact on C4 stress, indicating that the larger the a/b of the ellipse, the more effective it is in reducing C4 stress. Moreover, the influence of angles on stress is minimal, with only stress values at 0 ° and 90 ° being smaller for DOE2-2 and DOE3-2 cases, indicating that stress is more mitigated in these two directions.

B. Si Interposer stress analysis on same direction



(a)



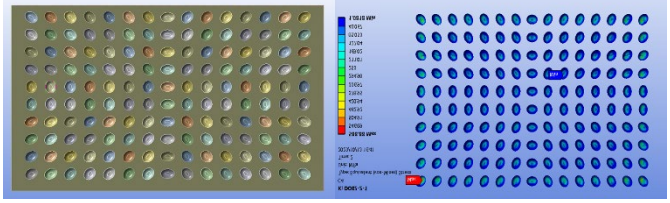
(b)

Fig. 8. Si interposer stress distribution on same direction

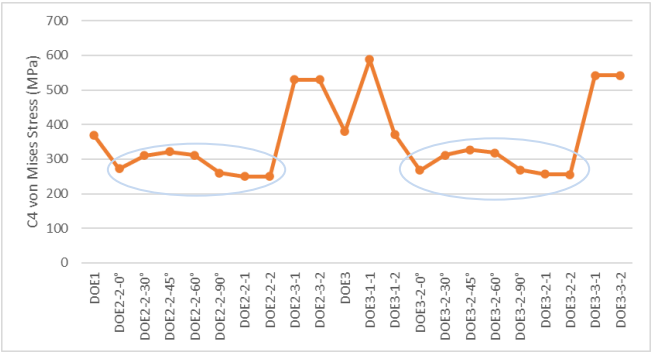
In the setting of the DOEs, the segmentation of PI is also a consideration point, and this change in C4 bump stress also needs to be checked to see if it has a corresponding impact on the Si interposer itself. Figure 8 (a) is an example of stress analysis during the simulation process, and (b) shows the stress values on the interposer that are statistically analyzed. It can be seen that except for the cases where the ellipse turns 45° and 60°, the influence of PI segmentation on the stress effect of the interposer cannot be seen in other cases. So whether PI has certain effect on the stress of the interposer can be considered based on the overall packaging in practical situations.

For cases where the stress values at 45° and 60° are significantly smaller, according to the von Mises stress calculation method [10], the encapsulated tensile stress in this direction may have been correspondingly offset, with shear stress dominating. In the actual reliability process, special attention should be paid to the anomalies from this perspective, and corresponding angle optimizations can also be made for layout in order to offset or bypass this dominated shear stress.

C. Stress analysis on dispersed directions



(a)



(b)

Fig. 9. Stress distribution on dispersed directions

Finally, compare the stress trend of elliptical C4 with the arrangement of dispersed C4 and observe the relevant patterns. Figure 9 (a) shows an example of stress analysis during the simulation process, (b) shows the stress values on C4, which have been added to the C4 stress values of the same direction. At the mean time, data on the divergent arrangement of C4 in each DOE, such as DOEX-1 and DOEX-2, are also taken into consideration.

From the data in Fig 9(b), it can be seen that C4 has relatively good stress values in DOEX-2-X, and is not affected by the angle of C4. This means that even if C4 is dispersed, the stress in C4 is significantly released. However, for DOEX-1-X, DOEX-3-X, the dispersed C4 arrangement failed to release stress. It can be concluded that the stress of C4 has a strong correlation with the shape of the ellipse. As long as the elliptical shape of C4 matches properly, its stress will be released accordingly. So, the layout of C4 can be considered more from a design perspective, that is, the convenience of layout is the first consideration factor.

CONCLUSION

This paper selects a typical 2.5D structure, arranges three types of chips in the package, and then sets the shapes of the C4 bump. By selecting circles and ellipses of equal area, defining the a/b of ellipses differently, and then conducting simulations to compare the maximum stresses, including those on C4 itself and the interposer.

Through these DOEs, it is possible to provide better design recommendations on how to release stress through C4 bump shape optimization under equal area conditions. From the final result, it can be seen that one of the elliptical C4 (80*105um), regardless of whether the bumps are arranged in the same direction or divergently, has very low C4 stress. It also can be concluded that as long as C4 is set to a specific shape, stress can be effectively released. At the same time, the stress on the interposer was also observed, and except for a corresponding decrease in stress at certain angles, the setting of C4 did not affect the stress on the interposer. Its stress was only related to the von Mises stress of the packaging structure itself, and targeted layout optimization can be carried out to mitigate this stress. Through this study, certain guidance can be provided for design, so as to provide forward-looking design suggestions, the probability of packaging failure caused by stress accumulation can be decreased, and finally the success of product introduction can be achieved.

ACKNOWLEDGMENTS

The author would like to thank the JCET 2.5D team for the modeling, wafer tape-out and assembly work, and thank JCET Design Service BU for 2.5D design instructions.

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