Characterization of Thermally-Enhanced Advanced Electronic Flip Chip CSP Packages

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Abstract

In recent years, high performance and low cost have been the prime motivation for the advanced package developments. The cost-effective flip chip chip-scale package (fcCSP), well stablished in the semiconductor industry, has been extensively utilized in industrial, space, and automotive applications as well as consumer electronics devices. Recently, fcCSP devices have been built using coreless embedded trace substrates (ETSs) that have the advantages of low cost and better electrical performance. However, the standard fcCSP-ETS package is overmolded and has limited capability to handle high performance devices. In this paper, we explore enhancing the thermal performance of advanced fcCSP packages on a two-metal layer coreless ETS, targeting industrial and automotive applications. To this end, three different 13x13 mm^2 package configurations, namely overmolded (baseline), exposed die (lidless), and lidded packages are designed, fabricated, and characterized and their thermal performances are compared under different ambient temperatures. Thermal modeling simulations for all scenarios are carried out in a 3D commercial modeling software and validated against the experimental measurements. From the obtained results, thermal performance of various fcCSP package configurations are compared and the relevant design guidelines are drawn.

Key words

Die junction temperature, exposed die fcCSP, flip chip chip-scale package (fcCSP), lidded fcCSP, overmolded fcCSP, thermal resistance.

I. Introduction

Driven by advanced silicon nodes, the breakthroughs in semiconductor packaging technologies are pushing the boundaries in the post-Moore era to meet the stringent requirements of electronic industry with the smaller form factor, increased functionality, lower cost, and improved reliability, posing new challenges at the device and package levels in terms of finer bump pitches, smaller feature sizes, reduced size, higher I/O counts, better heat dissipation, and innovative failure analysis methods [1]. The thermal management issues on a single die, stemmed from increased processing power and functional density, become complicated with the integration of multiple heterogeneous die or chiplets in a single package, leading to hotspots at varying workloads and use cases [2]. The flip chip BGA (fcBGA) and flip chip CSP (fcCSP) packaging architectures have emerged over traditional wire-bond, QFN or FLGA packaging solutions to address the demanding requirements for the electrical and thermal performances as well as higher I/O densities for AI/HPC applications, consumer electronics, mobile devices, infotainment and ADAS in automotive applications [3, 4]. In several research works [5-9], the thermal management solutions for different fcBGA package configurations, i.e., bare die, lidded and overmolded, with various body sizes and die dimensions, were experimentally characterized and numerically modeled to compare their thermal performances using thermal resistance values obtained between the die junction and a reference point, which can be either the case, board, or ambient, under various power dissipation levels at the room temperature. In addition, the impact of using heatsink on the thermal performance of fcBGA packages were studied in [10, 11]. Detailed numerical modeling of 2.5D and 3D fcBGA package configurations under various power consumptions

and different airflow rates with heatsink was also presented and discussed by Hisada and Yamada [12]. To optimally design a package-on-package (PoP) package for tablet applications from the standpoints of size and material, thermal performance of a PoP package configuration consisting of a bottom fcCSP package and a top thin fine pitch BGA (TFBGA) package, serving as CPU function and DRAM memory, respectively, stacking through solder joints, was computationally modeled and investigated by Chen *et al.* [13]. Further, H.-Y. Zhang *et al.* [14] presented experimental measurements and thermal simulation models of both bare die and overmolded 2.5D packages on through silicon interposer (TSI) under various heat dissipation levels at the room temperature and compared the thermal performance of both packages through thermal resistance measurements from junction to the ambient, from junction to the board, and from junction to top casing. Along with modeling and characterization efforts to achieve accurate measurements and good agreement between simulation and measurement, the effects of overmold thickness and power dissipation from the multichip module on the interposer were also examined. Challenges pertaining to the thermal design and thermal crosstalk between chiplets in a chiplet-based packaging with a 2.5D through-silicon via interposer were also discussed in [15] through conducting detailed thermal modeling simulations to study the effect of the lid, heatsink structure, thermal interface material (TIM) type, bonding approach between chiplets and interposer, and convective heat transfer coefficient above the lid on the thermal management enhancement. Compared to fcBGA packages, fcCSP packages have a smaller package body to silicon size ratio, making heat spreading away from silicon much more challenging [3]. To address these challenges, advanced fcCSP packages are needed to be developed to investigate the thermal enhancement opportunities within the package design for high power applications under harsh operating temperatures. To this end, three different fcCSP package configurations including conventional overmolded one and two thermally-enhanced (TE) designs, namely, lidded and exposed die (lidless), with the body size of 13x13 mm^2 and a thermal die of 8x8 mm^2 size, mounted onto a four-layer JEDEC thermal test PCB [16], are thermally characterized in this paper, for the first time, for automotive and industrial applications. Based on experimental measurements, thermal performance of packages is compared using the junction to ambient thermal resistance value under various operating conditions. Moreover, thermal modeling simulations are conducted in a 3D commercial modeling software to predict the thermal performance of packages, validated against their thermal measurements. The rest of this paper is structured as follows. Section II describes the details of thermal test vehicle (TTV) designs. The experimental setup used for thermal characterization of fcCSP packages along with the obtained results are presented in Section III, followed by package thermal modeling simulations and result discussions, provided in Section IV. Concluding remarks and suggestions for future works are given in Section V.

II. Thermal Test Vehicle Details

A. fcCSP Package Designs

The thermal test vehicle (TTV) consists of three different fcCSP package designs, i.e., overmolded, lidded, and exposed die, as shown in Fig. 1, where the flip chip thermal die with a size of 8x8 mm^2 is bonded to a two-layer ETS through solder bump interconnects and underfill material.

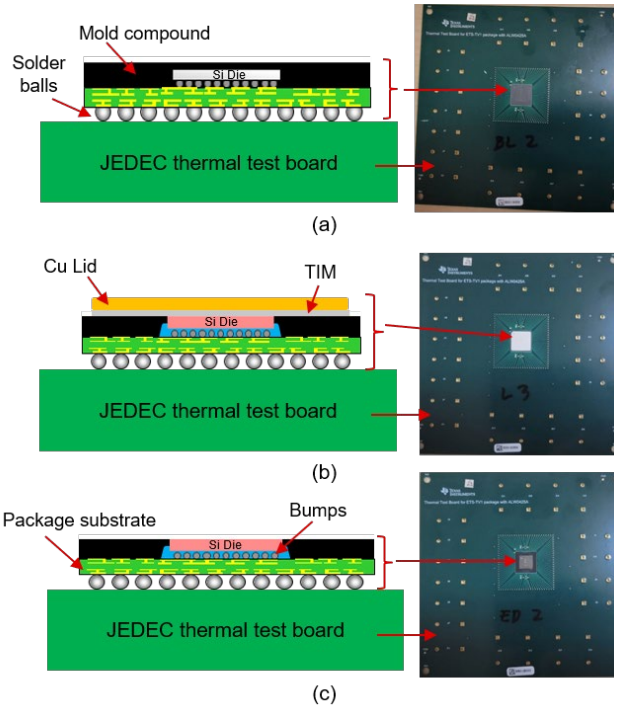

Fig.1. Schematic of different fcCSP package configurations (left) and the board assembly (right). (a) Overmolded, (b) Lidded, (c) Exposed die.

For all package types, the thickness of the mold compound formed on the chip package is 450 µm. In Fig 1(b), a flat copper lid is mounted over the silicon die with a TIM. The package substrate with the body size of 13x13 mm^2 is then assembled onto a four-layer PCB, a 2s2p standard JEDEC thermal test board, as illustrated in Fig. 1(a)-(c).

B. Thermal Die Layout

In design and fabrication of TTV, thermal die has three built-in heating resistors, i.e., R1, R2, and R3, as depicted in Fig. 2, for dissipating the power during package thermal characterization. In the overmolded package, the equivalent DC resistance value for both R2 and R3, serving as localized hotspots beneath the die, is 315 Ω, while that for R1,

providing uniform heating beneath the die surface, is 307 Ω. In this paper, the power dissipation only through R1 is used for thermal measurements of packages. The die junction temperature sensor is located at the top right corner of the die layout, as shown in Fig. 2. The sensor resistance is measured based on four-wire resistance measurement method and its calibration procedure is explained in the following section.

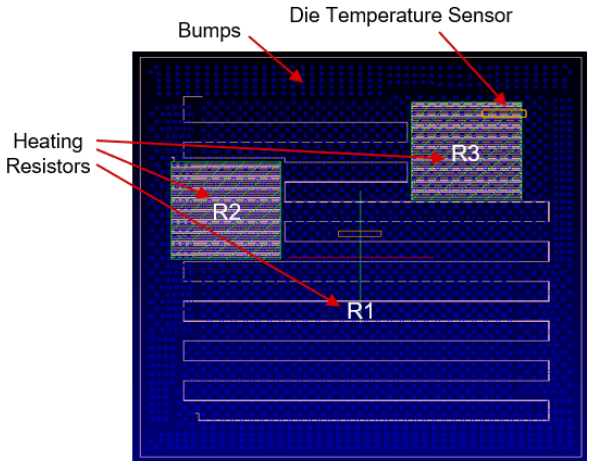

Fig.2. Layout of thermal die with bumps, built-in heating resistors, and die temperature sensor.

III. Thermal Characterization Methodology

To facilitate the electrical measurements during thermal characterization of packages, the required connectors are soldered onto assembled TTVs, as shown in Fig. 3. For each TTV, the temperature sensor of thermal die needs to be calibrated first to obtain the linear temperature-resistance equation of the sensor for extracting the die junction temperature during package thermal measurements. To this end, the sensor calibration is conducted in a temperature-controlled oven at still air condition (natural convection), as shown in Fig. 4. Due to the presence of a fan inside the oven, assembled TTV is placed into a transparent enclosure, made of polycarbonate material. Throughout experimental thermal characterization of packages, temperatures at the board, top case, and ambient need to be measured. The board temperature is captured using a calibrated platinum thin film (PTF) resistance temperature detector (RTD) sensor [17], soldered and attached onto the board surface, as depicted in Fig. 3. The linear performance curve of RTD sensor [17] is validated with the four-wire resistance measurement using a Keysight DMM, shown in Fig. 4. Also, the temperature at the case is measured using a T-type thermocouple (TC) with calibration curve from the manufacturer's datasheet. As shown in Fig. 3, to maintain the fixed position of TC wire during thermal measurements, TC is attached to the top surface of each package type using a high-temperature, high thermally conductive silicone paste, OMEGATHERM 201 [18], and taped using a high-temperature Kapton tape. To determine an appropriate position for ambient temperature measurement using a T-type TC, an initial thermal modeling simulation is conducted in a 3D commercial modeling software. To minimize observed variations within the enclosure, the thermocouple was placed 2.5 in below the test board, as illustrated in Fig. 5.

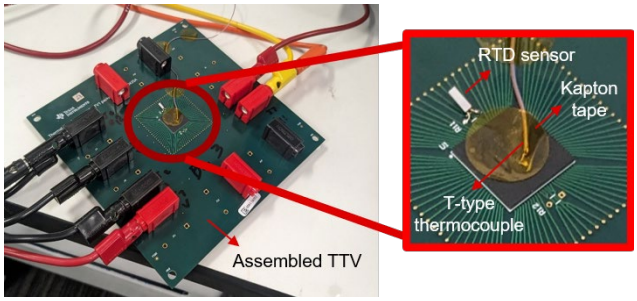

Fig.3. Assembled TTV for electrical and thermal measurements.

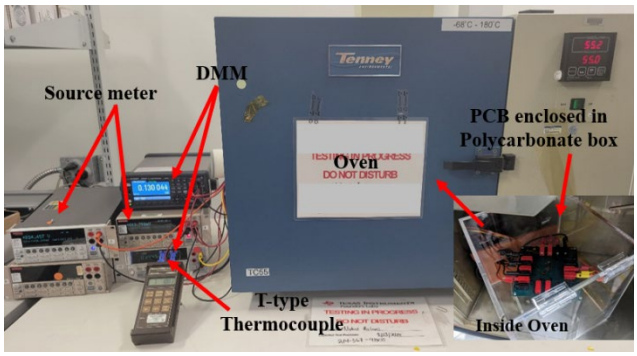

Fig.4. Measurement setup for thermal characterization of packages.

A. Die Temperature Sensor Calibration

Without dissipating any power in the heating resistor R1, the temperature sensor of the thermal die for each package type is calibrated in the air-convection oven at various temperatures. A 30-mA current from the Keithley 2400 sourcemeter is supplied across the die sensor. The case temperature and the voltage drop across the die sensor, measured with the sourcemeter, are captured at each temperature setpoint, after waiting for 150-180 minutes, at the steady state room temperature, to extract the resistance versus temperature relation at the stabilized conditions. Fig. 6 plots the calibration curve of the die sensor for all package types obtained from measurements. As evident in this figure, excellent linearity with R-squared value better than 0.99 is achieved for all three packages. After die sensor calibration, thermal measurements of all package types are performed by injecting various current levels from the sourcemeter to the heating resistor R1 to dissipate different power levels at the thermal die, under various ambient temperatures, namely, room temperature (RT), 55°C and 85°C, enclosed inside the

oven, as shown in Fig. 4.

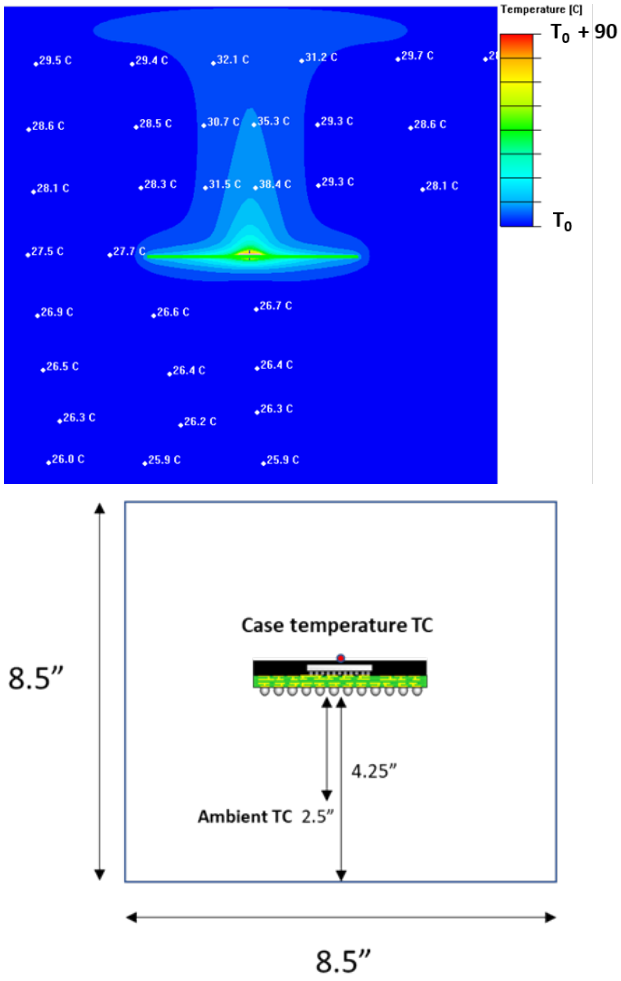

Fig.5. Variations in the air temperature around a board simulated inside a one-feet cubic box (top) and cross-section of experimental box used, showing the best location for ambient TC below the board (bottom).

At each measurement scenario, listed in Table I, temperatures at the board, top case, and ambient are read. Moreover, die junction temperature is extracted based on the four-wire resistance measurement, from sourcemeter reading, and calibration curves plotted in Fig. 6. The power dissipated in R1 at each scenario is calculated from the product of the current level, fed to R1, and the voltage drop reading at R1 using HP DMM, as shown in Fig. 4. Similar to die sensor calibration, all readings are captured after waiting for 150-180 minutes. Afterwards, thermal resistance of each package type from junction to ambient, i.e. R_{ja} (°C/W), at each measurement scenario, is calculated using (1):

$$R_{ja} = \frac{T_j - T_a}{P} \quad (1)$$

Where T_j, T_a, and P are the extracted die junction temperature, measured ambient temperature, and total power dissipation at thermal die, respectively. Thermal measurement results of all fcCSP package types are presented and analyzed in the following section.

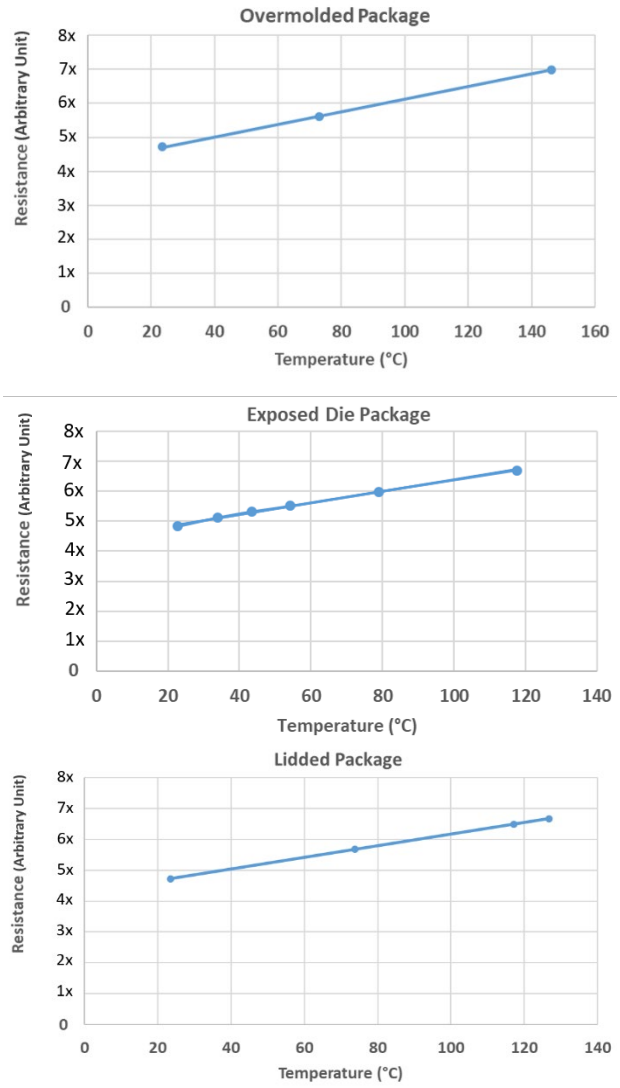

Fig.6. Calibration curves of die temperature sensor for overmolded (top), exposed die (middle), and lidded (bottom) fcCSP packages.

B. Thermal Measurement Results

The measured thermal resistances for R_{ja} and extracted die junction temperatures for all package types at all measurement scenarios are shown in Fig. 7. As it can be seen, lidded package outperforms the other two packages in terms of R_{ja} and T_j and exposed die package exhibit a slightly worse performance than lidded package, but better than overmolded one at all measurement scenarios. Irregular trends at isolated datapoints in R_{ja} can be attributed to the measurement uncertainty sources shown in Fig. 4, including

DMMs, sourcemeters, TC, oven, and wires. According to the analysis conducted in [14], the uncertainty associated with thermal resistance measurements of overmolded and exposed die packages is estimated to be around 5%. While all efforts have been made in this work to capture the measurements as accurate as possible, the impact of uncertainty on measured results is inevitable. One way to reduce this impact is repetition of measurements under the same test condition.

TABLE I. DIFFERENT MEASUREMENT SCENARIOS FOR PACKAGE THERMAL CHARACTERIZATION

Measurement Scenario	Power dissipated in R1 (W)	Ambient Temperature (°C)
1	1x	RT
2	3x	RT
3	5x	RT
4	1x	55
5	3x	55
6	5x	55
7	1x	85
8	3x	85

Overall, in different fcCSP package configuration shown in Fig. 1, the heat dissipation is available in all three heat transfer mechanisms, namely conduction, convection, and radiation. The surface emissivity coefficient involved in thermal radiation, dependent on the surface temperature and surface finish, for the plastic mold compound is higher than that on both silicon and copper surfaces [19]. However, the impact of radiation and natural convection for heat removal in these packages is minimal and majority of the heat is dissipated through conduction from the die to the PCB via package substrate and solder balls. The other path is from the die top to the ambient through mold compound and metal lid. It is worth noting that the thicker die in both lidded and exposed die packages compared to the overmolded one helps achieve lower R_{ja} and T_j values. Also, the metal lid attached with TIM on top of the silicon die in the lidded package provides a better conduction path for heat dissipation from top of the die to the ambient, compared to the exposed die package. Fig. 8 shows the improvements achieved in measured R_{ja} and T_j for the lidded package compared to the overmolded one, where the maximum improvements obtained in R_{ja} and T_j are 16.6% and 6.1%, respectively.

IV. Thermal Modeling Simulations

The 3D finite-element models of package configurations shown in Fig. 1 are built in a 3D commercial modeling software using nominal dimensions of stack-up and thermal conductivity values of materials, and simulated under the measurement scenarios shown in Table I to predict the thermal performance of fcCSP packages.

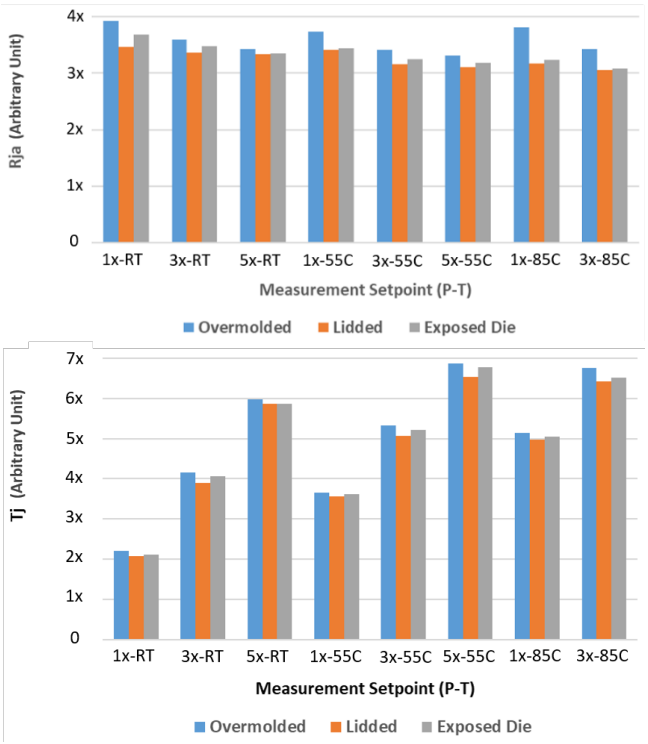

Fig.7. Measured R_{ja} of fcCSP packages (top) and their extracted die junction temperatures (bottom) at all measurement scenarios.

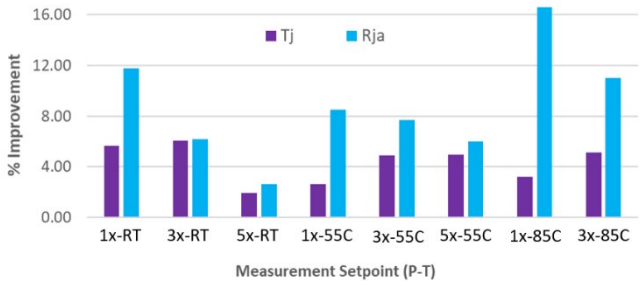

Fig.8. Achieved improvements in measured R_{ja} and T_j for lidded package versus the overmolded one.

The main purpose of this work is to attain a validated thermal model for all package types with minimal deviation to better design them through conducting various parametric studies. To this end, the measurement results, presented in Section III-B, are compared against thermal modeling simulation ones in the following.

A. Thermal Model Validation

Fig. 9 shows the comparison of measured and simulated R_{ja} values for all package types at all measurement scenarios.

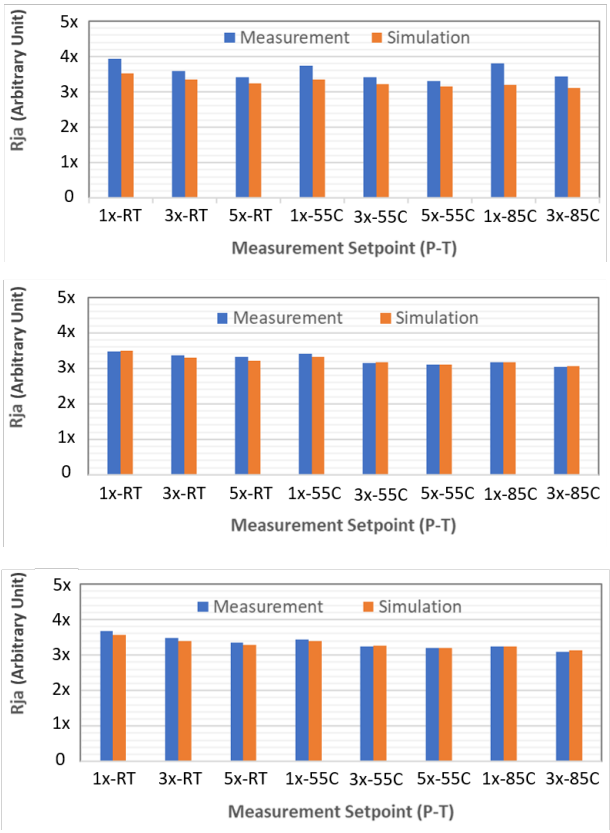

Fig.9. Comparison of measured and simulated R_{ja} at all measurement scenarios for overmolded (top), lidded (middle), exposed die (bottom) fcCSP packages.

As it can be seen, the lidded and exposed die packages exhibit excellent correlation with deviation less than 4% and 3%, respectively. For the overmolded package, the correlation deviation at all measurement cases is less than 11.3% except for the case of 1x-85°C, which is 18.7%. In addition, the measured and simulated T_j values for all package types at all measurement scenarios show a maximum deviation up to 4.86 °C, indicating good agreement between simulated and measured results. Fig. 10 plots the simulated temperature profile at silicon die for the overmolded (baseline) package at the measurement scenario of room temperature and various power dissipation levels. In these figures, along with the location of maximum die temperature, it is obvious that ambient temperature at 3x and 5x W power dissipation levels is higher than that at 1x W, which is due to die heating.

B. Result Discussions

Although thermal simulation models of fcCSP packages are

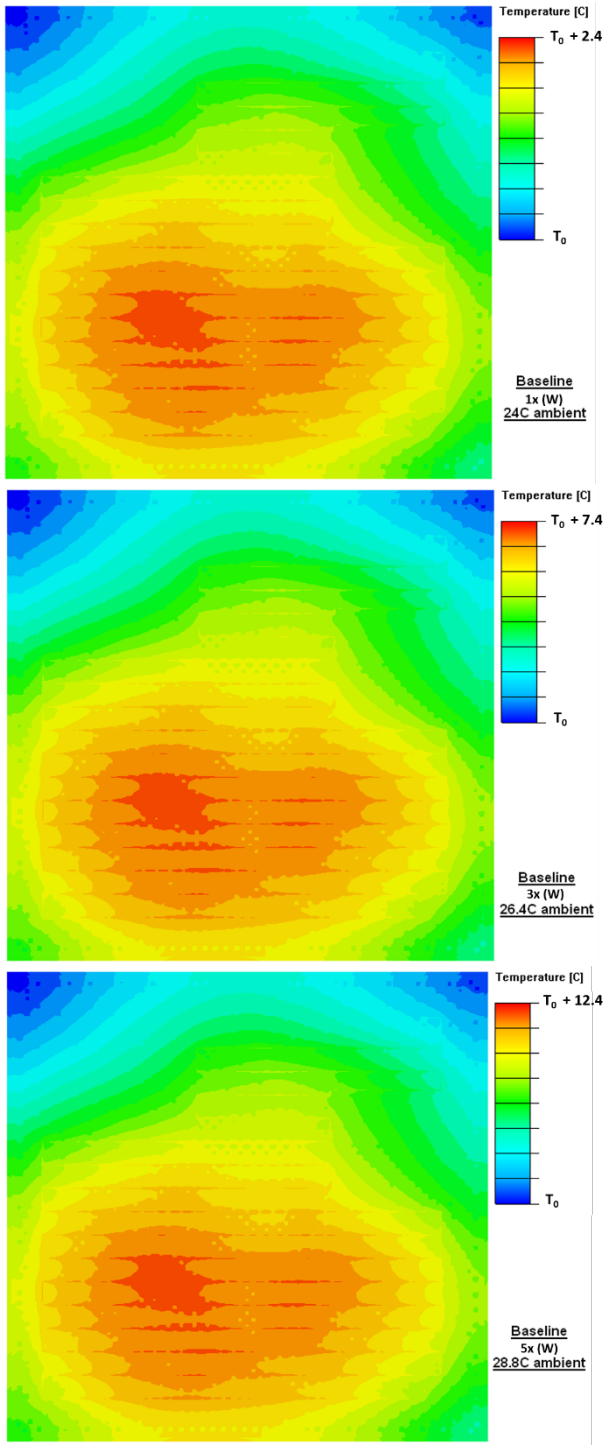

Fig.10. Top view of simulated temperature profile at die for overmolded (baseline) package at room temperature for power dissipation of 1x (top), 3x (middle), and 5x W (bottom).

validated with good agreement and acceptable tolerances, there is still room for improvement especially in overmolded package, to reduce the gap between simulated and measured results. In this regard, the following recommendations are

suggested:

- Modeling the thickness tolerances associated with different parts of stack-up based on the cross-sectioning study of all package types and using the temperature-dependent data for the thermal conductivity of different sections in stack-up into simulation models.
- To monitor the variations of die junction temperature at various ambient temperature and power dissipation levels, its measurement using multiple built-in sensors at different locations would be helpful. This will be considered in future designs of TE-fcCSP packages.
- To capture the inherent uncertainty associated with the experimental measurements and obtain the validated model with the least deviation, thermal characterization of multiple samples of the same package type is also recommended to quantify the thermal performance of packages with more statistical datapoints.
- Using in-plane and out-of-plane thermal conductivity values for each material used in the TTV stack-up into thermal modeling simulations, as implemented in [14], can help reduce the correlation deviation, thereby achieving better validated thermal model.

Based on the obtained results in this work, Table II summarizes the maximum power dissipation limits for each package type at the ambient temperature of 85°C, targeting industrial ($T_j \leq 105\,°C$) and automotive ($T_j \leq 125\,°C$) applications. As evident, the 13-mm size lidded fcCSP package stands out among the rest in terms of lower thermal resistance and higher maximum power dissipation limits for both industrial and automotive applications.

TABLE II. MAXIMUM POWER LIMITS OF 13MM FCCSP PACKAGES AT 85°C AMBIENT TEMPERATURE FOR INDUSTRIAL AND AUTOMOTIVE APPLICATIONS

Package Type	P_{max} (W) for $T_j \leq 105°C$	P_{max} (W) for $T_j \leq 125°C$
Overmolded	1x	1x
Exposed Die	1.12x	1.11x
Lidded	1.22x	1.17x

V. Conclusion

In this paper, thermal performance of different fcCSP package configurations, including traditional overmolded one and two TE designs, i.e., exposed die and lidded packages with 13x13 mm^2 body size and a thermal die of 8x8 mm^2 size, assembled onto a four-layer JEDEC thermal test PCB, is investigated through experimental measurements and numerical simulations. Obtained results in this work provide the design guidelines for the TE-fcCSP packages for automotive and industrial applications as the increased power density with miniaturized packages are highly demanded for such applications. According to the obtained results, lidded package outperforms the other two package types in terms of thermal resistance and die junction temperature. Also, exposed die package indicates a very close performance to the lidded one, and better than overmolded package. Future works include conducting uncertainty analysis for the thermal measurement results of fcCSP packages, and investigating heatsink impact on the thermal performance of different types of packages under various power dissipation levels at the room and elevated ambient temperatures. The thermal simulation modeling results are also compared against the measurement results for all package types using the heatsink to validate the obtained results.

Acknowledgment

The authors would like to thank the technical support from staffs in Founders Lab at Texas Instruments Incorporated for experimental thermal measurements of fcCSP packages.

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