Development of Virtual Material Approach for Modeling Viscoelasticity of Underfill in Flip Chip Packages

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Abstract

This paper presents a virtual material approach to modeling the viscoelastic properties of underfill materials in flip chip packages. The role of underfill is critical, particularly in addressing the challenges associated with cracks in solder bumps in thermal cycles. To ensure the long-term reliability of the semiconductor packages, it is crucial to understand how different underfill properties interact with the package and influence the stress distribution. A fully cured underfill material exhibits viscoelastic behavior. But in many cases, viscoelasticity is neglected and underfill properties are simplified to linear elastic in the finite element analysis (FEA) to save computational cost. For high accuracy numerical predictions, it is indispensable to include a full characterization of viscoelastic properties for underfill in simulation. This work develops a virtual material approach to parameterize the viscoelasticity of underfill materials. A generalized logistic function is adopted for the parameterization of the frequency-dependent modulus in master curve. The master curve is then calibrated in Prony series for numerical implementation. A three-dimensional FEA model is built for evaluating underfill properties in flip chip packages. Fine details such as solder bumps are only included in the sub-modeling for computational efficiency. The FEA model is validated by warpage measurement on a test vehicle in reflow process. Finally, with the developed virtual material approach and the FEA model, various viscoelastic properties of underfill are compared, and the influence on package stress including fillet top stress, die corner stress, and solder bump creep strain is evaluated. The virtual material approach can be particularly useful when dynamic mechanical analysis (DMA) results are not available or in scenarios where obtaining certain properties is challenging. The findings of this study contribute to the development of guidelines for selecting optimal underfill materials, ultimately enhancing the reliability of electronic devices.

Key words

FEA, Flip Chip Packages, Underfill, Viscoelasticity

I. Introduction

Flip chip technology has become a cornerstone of modern microelectronics due to its ability to achieve high-density interconnects and miniaturization. Traditional wire bonding methods limited the number of connections due to space constraints. Flip chip allows for solder bumps to be placed across the entire chip, enabling a significantly higher density of interconnections. By flipping the chip and placing it directly on the substrate, signal paths become shorter, which translates to faster signal transmission and improved electrical performance.

While flip chip technology offers significant advantages, there are challenges associated with its design and manufacturing. The relentless pursuit of smaller chip sizes translates to minuscule solder bumps and tighter spacing, which present difficulties to reliable bump formation and precise alignment [1]. The solder bumps experience significant stress during operation due to thermal cycling and coefficient of thermal expansion (CTE) mismatch between different materials. This stress can lead to premature failure of the solder joints and compromise the package reliability. Underfill materials, introduced between the die and substrate, play a critical role in mitigating these challenges. By encapsulating the solder bumps, underfills provide mechanical support, redistribute stress, and enhance the overall integrity of the flip chip packages. Therefore, choosing the right underfill material with optimal mechanical properties is essential and becomes more challenging with miniaturized packages.

The selection of an appropriate underfill material hinges on its mechanical properties among others, which directly influences the package's performance and reliability. A high modulus allows the underfill to take more load and prevent it from concentrating on solder joints, but it also poses risks due to underfill delamination and cracks [2]. Small CTE is desired and should always be close to that of the die to minimize the stress caused by thermal expansion mismatch. The glass transition temperature (Tg) is rather complex and should be in an appropriate range to protect both solder bumps and low-k material [3]. So far there has been very scattered study about the influence of underfill mechanical properties on package reliability, see [4]-[6].

To simulate the stress distribution within flip chip packages, finite element analysis (FEA) is often utilized. By analyzing the simulation results, engineers can identify areas of high stress concentration and optimize the underfill design, solder joint materials, or overall package geometry to improve reliability and performance. Underfill materials are usually polymer-based and exhibit viscoelastic behavior meaning their properties change depending on both time and temperature [7]. Viscoelastic material models capture behavior such as stress relaxation over time, providing a more realistic picture of stress distribution within the packages. However, due to limited computing resources, viscoelasticity is neglected and simplified material models such as temperature-dependent linear elasticity are often utilized for underfill [8]. By neglecting viscoelasticity, simulations might underestimate the accumulated strain and overestimate the fatigue life of the packages [9].

The aforementioned challenges in underfill properties and material modeling necessitate ongoing research and development of a virtual material approach. This paper utilizes a generalized logistic function to fit the S-shape master curve, and by varying the parameters, one can study different properties such as Tg, instantaneous and long-term modulus without the need to perform dynamic mechanical analysis (DMA) test in real-world. Different properties are studied in a FEA model of flip chip package in thermal cycling, and stresses within packages are compared. The findings of this study contribute to the development of guidelines for selecting optimal underfill materials, ultimately enhancing the reliability of electronic devices.

II. Methodology

A. Generalized Logistic Function

The generalized logistic function is an extension of the logistic or sigmoid functions. Originally it is developed for growth modeling, it allows for more flexible S-shaped curves [10]. The master curve of a viscoelastic material is often S-shaped due to the interplay between the elastic and viscous properties of the material across a range of time or frequency, thus the generalized logistic function is an ideal choice for fitting master curves in log-log space.

The generalized logistic function for master curves has the following form:

$$\log(y) = \log(E_\infty) + \frac{E_0 - \log(E_\infty)}{(1+Qe^{-R\hat{x}})^{1/p}} + \log(b_T) \qquad (1)$$

where E_∞ is the long-term modulus, and E_0 is associated with the instantaneous modulus and has the following form:

$$E_0 = g_1\hat{x} + \log(g_2) \qquad (2)$$

where g_1 and g_2 are the gradient and the asymptote of the instantaneous modulus, respectively. To control the inflection point that has the maximum growth rate, the input variable, namely frequency, is shifted by the following:

$$\hat{x} = \log(x) - (\log(f_c) - \log(a_T)) \qquad (3)$$

where f_c is the frequency associated with inflection point, and a_T and b_T are the horizontal or vertical shift if required, otherwise $a_T = b_T = 1$. The Q in (1) is related to the modulus at inflection point $x = f_c$. The R in (1) is the growth rate; $p > 0$, and it affects near which asymptote maximum growth occurs.

Some examples of master curves by generalized logistic functions are shown in Fig. 1 to demonstrate how to adjust modulus and/or adjust Tg.

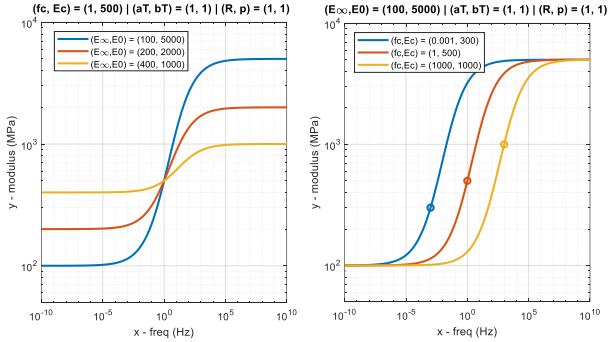

Figure 1. Examples of master curves by generalized logistic function: adjust long-term and/or instantaneous modulus (left) or adjust inflection point for Tg (right).

B. FEA Model

A three-dimensional (3D) finite element model is constructed for flip chip package to study the effect of underfill material properties on the stress distribution. The flip chip package consists of a 20 by 20 mm die which is connected through solder balls to a 35 by 35 mm substrate. The solder bumps are modeled as cylinders rather than spheres because cylinder is preferred for meshing in FEA although sphere is closer to reality. The diameter is 75um,

and the pitch is 150um. The solder bump height is 60um, which is same as underfill thickness. Only one quarter of the test vehicle is modeled to save computational cost, and symmetry boundary conditions are applied.

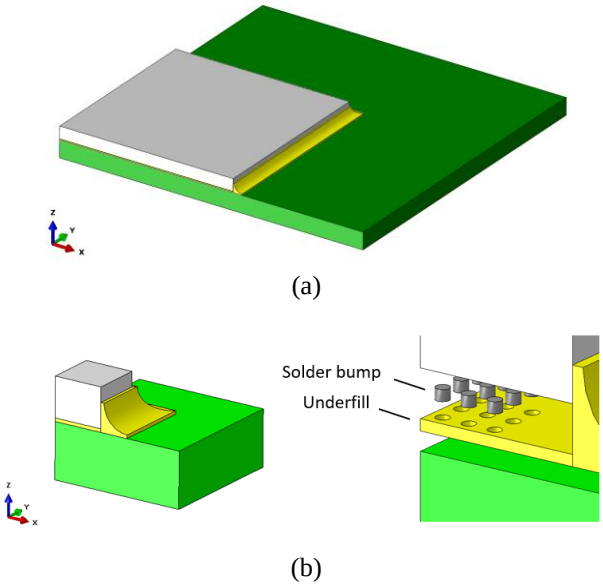

Figure 2. The FEA model for flip chip package: (a) the global model, (b) the local model.

The FEA model consists of a global and local model, as shown in Fig. 2. This sub-modeling technique is used to achieve more accurate results in the die corner by applying a finer mesh locally without having to mesh the entire package with high details. This technique leverages the concept of Saint-Venant Principle, which essentially states that as long as the boundary of a region of interest is far enough away from the area where loads are applied, the effect of those loads can be represented by equivalent forces on the boundary [11]. In the global model, the entire package is discretized with a coarse mesh just to get a general solution for the whole system. The global model does not necessarily have to include details such as solder balls as they do not affect the displacement solution significantly. In the local model, a sub-region at the die corner is modelled with solder balls and refined mesh. The boundary condition of the sub-model inherits the behavior from the global model by enforcing displacement at sub-model boundary to match the results obtained from the global model analysis. Sub-modeling technique optimize computational efficiency and achieve a balance between accuracy and computational cost. ABAQUS standard commercial finite element code is used for FEA in this paper. All components are meshed using quadratic 3D hexagonal elements with a reduced integration formulation (C3D20R). Four elements through thickness are used for underfill to ensure results accuracy. The contact surfaces such as die to underfill and solder, underfill / solder to substrate are tied together using the default tied constraint.

The generalized logistic function described in Section II.A is used for creating virtual master curves for underfill. The master curves are then fitted with Prony series for FEA implementation [12]. A visco-plastic constitutive model, the Anand model is used to describe the creep behavior of the solder balls. The Anand model parameters are adopted from [13] and listed in Table. 1. Elastic material model is used for die and substrate, and their material properties and coefficient of thermal expansion (CTE) are provided in Table. 2.

Table 1. The Anand model parameters for solder.

S1	32.3
Q/R	9320
A	2800
Xi	4
m	0.29
A0	186000
S^	44.67
n	0.012
a	1.72

Table 2. Material properties for die, underfill, substrate

	Die	Underfill	Substrate
Young's modulus (GPa)	169	-	24 @ -55°C 12 @ 250°C
Poisson's ratio ν	0.27	-	0.25
CTE1 (ppm/°C)	2.6	10	12
CTE2 (ppm/°C)	-	50	15.5
Tg (/°C)	-	140	81

III. Results and Discussion

The FEA model is validated by comparing the warpage prediction against experimental results to gain confidence. Warpage is measured in experiment at different temperatures by Akrometrix from -55°C up to 200°C. The stress-free (initial) temperature in simulation is chosen such that it matches with the experiment. The comparison is shown in Fig. 3, and it is a good match.

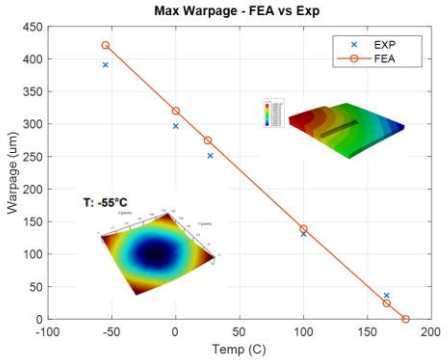

Figure 3. The FEA model validation with experiment.

Three design of experiments (DOE) are conducted to determine the influence of underfill mechanical properties on package stress. Each DOE focuses on a single property of underfill, i.e. the modulus at low temperature, modulus at high temperature and Tg. These are the most common mechanical properties engineers are concerned with for underfill. The DOE matrix is listed in Table 3.

Table 3. DOE matrix for underfill

	#1	#2	#3
DMA (25°C) [GPa]	5-20	10	10
DMA (250°C) [GPa]	0.5	0.2-0.8	0.1
DMA Tg [°C]	140	140	80-140

The temperature profile is one cycle of thermal cycling in Fig. 4. The stress-free temperature is assumed at 135°C. The temperature is reduced from 135°C to -55°C and elevated back to 135°C for one thermal cycling simulation. Examples of fillet top stress, die corner stress and solder bump creep strain are shown in Fig. 5.

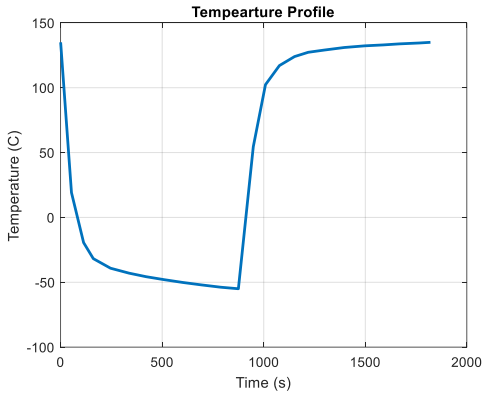

Figure 4. The temperature profile used in FEA simulation.

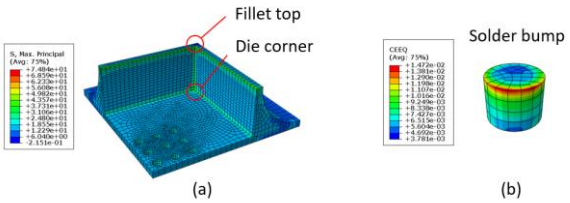

Figure 5. Example of (a) fillet top stress, die corner stress, and (b) solder bump creep strain.

The DOE #1 is to evaluate the influence of modulus at low temperature (or high frequency). The storage modulus and loss modulus are linked and changed simultaneously. The master curves and their distribution in temperature domain via time-temperature superposition (TTS) shift factors are shown in Fig. 6. The TTS shift factors are assumed constant at C1=300, C2=2000.

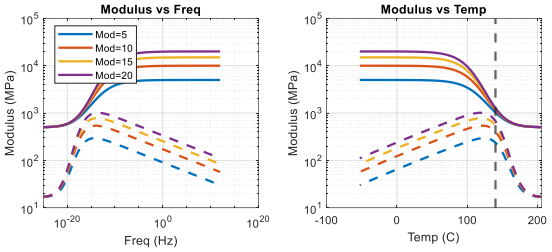

Figure 6. DOE #1 – modulus at low temperature (or high frequency). Solid lines are storage modulus (E'), and dash lines are loss modulus (E").

Simulation results such as warpage, fillet top stress, die corner stress, solder creep strain are shown in Fig. 7. The results at temperature = -55°C are also compared in Table. 4. From the simulation results, one can see that higher modulus leads to higher underfill stress at both fillet top and near die corner. If the fracture toughness does not change, higher the stress means higher the chance of crack and thus fewer thermal cycles of survival before crack. The die corner stress is under compression thus it is less critical than fillet top which is mostly under tension. The solder creep strain goes down as the modulus goes up. Higher modulus of underfill can provide better protection to the solder bumps, thus it will render the package a better electrical reliability.

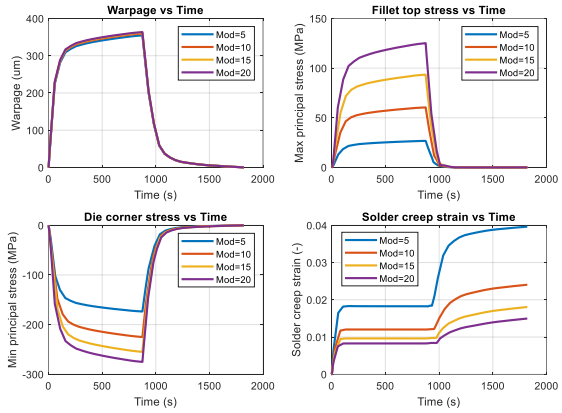

Figure 7. Simulation results for DOE #1.

Table 4. Comparison of results at T=-55°C for DOE #1.

Modulus E' (GPa)	5	10	15	20
Warpage	100%	101%	102%	102%
Fillet top stress	100%	226%	350%	469%
Die corner stress	100%	130%	147%	158%
Solder creep strain	100%	61%	46%	38%

The DOE #2 is to evaluate the influence of modulus at high temperature (or low frequency). The master curves and their distribution in temperature domain via TTS shift factors are shown in Fig. 8.

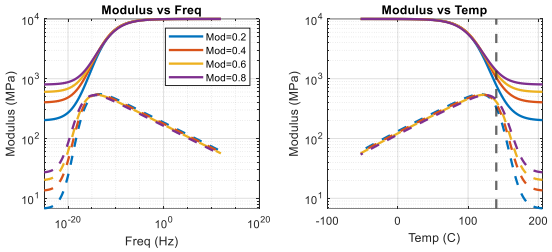

Figure 8. DOE #2 – modulus at high temperature (or low frequency). Solid lines are storage modulus (E'), and dash lines are loss modulus (E'').

Simulation results are shown in Fig. 9, and stresses at temperature = -55°C are reported in Table. 5. From simulation results, one can see that the impact on package stress is very minor. This is because the modulus at high temperature is beyond the temperature range of thermal cycling, thus for underfill that has Tg close to 140°C particularly, changing modulus at high temperatures will only affect the stress marginally.

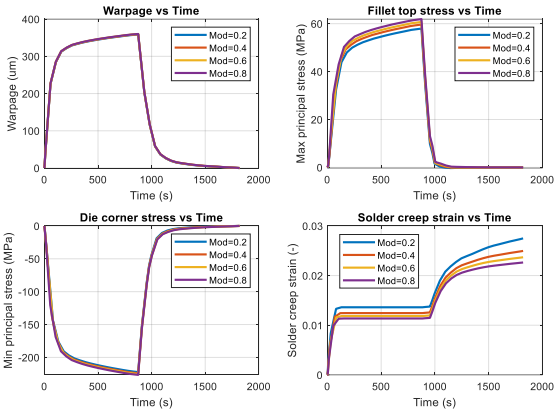

Figure 9. Simulation results for DOE #2.

Table 5. Comparison of results at T=-55°C for DOE #2

Modulus E' (GPa)	0.2	0.4	0.6	0.8
Warpage	100%	100%	100%	100%
Fillet top stress	100%	103%	105%	107%
Die corner stress	100%	101%	101%	102%
Solder creep strain	100%	91%	86%	82%

The DOE #3 is to evaluate the influence of Tg. The master curves and their distribution in temperature domain via TTS shift factors are shown in Fig. 10.

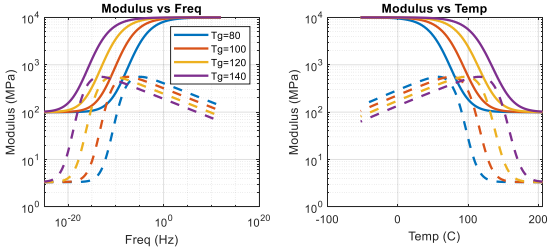

Figure 10. DOE #3 – Tg. Solid lines are storage modulus (E'), and dash lines are loss modulus (E'').

Underfill material typically behave glassy below Tg and rubbery above Tg, so changing Tg will change the stress distribution for temperature near Tg. From the simulation results in Fig. 11 and Table. 6, one can see that increasing Tg will increase the fillet top stress but does not affect the die corner stress. The solder creep strain is reduced significantly as the Tg goes up. This indicates that increasing Tg can provide a better protection to solder bumps, and only increases the fillet top stress moderately. One can combine the findings in this study to find the most optimum selection of Tg and modulus for underfill.

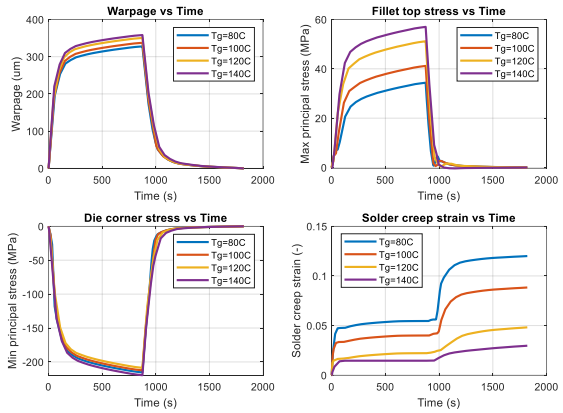

Figure 11. Simulation results for DOE #3.

Table 6. Comparison of results at T=-55°C for DOE #3

Tg (°C)	80	100	120	140
Warpage	100%	102%	107%	109%
Fillet top stress	100%	120%	149%	166%
Die corner stress	100%	99%	97%	102%
Solder creep strain	100%	73%	40%	25%

IV. Conclusion

In this paper, a virtual material modeling approach is developed based on the generalized logistic function. Such virtual approach is utilized in modeling the viscoelastic properties of underfill in flip chip packages. The virtual material approach can provide an estimation to the material characterization when the DMA results are not available.

The impact of different viscoelastic properties of underfill on flip chip package is evaluated in FEA. The simulation results reveal that both modulus at low temperature and Tg play an important role in package stress such as fillet top, and also the creep damage to solder bumps. This study provides a design basis or contribute to selection guide for choosing the right properties for underfill to achieve the optimum overall reliability performance of the package.

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