# Ultra-High density RDL on Glass Core Substrate for Heterogenous Integration

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## Abstract

As the industry moves toward high-performance computing (HPC) for huge data transmission with low power consumption. The requirements for advanced package (PKG) structures have become more challenging. The major engineering requirements for HPC application are high-density, high-speed data transmission, low loss, precision manufacturing with low-cost process. High pin counts need large area package with high mechanical stability and low warpage. The demand for high density and high-speed data transmission becomes strong need for leading edge semiconductor packaging. 2.5D and 3D heterogenous package realize this solution. On the 2.5D heterogenous package structure, high interconnect density with fine line wiring layers providing high speed transmission is required to-connect CPU chips or chiplet arrays and HBM chip stacks. Silicon interposers with through silicon vias (TSVs) have scaled to meet this demand, but face three major barriers: high electrical loss, package size and cost. On the other hand, glass has many properties that make it an ideal core material for advanced substrates such as ultra-low loss tangent, adjustable thermal expansion (CTE), mechanical stability and manufacturability with large panel formats.

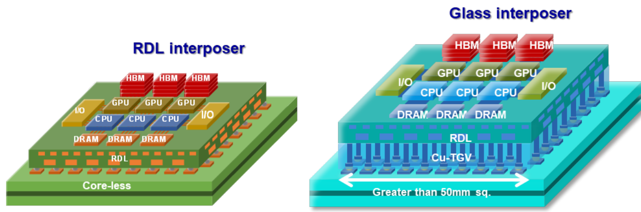
This paper presents the demonstration of Glass core substrate with fine line redistribution layers (RDL). Glass core substrate with fine pitch metalized through glass vias (TGV) and fabricate RDL with low loss dielectrics. In case of Glass core substrate, three TGV copper metalized processes were compared for process capability, -reliability and high-speed transmission characteristics. Copper metallization provides low resistance, high transmission rate and high-power density. The reliability test results show stable resistance data because of combination of double-sided polymer dielectrics. The double-sided polymer dielectrics providing stress buffer for glass and copper CTE differences. TGVs filled with Cu by three methods were demonstrated with large panel size format max 550x650mm.The ultra-high density RDL process using non-organic protective layer fabricated on the glass substrate. High aspect ratio Cu traces enable to minimum 3um pitch, high transmission rate and high reliability. We also compare high speed transmission characteristics with TGV and transmission trace with multi-layer RDL on panel level format. Finally, we compare the transmission characteristics using eye diagram for heterogenous integration application.

## Key words
HPC, high-speed data transmission, high reliability, fine line RDL, glass core substrate, large panel size

## I. Introduction

In recent years, as data centers have grown larger and the utilization of AI has advanced, there is increasing expectation for semiconductor products that can handle increasing data transmission and high-speed signal transmission. Thus, new structures such as chiplets and heterogeneous integration packaging have been proposed. On the other hand, with the miniaturization, lightweight, and increased functionality of electronic devices, there is a growing demand for high density and high integration. As the industry increasingly adopts HPC for large-scale data transmission while minimizing power consumption, the demands on package structures have become more complex and challenging. The major engineering requirements for HPC application are high-density, high speed data transmission, low loss, precision manufacturing and low cost. In response to these challenges, we have developed low-loss RDL and glass core technologies. Fig. 1 shows images and characteristics of RDL interposer and glass interposer (GIP)

as examples of ultra high-density substrates.




| Products | RDL interposer | Glass interposer |
|---|---|---|
| Applications | General purpose<br>・PC<br>・Mobile<br>・Switching, etc. | High-performance<br>・A.I. computing<br>・Graphics<br>・Game, etc. |
| Advantage | Cost effective | Larger size ( >50mm sq.) |

Fig. 1 Ultra high-density substrate

## II. RDL Interposers

### *A. Concept of development*

Fig. 2 shows target specification and feature of RDL Interposer for high performance computing.

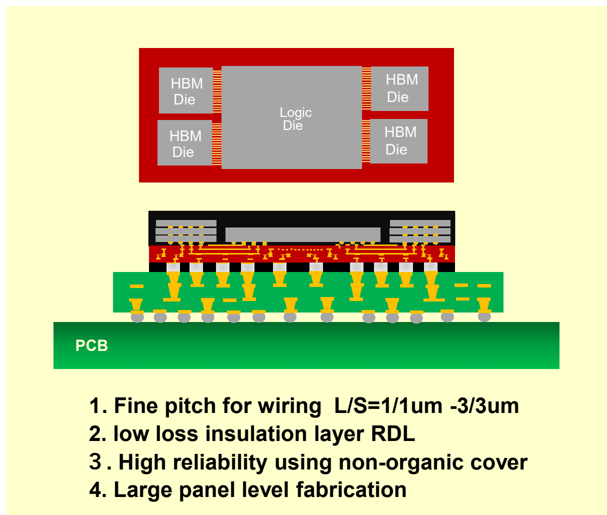



Fig. 2 Schematic structure and feature of RDL Interposer

### *B. Demonstration of fabrication with 300mmx400mm panel*

Fig. 3 shows process flow of RDL layers. At first, seed layer formation on lower steps on the insulation layer. (a) Secondary, photo resist formation and open the wiring area with developer. Thirdly, electro-plating applied open area of photo resist. (c) After resist stripped(d), seed layer metal was etched. (e) And then inorganic layer deposit on the Cu trace(f). It is original process for high reliability of the RDL layer. After insulation layer formation, inorganic layer was dry etched through opening area of insulation layer. Finally micro bumps formation on the top layer.[1] Fig. 4 shows demonstration result of fine wiring layers on 300x400mm Glass panel format. 2-µm pitch Cu trace fabricated on the large glass.

High aspect ratio wiring obtained electro-plating with semi-additive process. Fig. 5(a) shows high aspect ratio wiring. Aspect ratio of wiring was about 3 on L/S=1/1µm.

Fig. 5(b) show L/S=1/1µm trace with protective layer. Inorganic layers highly enhance reliability on the narrow pitch under 2µm. [2)3)]

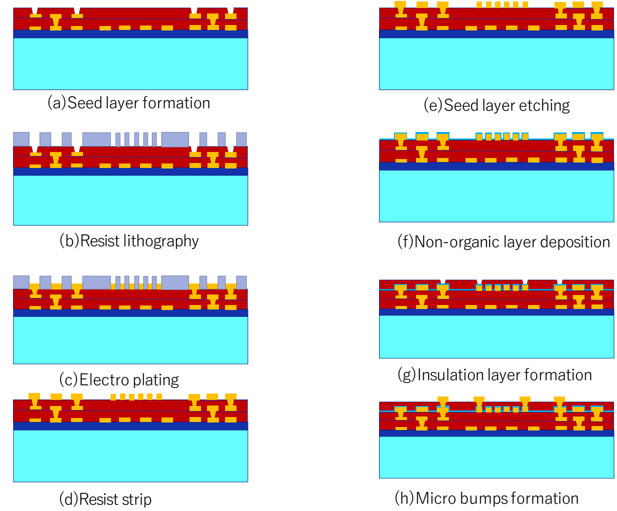



Fig. 3 Process flow of RDL layers.

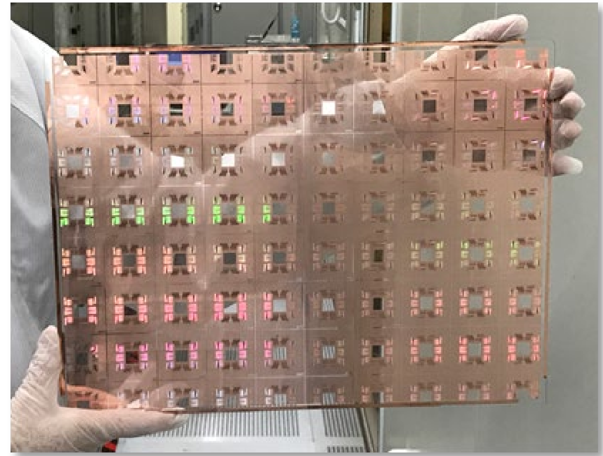
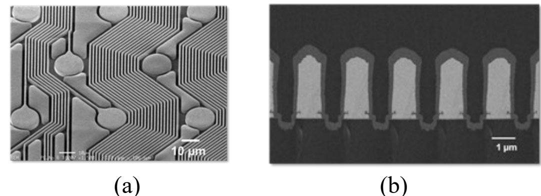


Fig. 4 Fine wiring layers on 300x400mm Glass panel format.




(a) (b)

Fig. 5 (a) L/S=1/1µm trace, (b)trace profile with protective layer.

Insulation layer materials is important role of RDL properties. Insulation layer materials needed small size micro via, Low stress for reduction warping and low loss tangent for high-speed signal transmission.

Fig. 6 shows result of via diameter with positive tone photo imageable dielectric material (PID). Via shapes is taper forms, minimum diameter was top 5.7µm and bottom 3.0µm.

Fig.7 shows multi-layer stack of RDL. 5metal RDL layer include fine pitch layer demonstrated stacking on carrier glass. Fine wiring layer fabricated on flat intermediate RDL surface.

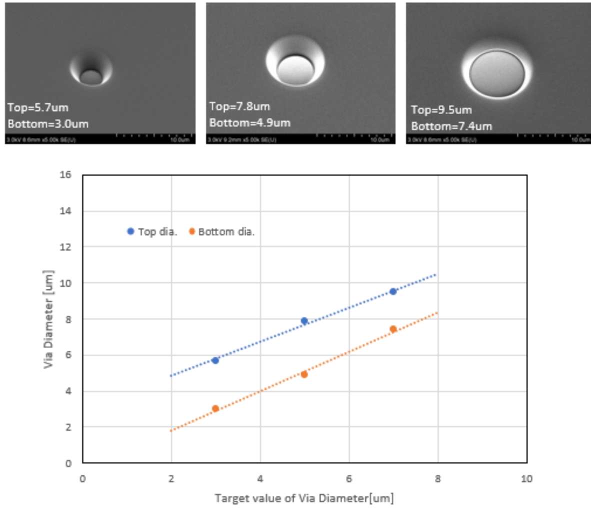



Fig. 6 Via diameter of insulation materials PID.

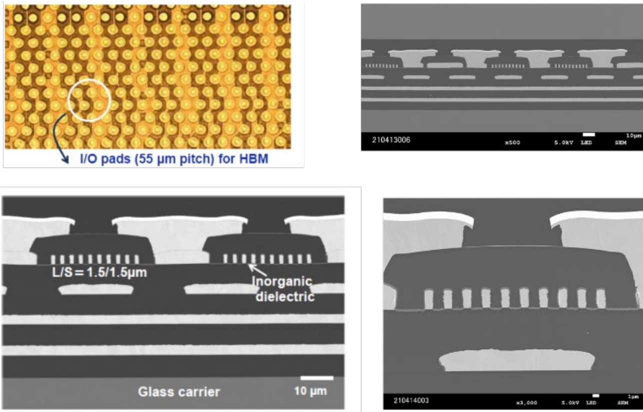



Fig. 7 Profile of 5metal layer stack.

We demonstrate coplanar waveguide (CPW) transmission line with fine wiring layers. Test elementary group (TEG) fabricated on core glass to measure high frequency characteristics. Fig.8 shows real measurement result of fine wiring consist of CPW structure with 5mm length. Insertion loss has large value with fine wiring pitch due to the conductive loss will be large. As the L/S becomes finer than 2/2µm, there is a tendency for the Cross-sectional Area to decrease, which results in an increase in insertion loss and deterioration of Eye Diagram (Fig.9). Therefore, it is crucial to focus on the high-aspect-ratio formation of the Transmission Line.

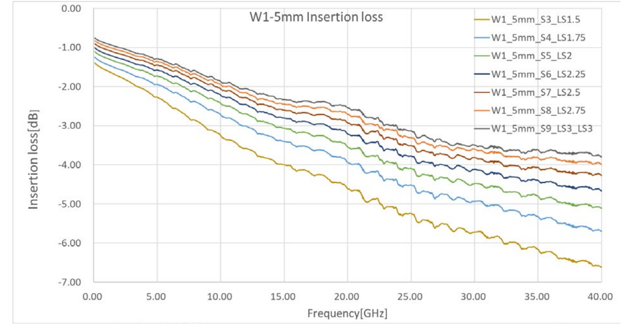



Fig. 8 Measurement result of fine wiring consist with CPW structure.

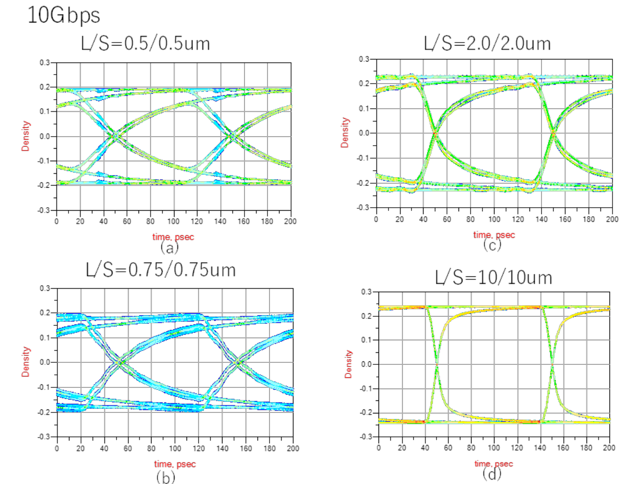



Fig.9 Eye diagram simulation result of CPW on RDL.

### C. *Examining the Applicability for UCIe 1.0 specification*

The specification opened in UCIe 1.0 is expected to provide standardization of chiplet-based communication for advanced packages. In the specification of advanced packaging, the required processing speed is ranged from 4 to 32 Gbps/line, which corresponds to the bandwidth density of from 1.0 to 10.5 Tbs/mm. On the basis of the specification of the UCIe1.0, we set signal line length between chiplets to 1.0 mm in the I/O sections (1.0 mm x 2) and 0.4 mm in the middle section, so the total length was 2.4 mm (Fig.10). This is 20% longer that of the required signal line length/channel length between chiplets (2.0 mm) in the specification of UCIe 1.0.

Cross-sectional dimensions used in the simulation for the topologies of GSG, SSG and SSS are shown Fig. 11 (a), (b) and (c). The wave form for the topology of SSG did not cross the keep-out area, indicating a shield effect created by the

ground line neighboring the signal line reduced the crosstalk (Fig. 12 (b)). The wave form for the topology of GSG was away from the keep-out area enough (Fig. 12 (a)). Both side ground lines neighboring the signal line greatly removed electromagnetic force generated around the signal lines. Both topologies of GSG and SSG met the specification of UCIe 1.0 at 32 Gbps.[4)]

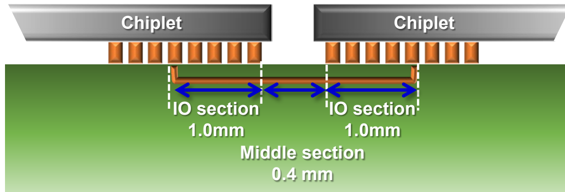



Fig. 10 Length of signal line consisting of both IO sections and middle section for specification of UCIe 1.0.

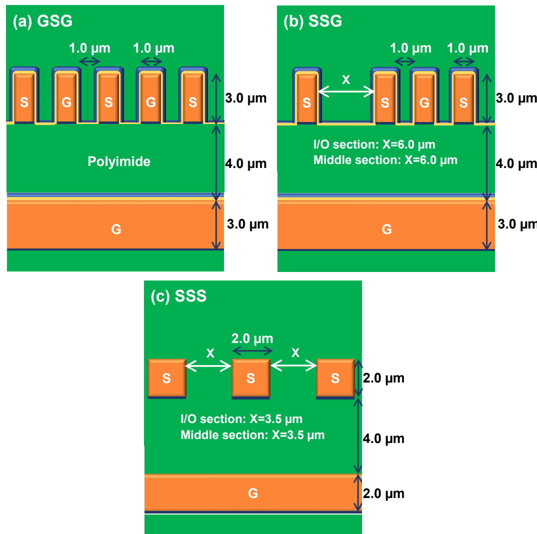



Fig. 11 Cross-sectional dimension of signal line for topologies of GSG (a), SSG (b) and SSS (C).

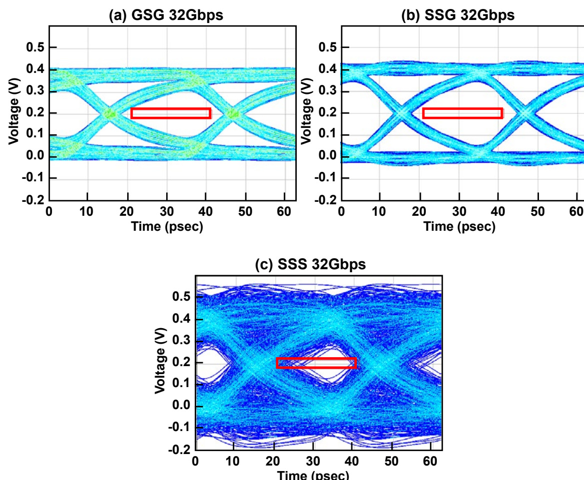



Fig. 12 Simulated eye diagram of topology GSG (a), SSG (b) and SSS (c) at 32 Gbps in specification of UCIe 1.0.

## III. Glass Interposers

### *A. Concept of development*

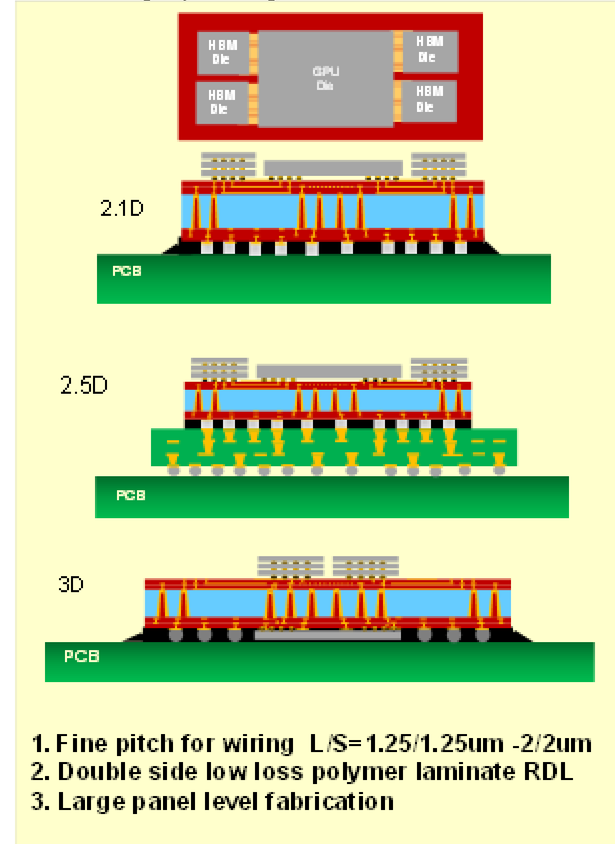



Fig. 13 Schematic structure of Glass based Interposer.

Fig. 13 shows target specification and feature of glass Interposer for high performance computing. Fig. 14 shows process flow of Glass interposer. First, TGVs of 80µm in diameter and 200µm in pitch were formed on 400µm thick alkali-free glass. Ti/Cu seed layer deposition. Then the via was deposited with Cu by conformal electroplating. Thick dielectric polymer layer was laminated on the wafer as RDL passivation film. Redistribution lines were patterned with photo resist. Cu RDL line of 5 µm thickness was deposited by Cu electroplating followed by photo resist and Cu seed layer removal.

The conformal plating method has great advantage of process time of plating. After depositing the seed layer, plasma ashing was done from both sides of the panel to improve the hydrophilic property of the surface of Cu seed layer. Fig.15 demonstrates a 300x400mm panel with conformal TGV. Fig.16 showcases a filled via with dimensions of 510x515 mm, while Fig. 17 exhibits a partially filled Cu method on a 300x400mm panel.

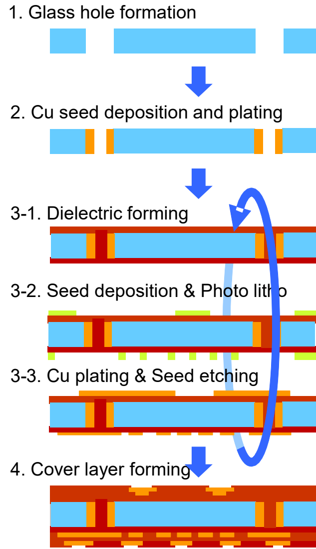



Fig. 14 process flow of Glass interposer

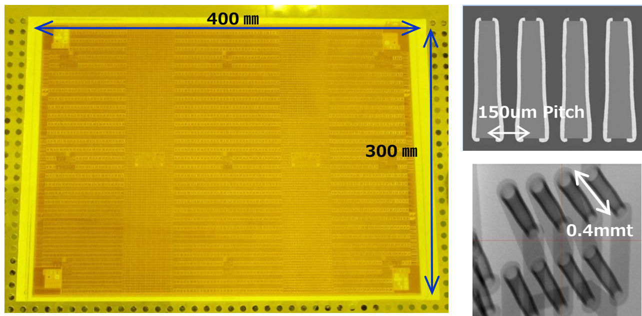



Fig.15 Conformal TGV Cu method

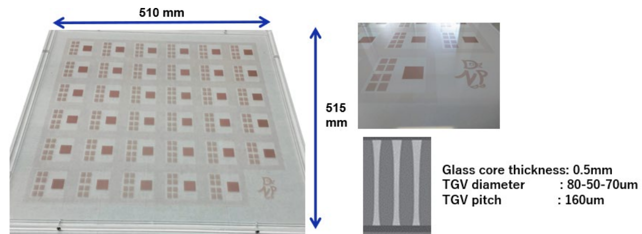



Fig.16 TGV Filled with Cu method.

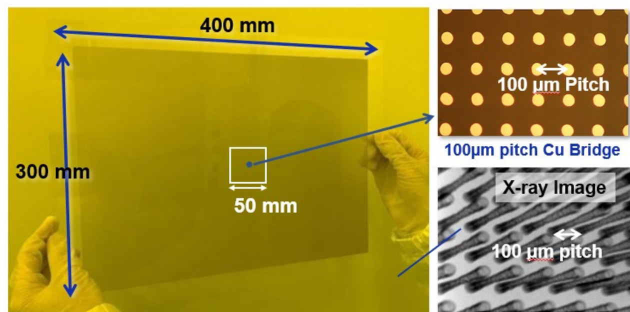



Fig.17 Partially filled with Cu method

*B. High frequency characteristics*

High frequency electrical characteristics of interposers were evaluated with three TGV type metalized methods. We have selected a combination of a transmission wiring with coplanar waveguide structure (CPW) and TGV to study the influence of TGV on high frequency region. The measurement of TGV only itself is difficult because measurement TEG needs outer pad for probing. It is not ignored influence of the outer pad. We choice the method compared CPW and CPW+TGV show in Fig. 18. The data are corrected from TEG which have Line and space are 30μm and 15μm for impedance 50ohm matching. Length of CPW is 10mm.

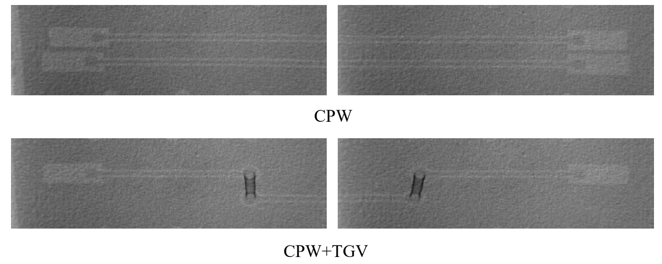



Fig. 18 CPW transmission line TEG

Double side metal layer test vehicle containing CPW with TGV transmission were designed. Electrical measurement was performed after short open load through (SOLT) calibration and the CPW transmission characterized up to 40GHz. Fig.19(a) shows test vehicle containing CPW with filled types of metalized method. Fig.19(b) shows test vehicle containing CPW with conformal TGV metalized method. The network analyzer S-parameter measurements indicate that CPW has lower loss than CPW+TGV in transmission shown in Fig.19.

Both types of metalized TGV have excellent transmission. Filled via has slightly lower loss than Conformal via in transmission shown in Fig.19.

It causes reflection on the joint with trace and TGV. Highly bulk resistance of TGV resulted in an insertion loss less than -0.5dB at 30GHz. It causes reflection on the joint with trace and TGV.

The new types of partial filling plating method applied for measurement. Partial filling types have great advantage of fine pitch arrangement due to half diameter of conventional ones. [5] Fig.20 shows test vehicle containing CPW with partial filling types of metalized method using small diameter TGV. Fig. 21 shows measurement result CPW and CPW with TGV. The differential of S21 summarized in Table 1. Three types of TGV were all very low loss. Specifically, the filling type exhibited the lowest loss, with a tendency for TGVs with a larger filled portion to have lower insertion losses.

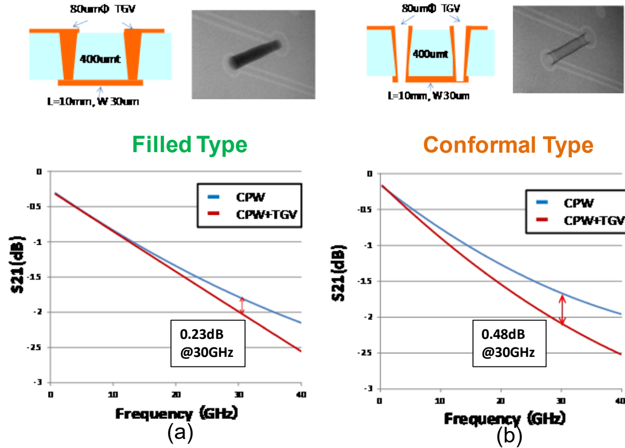



Fig. 19 Co-planar waveguide (CPW) test vehicle

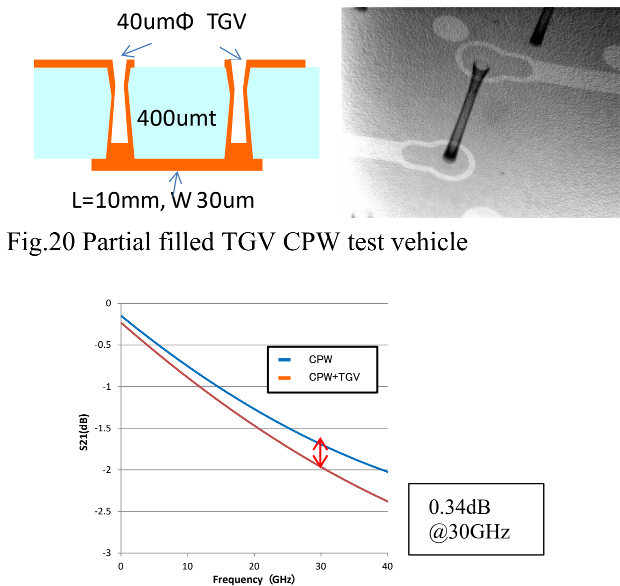



Fig.20 Partial filled TGV CPW test vehicle

Fig.21 Measurement result of partial filling TGV

Table 1 Insertion loss of three types of TGV at 30 GHz

| Types of TGV plating method | Difference of S21 |
|---|---|
| Filled type | 0.23 @30GHz |
| Conformal type | 0.48 @30GHz |
| Half fill type | 0.34 @30GHz |

## C. *Reliability of glass interposer*

We conducted reliability tests on each of the three types of TGV. Fig.22 shows result of Thermal cycle test (TCT) for conformal type. Test condition is temperature cycles from -40°C to 85°C with a dwell time of 30 min at each temperature. No significant resistance changes were observed during the test, even after conducting 1000 cycles.

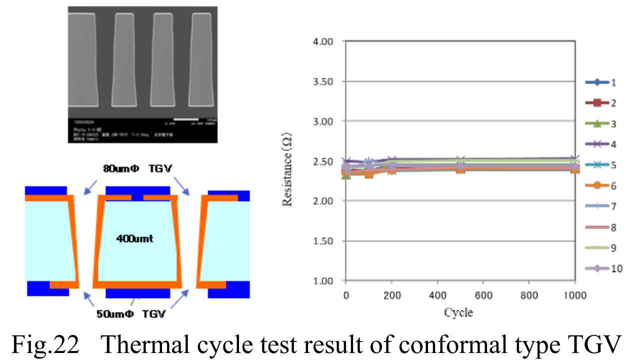



Fig.22 Thermal cycle test result of conformal type TGV

Next, Figure 23 shows the results of filled type TCT. The conditions for this TCT were a cycle of -55℃ to 150℃. As with the conformal type, no significant resistance change was observed even after 1000 cycles.

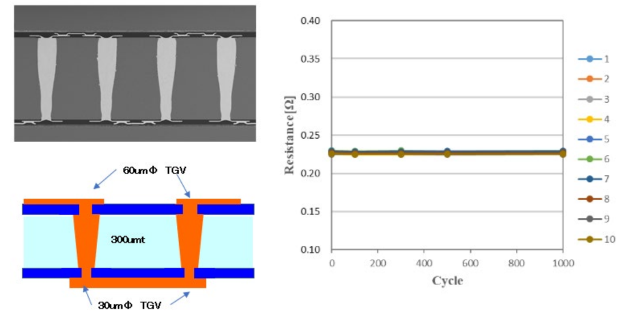



Fig.23 Thermal cycle test result of Filled type TGV

Finally, Fig. 24 shows the variation in electrical resistance of a partially filled TGV when subjected to thermal cycling from -45℃ to +120℃. The plotted data were converted into the electrical resistance of partially filled TGV from a TGV daisy chain consisting of 1000 TGVs. The electrical resistance was unchanged after 1000 cycles. This shows that the structure of the partially filled TGV effectively reduces the residual stress caused by the CTE (coefficient of thermal expansion) mismatch between glass and Cu. [5)]

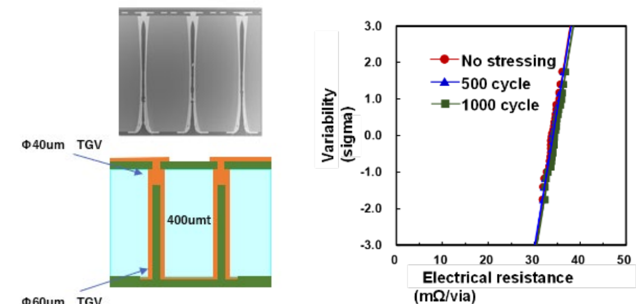



Fig.24 Change in electrical resistance of partially filled TGV stressed by thermal cycling test.

*D. Large panel level fabrication*

We present the results of our maximum size demonstration. This glass core size is 550X650mm, and the TGV are fully filled with Cu. We have successfully fabricated it without encountering any issues in the overall dimensions of 550×650mm.

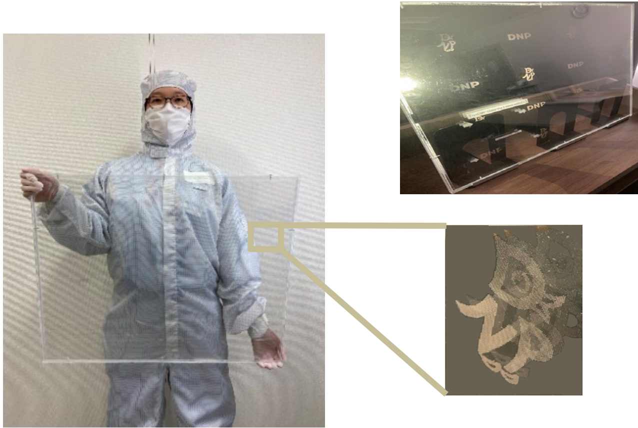


Fig.25 550X650mm glass core panels

## V. Conclusion

To achieve Ultra-High density RDL, it is necessary to miniaturize the wiring (L/S=1/1) and the vias (Bottom diameter 3um). We conducted the necessary verification for Ultra-High density RDL on a panel size of 300×400 ㎜. We also demonstrated the multilayering and conducted a demonstration of a 5-layer RDL. Additionally, although not mentioned in this paper, we announced that high reliability can be achieved by protecting the fine wiring with inorganic dielectric. [6] The measurement results of the insertion loss (S21) of the fine wiring and the simulation results of the eye pattern show that as miniaturization progresses, the high-frequency characteristics deteriorate. To solve this issue, it is necessary to increase the thickness of the wiring to reduce the resistance of the conductor. Therefore, we have achieved a high aspect ratio (A/R=3) by adopting a semi-additive process (SAP) in the fine wiring section. By adopting a high aspect ratio (A/R=3) and applying GSG and SSG structures, it was found that it is possible to meet the UCI E1.0 standard (32 Gbps/line).

As for TGV, we have developed three types (conformal, field, partial filled) and have revealed that each type achieves low insertion loss (good high-frequency characteristics) based on the measured results. Furthermore, by conducting Thermal Cycling Test for the three types, high reliability has also been demonstrated.

TGV has also been developed on a panel scale, and the highest record for Cu filled TGV in terms of panel size is 550 ×650 ㎜.

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