Fabrication and Passive Assembly of Broadband Evanescent Couplers for Sustainable Pbps Co-Packaged Optics

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Abstract
A passively assembled chip-to-package substrate evanescent coupler between silicon nitride and silicon was experimentally demonstrated across the 1480-1640 nm wavelength regime with a 0.39 ± 1.06 dB coupling loss at 1550 nm, a 160 nm 1-dB wavelength tolerance (1480-1640 nm), and a 1-dB lateral alignment tolerance of ± 1.56 μm. The thermal stability was evaluated from 23-60°C with average coupling loss and alignment tolerance varying by less than ± 0.35 dB and ± 30 nm, respectively. The repeatability of the packaging process flow was also evaluated by measuring coupler performance across four separately packaged systems, with a total range of 1.5 dB for coupling loss observed. Results show the viability of this coupler to help achieve Pbps co-packaged optics switch performance by eliminating active fiber-to-chip alignment and scaling down optical input/output pitch at the die level.

Key words
silicon photonics, co-packaged optics, passive assembly, evanescent coupling

I. Introduction
Historically, data center top of rack (ToR) switch packages have doubled total bandwidth capacity every two years to meet demand, with commercial packages reaching 51.2 Tbps using 106.25 Gbps per lane [1]. Standardization of 200 Gbps per lane is already underway [2]. However, the power consumed by board level copper traces and the limited pitch of pluggable transceivers has forced a transition to co-packaged optics (CPO) [3]. Scaling using CPO has challenges also, such as the active alignment of single mode fiber (SMF) arrays to silicon photonic integrated circuits (PICs), a problem underscored by the fact that photonic packaging, assembly, and testing occupies 70-80% of the total cost of PIC manufacturing [4–7]. Looking ahead, greater than 10^3 SMFs will be required to scale to the Pbps bandwidth capacities required by 2035 according to current trends [8]. Meeting these fiber count benchmarks is also made more difficult because standard telecom SMF arrays have minimum pitches of 127 μm, meaning a density of only 8 fibers/mm is possible. A sustainable solution is to use fine pitch waveguide-to-waveguide couplers to connect die to package substrates and substrates to boards, enabling optical fan-out. Such an architecture would permit massive numbers of parallel optical connections and passive flip-chip assembly using automated pick-and-place technology. To this end, the substrate-to-die evanescent coupler design outlined in [9] was fabricated, packaged, and tested to demonstrate feasibility.

II. Device Fabrication, Die Packaging, and Testing
A. Silicon-on-insulator substrates and silicon nitride-on-fused silica die for chip-to-chip coupling
The proposed coupler, shown in the upper callout of Fig. 1(a) included two overlapping, double tapers, and was distinct from other evanescent couplers in two ways: 1) it was an inter-chip coupler as opposed to an intra-chip coupler and 2) it used a fused silica package substrate with 220 nm silicon nitride (Si_3N_4) waveguides. The Si_3N_4-on-glass substrate maintained CMOS compatibility, lowered cost, had the prospect of low propagation losses, and increased minimum feature sizes to > 200 nm due to a lower index

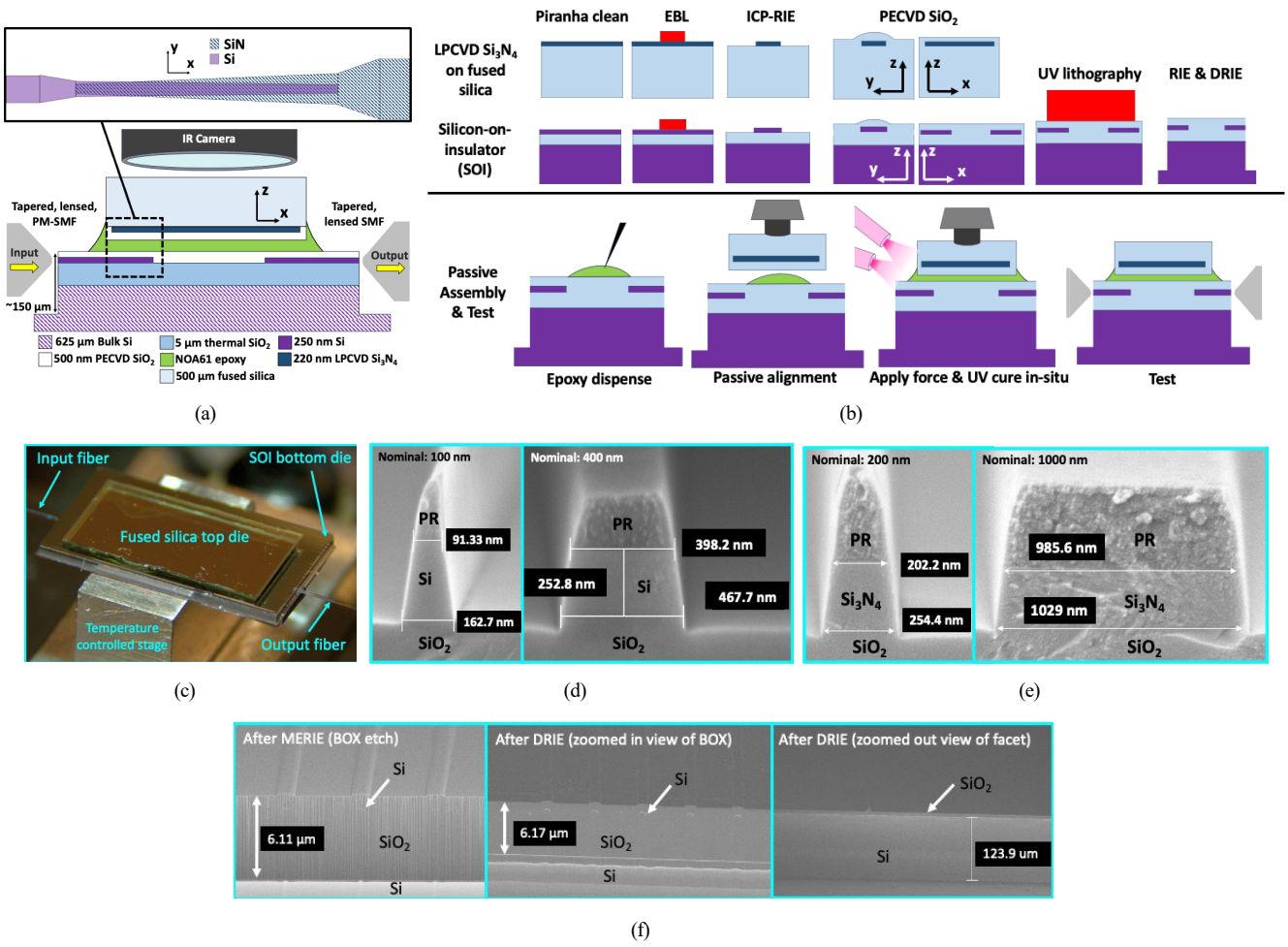
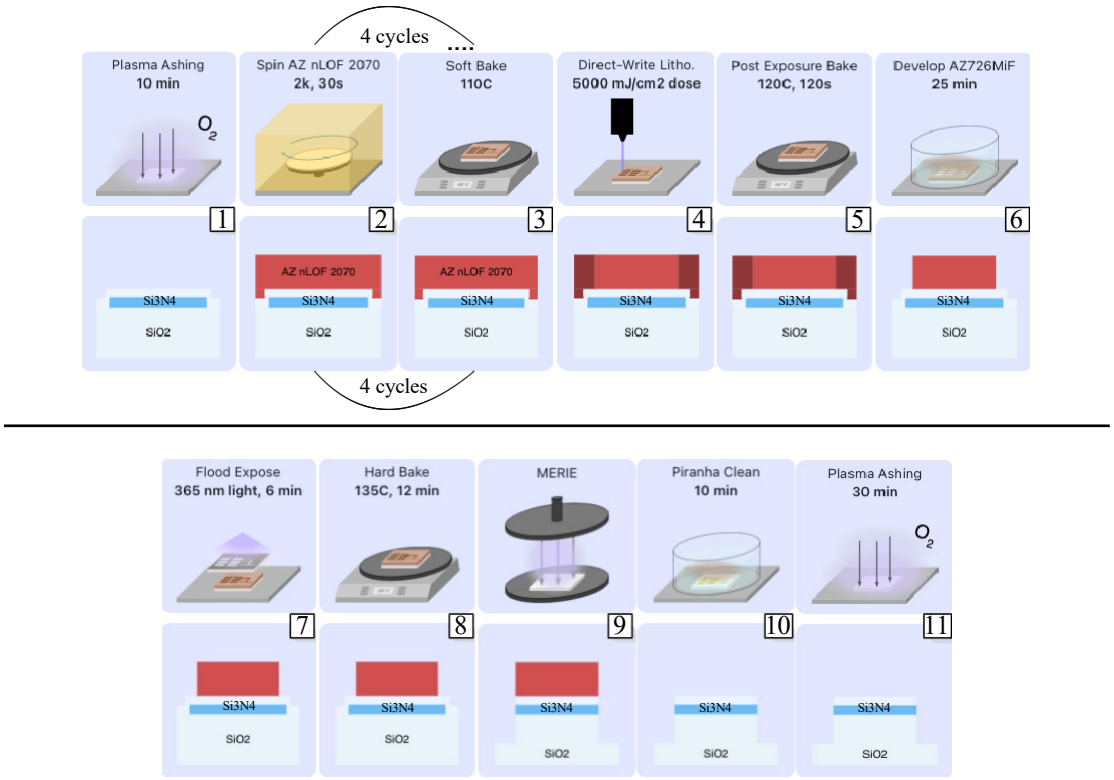
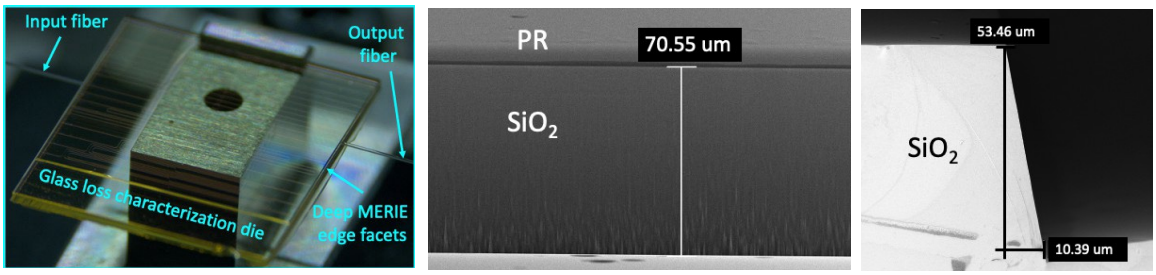


Figure 1: In (a) a cross sectional view of the experiment with a callout showing the double taper design. In (b) the process flow for packaging and assembly of the inter-chip coupling prototype. In (c), the fully packaged system are shown on the testing stage. In (d) and (e) images show the minimum and maximum feature sizes were accurately achieved for SOI and Si_3N_4 after ICP-RIE using the process flow outlined in Fig. 1(b). In (f) the images show a SOI edge facet for a dummy sample fabricated using the MERIE and DRIE technique.

contrast [9]. By optimizing a double taper coupler geometry using 3D FDTD simulations, footprint was minimized ($< 520\ \mu m$ total length) for wide alignment tolerances ($> \pm 2.5\ \mu m$) compared to linear inverse tapers [9]. Prototypes were made according to the flow shown in Fig. 1(b), with an image of a final package shown in Fig. 1(c). The flow started with 150 mm fused silica wafers with a 220 nm low pressure chemical vapor deposited Si_3N_4 film and 150 mm SOI wafers (250 nm device layer, 5 μm buried oxide (BOX)). Waveguides were patterned using electron beam lithography (EBL) with an Elionix HS-50, 50 keV accelerating voltage system followed by inductively coupled plasma reactive ion etching (ICP-RIE) using a Samco RIE-230iP tool, and were cladded with 500 nm SiO_2 using plasma enhanced chemical vapor deposition (PECVD) on a Samco PD220NL tool. The measured SOI sidewall slope, as shown in Fig. 1(d), was 7.97° while the Si_3N_4 sidewall slope was 6.48° as shown in Fig. 1(e). The samples were annealed using a Lindberg/Blue M CC58434P4C furnace at 1000°C for 2 hours in an N_2 ambient environment to remove excess hydrogen in the PECVD SiO_2 cladding. This prototype was for testing the evanescent coupler only, so SOI was used as the package substrate due to the fact that fabrication of high quality edge facets could be done through well established processes [10]. These processes included defining the edge facet mask which done using 375 nm direct write UV lithography on a Heidelberg MLA 150 tool where sub-micron mask alignment was accomplished using specialized alignment crosses on the SOI substrate. Following mask patterning, a combination of magnetically enhanced RIE (MERIE) using an Applied Materials Precision 5000 RF tool followed by deep reactive ion etching (DRIE) on a STS Pegasus Pro ICP tool. The trench depth was verified after etching to ensure an SMF with a diameter of 127 μm could fit without contacting the substrate, and it was determined via profilometry to



(a)



(b) (c) (d)

Figure 2: Images showing fabrication of the separate fused silica die. In (a) the fabrication process for the fused silica die edge facets. In (b) the fabricated glass die with Si_3N_4 waveguides is shown on the testing stage. In (c), a cross sectional image of a fully etched dummy sample is shown after MERIE, but prior to photoresist removal. In (d), a zoomed in cross sectional image of a partially etched dummy sample after photoresist removal showing the edge facet slope.

be approximately 150 μm deep. Examples SEM images are shown in Fig. 1(f) demonstrating deep SOI edge facets, in this case created in dummy samples which only went approximately 125 μm deep. After DRIE, wafers were diced and cleaned thoroughly using a combination of an O_2 plasma clean and isopropyl alcohol.

B. Automated Flip-Chip Packaging with Passive Assembly

Prior to bonding, die were inspected and cleaned again using a non-particulating cotton swab with isopropyl alcohol (IPA) while under a microscope to ensure no stray dust would impact the chip-to-chip gap size (i.e. the thickness of the epoxy). Immediately prior to bonding, a 27 gauge syringe needle was used to apply a droplet of NOA61 UV curable epoxy [11] to the center of the lower chip via gentle dabbing of the SOI chip. Bonding was performed using a Finetech FINEPLACER® femto 2 commercially available, high speed pick-and-place die bonder through passive alignment with machine vision only [12]. During bonding, the alignment marks on the die and the substrate were passively located using the tools machine vision system and the die was flip-chip bonded

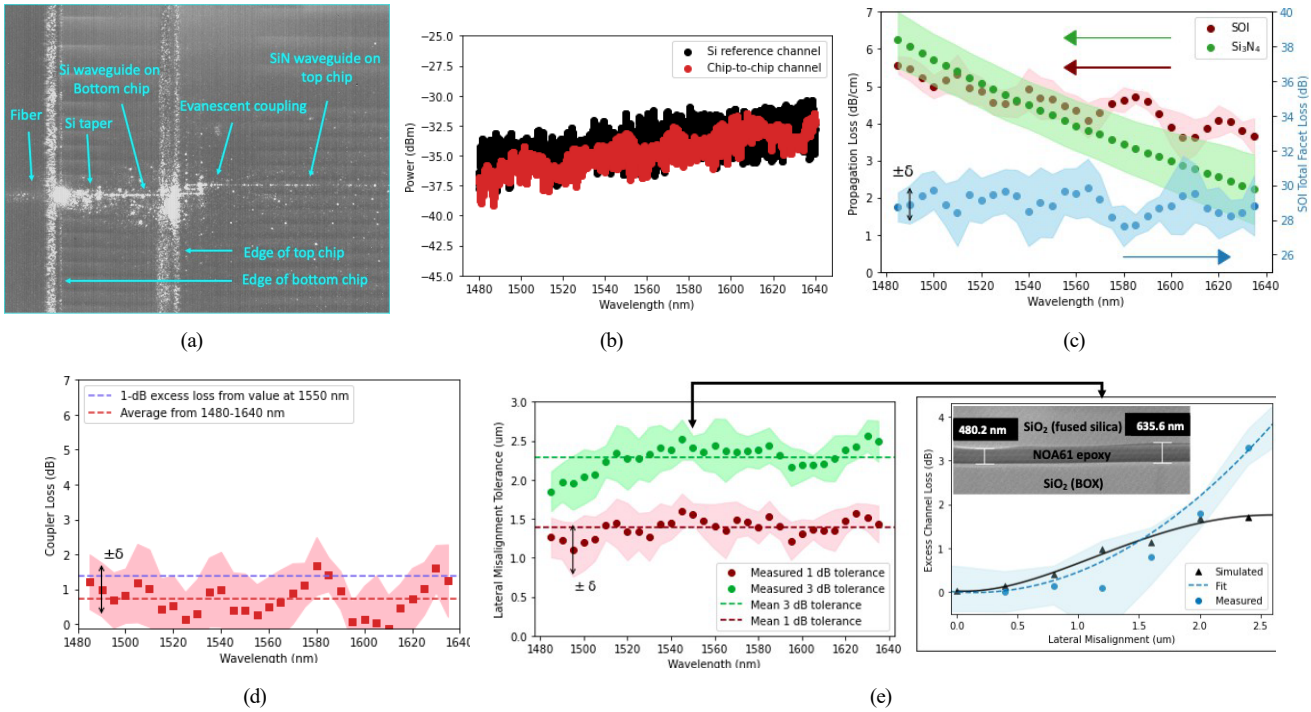


Figure 3: The image in (a) shows coupling near 1550 nm from the SMF to the SOI package substrate and into the separate fused silica die using a mounted infrared camera. In (b) raw data of a wavelength sweep for a reference Si channel and a chip-to-chip channel. In (c) the propagation loss for the SOI and Si_3N_4, and the facet loss for the SOI, are shown. In (d) $P_{chip\text{-}to\text{-}chip}$ is shown for the best aligned channel. The inset shows schematically the plotted quantity. In (e), the 1-dB and 3-dB lateral alignment tolerances from 1480-1640 nm. The callout shows measured and 3D-EME results at 1550 nm. The inset is a cross sectional SEM image of a bonded package showing an epoxy thickness of 0.48-0.64 μm.

with sub-micron precision. The flip-chip bonding step included the application of 40N of force. While the tool was applying pressure, the epoxy was cured in-situ using a 1 minute exposure from a UV lamp with the light source pointed at the side of the die-substrate system. After the tool had stopped applying pressure and the tool arm retracted, a second 1 minute exposure was initiated to ensure full curing. Cross sectional measurements on bonded dummy samples using an SEM (shown later in Section III) demonstrated the epoxy bond line thickness was on the order of 0.48-0.64 μm.

C. Silicon nitride-on-fused silica substrates for loss characterization

A separate LPCVD Si_3N_4-on-fused silica chip was also fabricated as a means of measuring the Si_3N_4 propagation loss. The process flow for this chip was identical to that outlined in Section A except for the PECVD SiO_2 cladding thickness, anneal time, and edge facet process flow. Specifically, the PECVD SiO_2 cladding thickness was 2 μm instead of 500 nm and the anneal time was approximately 10 hours instead of 2 hours to account for the thicker cladding. The edge facet process flow, as shown in Fig. 2(a), involved patterning the die with a 44 μm thick AZ nLoF 2070 resist mask, as measured using profilometry with minimal undercut, using consecutive spin cycles. Moreover, between each new coat of photoresist, a different softbake time was implemented to account for the thicker photoresist (with all softbakes being done at 110°C), which were as follows: 1) 2 min, 2) 2 min, 3) 4 min, and 4) 11 min. The facet etching was done using MERIE with the same etch recipe and tool (except with a longer etch time) used for the 5 μm SiO_2 BOX of the SOI in Section A. The final die on the testing stage can be seen in Fig. 2(b). Using a combination of optical microscopy and profilometry, the SiO_2 etch depth was determined to be approximately 68 μm as shown in Figure 2(c) with a roughly 78°sidewall slope as shown in Fig. 2(d). The thick photoresist was stripped using a heated piranha solution (1:1 H_2SO_4:H_2O_2) at 85°C followed by a 30 minute O_2 plasma treatment. The dicing process was then identical to that outlined in Section A.

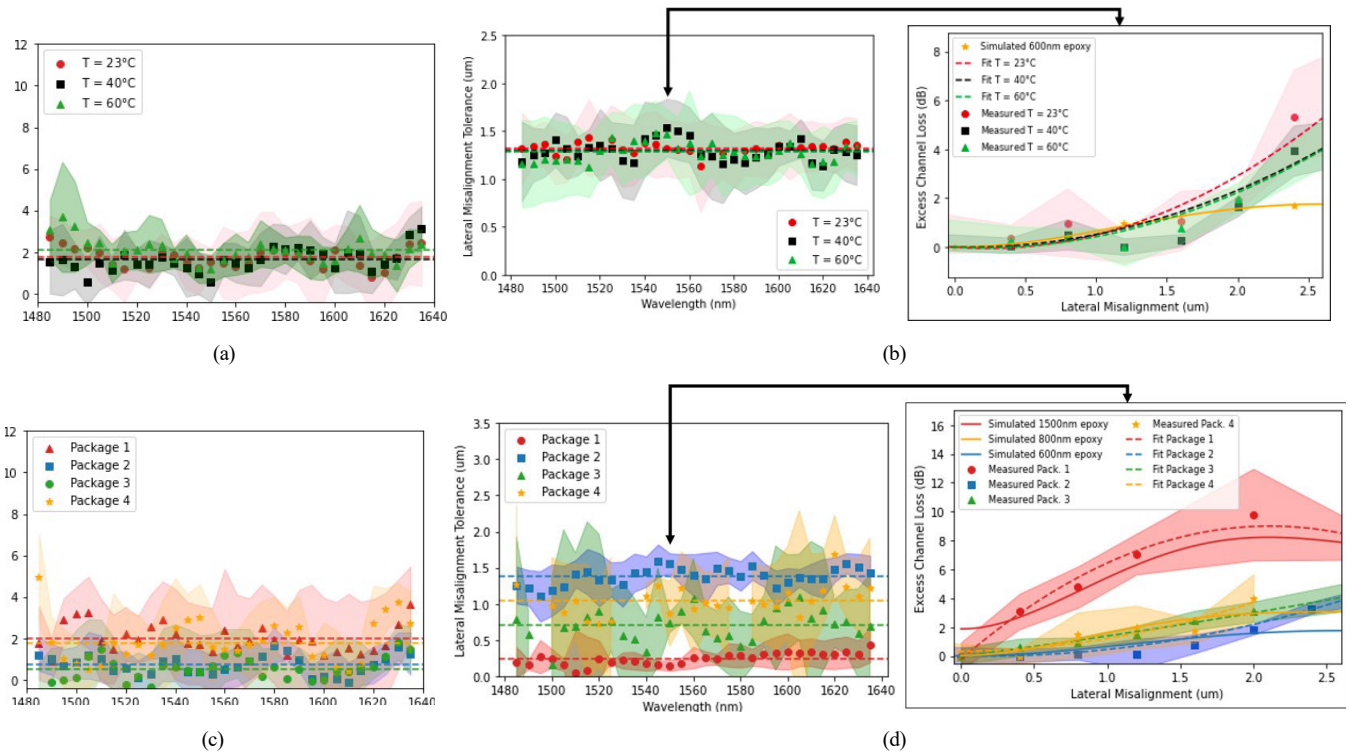


Figure 4: In (a) and (b) the data for $P_{\text{chip-to-chip}}$ and the 1-dB lateral alignment tolerance, respectively, are shown for temperatures between 23°C and 60°C. Likewise in (c) and (d) the data for $P_{\text{chip-to-chip}}$ and the 1-dB lateral alignment tolerance, respectively, are shown for four separately packaged systems.

D. Testing setup for PIC characterization

A Vernier waveguide layout comprised of 14 Si channels with a pitch of 127 μm and 14 Si_3N_4 channels with a pitch of 127.4 μm was used to measure lateral alignment tolerance to within 400 nm precision. Additionally, Si_3N_4 spirals of length 2-5 cm and Si spirals of length 1-5 cm were included to determine the propagation loss for the Si and Si_3N_4, and facet loss for the SOI. These spirals were necessary to determine the loss of a single evanescent coupler using the following equation:

$$P_{\text{chip-to-chip}} = \frac{(P_{\text{output}} - P_{\text{facets}} - P_{\text{Si}} - P_{\text{SiN}})}{2} \quad (1)$$

The testing setup consisted of a 1480-1640 nm wavelength laser injecting 0 dBm of light into a SMF. The SMF connected to a tapered, lensed polarization maintaining fiber (8 μm core, 125 μm cladding, 3 μm working distance) which went through polarization controlling paddles before being connected to a piezoelectric arm for sub-micron fiber-to-chip alignment. Once edge coupled, light traveled from the lower die's Si waveguides to the upper die's Si_3N_4 waveguides using the vertical coupler and then back down using a second vertical coupler where it was collected using an edge coupled, lensed SMF and fed into a photodetector. The aforementioned testing was repeated across four sets of packaged die to determine process and device repeatability. Finally, because the stage that the packaged die were positioned on could be temperature controlled from 23-60° C, measurements were repeated for the best performing package at temperatures of 23° C, 40° C, and 60° C to determine thermal stability.

III. Results

Successful inter-chip evanescent coupling was observed across the S, C, and L bands (1480-1640 nm wavelengths), as demonstrated by the example image in Fig. 3(a). This image was taken through the back of the glass top die using the mounted infrared camera, showing strong evanescent coupling near 1550 nm. A plot showing the raw measured output power for an entirely Si reference channel and a well aligned chip-to-chip channel can be found in Fig. 3(b). To determine P_{Si}, P_{SiN}, and P_{facets}, the output power versus spiral length was fit for wavelength windows pf ± 2.5 nm using linear regression, with the results being shown in Fig. 3(c).

Table 1: Summary of silicon photonic chip-to-chip evanescent couplers in chronological order of publication date. The rows shaded red indicate only simulation results were reported. Only inter-chip couplers were included.

Package	CL_{1550} (dB)	1-dB Tolerance (μm)		1-dB Bandwidth (nm)	LxW (μm)	Reference
		Lateral	Vertical			
SOI to polymer	0.4 (TE)	± 3	/	± 100 (1550)	200x5	[13]
SOI to polymer	0.4 (TE/TM)	2	1.5	100 (1470-1570)	1750x5.915	[5, 14]
Si_3N_4 to Si_3N_4	3.1	< ± 1	< 0.6	/ (1550)	500x3	[15]
Si_3N_4 to Si_3N_4	0.76	± 2	< 1	/ (1550)	500x3	[16]
SOI to polymer	1.25/0.5 (TE/TM) < 0.5 (TE/TM)	± 2 /	/	± 60 (1310) ± 70 (1550)	1500x6.5	[17–19]
SOI to polymer	0.2	> ± 5 ± 1.5°(yaw)	0.5	± 100 (1550)	200x15.3	[20]
SOI to IOX	< 1 (TE/TM)	± 4	3	± 30 (1550)	1500x12	[21]
Si_3N_4 to IOX	0.7	> ± 4	< 2	75 (1515-1590)	2000x11	[22]
Si_3N_4 to Si_3N_4	0.54	< ± 2	< 0.8	400 (1200-1600)	1000x3	[23]
SOI to Si_3N_4	**0.39 (TE)**	**± 1.56**	**> 1.1**	**160 (1480-1640)**	**520x1**	**this work**

CL_{1550} = coupling loss at 1550 nm wavelength
/ = not reported

By inserting the values for P_{output}, P_{Si}, P_{SiN}, and P_{facets} into Eq.1, $P_{chip\text{-}to\text{-}chip}$ was determined for all 14 chip-to-chip channels. The coupling loss for one of the best-aligned channels is shown in Fig. 3(d), with a value of 0.39 ± 1.06 dB at 1550 nm wavelength. The average coupling loss across the 1480-1640 nm spectrum was calculated to be 0.73 ± 0.92 dB (± 2σ) and the average coupling loss was 0.54 ± 0.90 dB across the C band (1530-1565 nm). The 1-dB excess loss wavelength tolerance, also termed the 1-dB bandwidth, was determined to be 160 nm based on Fig. 3(d), extending from 1480 nm to 1640 nm wavelength. This is supported by the fact that over 90% of the coupling loss data fell within ± 1 dB of the loss at 1550 nm.

Likewise, the 1-dB and 3-dB excess loss lateral alignment tolerances were determined using the Vernier layout, with results shown in Fig. 3(e). Specifically, the output power for all channels was normalized to the best aligned channel, the data was fit using a quadratic regression, and the 1-dB and 3-dB roll-off was determined. It was assumed that the best aligned channel had 0 μm lateral misalignment, with each adjacent channel having an additional 0.4 μm of misalignment. Based on this analysis, the passive pick-and-place accuracy for this set of chips was approximately 0.4 μm. The 1-dB alignment tolerance at 1550 nm was ± 1.56 μm and the 3-dB alignment tolerance was ± 2.41 at 1550 nm. Similarly, the maximum 1-dB tolerance was ± 1.60 μm at 1545 nm while the average 1-dB tolerance from 1480-1640 nm was ± 1.38 μm, with 95% of the data falling within ± 0.24 μm of this value for a vertical taper-to-taper spacing of greater than 1 μm.

Furthermore, the same data analysis for calculating the alignment tolerance and coupler loss was performed on the values obtained for the three different temperatures: 23°C, 40°C, and 60°C. The results for coupler loss can be found in Fig. 4(a) and the results for lateral alignment tolerance can be found in 4(b), alongside 3D EME simulation data for 600 nm thick NOA61 epoxy (which was run using room temperature conditions). The average coupling loss from 1480-1640 nm with uncertainty (i.e. one standard deviation) was 1.73 ± 0.46 dB, 1.62 ± 0.55 dB, and 2.08 ± 0.56 dB for 23°C, 40°C, and 60°C, respectively. The average 1-dB alignment tolerance from 1480-1640 nm with uncertainty was 1.32 ± 0.13 μm, 1.30 ± 0.21 μm, and 1.28 ± 0.19 μm for 23°C, 40°C, and 60°C, respectively. The plots of coupling loss and alignment tolerance for the four different packaged die can be found in Fig. 4(c) and 4(d), respectively. The average coupling loss from 1480-1640 nm with uncertainty was 2.00 ± 0.66 dB, 0.72 ± 0.46 dB, 0.51 ± 0.68 dB, and 1.88 ± 1.04 dB for Package 1, Package 2, Package 3, and Package 4, respectively. The average 1-dB alignment tolerance with uncertainty was 0.24 ± 0.16 μm, 1.38 ± 0.24 μm, 0.71 ± 0.42 μm, and 1.05 ± 0.40 μm for Package 1, Package 2, Package 3, and Package 4, respectively.

IV. Discussion

Based on the results presented in Section III, there are several notable aspects, beginning with the wavelength dependencies for the plots in Fig. 3. The coupling loss and 1-dB lateral misalignment tolerance showed little wavelength dependence between 1480-1640 nm, as indicated by the fact that 95% of the tolerance data falls within ± 0.24 μm of the mean, and 100% of the loss data falls within ± 1 dB of the mean. The data in Fig. 3(e), 4(b), and 4(d) also aligned well with 3D EME simulations done using Ansys Lumerical. From Fig. 3(e), the difference between the simulated data and the fit line of the measured data at 1550 nm was less than 0.1 dB for

misalignments of 1.5 μm or less and was less than 0.75 dB for misalignments of 2 μm or less. The divergence of the measured data from the simulated data by more than 0.75 dB for misalignments of 2 μm or more can be explained by the SiO-H absorption in the PECVD SiO_2 cladding [24] and any absorption within the NOA61 epoxy.

Furthermore, the data from Fig. 4 demonstrated the limited impact of temperature and repeatability across multiple packages. For example, in Fig. 4(a) the average coupling loss from 1480-1640 nm varied by less than $\pm$ 0.35 dB for temperatures from 23°C to 60°C. Similarly, in Fig. 4(b) the 1-dB lateral alignment tolerance varied by less than $\pm$ 30 nm from 23°C to 60°C. Along the same lines, from Fig. 4(c) it can be seen that the average coupling loss from 1480-1640 nm varied by less than 1.5 dB from the minimum of 0.51 dB (Package 3) to a maximum of 2.00 dB (Package 1). Similarly, Packages 2-4 show a tightly bound 1-dB lateral alignment tolerance with the average, calculated after combining the data from these three packages, being $\pm$ 1.05 μm with a standard deviation of $\pm$ 0.35. The lower alignment tolerance of Package 1, can be explained by a larger epoxy thickness. Based on how the EME simulation data correlates with the measured data in the callout of Fig. 4(d), the epoxy thickness for Package 1 is 0.7-0.9 μm larger than for Packages 2-4, meaning the total taper separation is approximately 2-2.25 μm compared to 1.1-1.8 μm. Despite the larger thickness, the coupling performance was not adversely affected as evidenced by the 2.00 $\pm$ 0.66 dB average coupling loss as shown in Fig. 4(c).

Lastly, a comparison of this device to other chip-to-chip evanescent couplers is shown in Table 1. To the best of the authors' knowledge, this was the first demonstration of an inter-chip evanescent coupler directly connecting SOI waveguides to other Si based waveguides. Moreover, the 1550 nm coupling loss of 0.39 $\pm$ 1.06 dB was on par with the lowest coupling losses reported for an entirely Si based coupler. The maximum 1-dB lateral alignment tolerance of $\pm$ 1.60 μm at 1545 nm was also on par with other experimentally demonstrated inter-chip evanescent couplers and was shown to be large enough to enable passive assembly using automated pick-and-place tools [12, 25]. Additionally, the longitudinal footprint was roughly a third of the typical length of other models, and the lateral footprint occupied only 33% of the space of the next thinnest design (and roughly 10%-20% of the space of typical designs), showing the potential for scaling to Pbps input/output counts in integrated photonic systems. Finally, the vertical taper-to-taper distance measured in this study was greater than 1 μm which will aid significantly in making the design compatible with typical BEOL layer thicknesses.

V. Conclusion

In summary, an evanescent package substrate-to-die coupler was fabricated, packaged, and tested using standard CMOS foundry materials and processes. The resultant data demonstrated the high performance of the coupler including sub-dB losses, broadband operation, robustness to lateral and vertical misalignment, low thermal sensitivity, and device repeatability. When employed in CPO designs, this inter-chip coupler can enable Pbps total data capacities by dramatically increasing the number of parallel I/O channels while simultaneously reducing the packaging and assembly inefficiencies associated with die-to-SMF connections.

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