Enhancing Signal Integrity in High-Performance Electronics through Advanced TGV Fabrication with LPKF's LIDE Technology

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Abstract

This paper explores the innovative Laser Induced Deep Etching (LIDE) technology developed by LPKF, focusing on its application in fabricating Through-Glass Vias (TGVs) for high-performance electronics. LIDE technology presents a significant advancement in microstructuring glass, addressing the critical challenge of surface roughness in TGV sidewalls, which is essential for minimizing signal loss in high-frequency communication systems.

The study delves into the LIDE process, which involves precise laser modification followed by wet chemical etching, producing high-aspect-ratio structures with exceptional smoothness and accuracy. The experimental results highlight the advantages of LIDE over traditional methods, including improved sidewall quality and reduced defects, leading to enhanced signal integrity and electrical performance. By optimizing parameters such as laser power and etching conditions, the research demonstrates the potential of LIDE to set new benchmarks in electronic packaging.

LIDE's compatibility with various glass types and its scalability for high-volume production make it a versatile and economical solution for modern microelectronic applications. This paper underscores the transformative impact of LIDE technology on the fabrication of TGVs, paving the way for advancements in 2.5D and 3D packaging, and contributing to the broader goals of reducing signal loss and improving system performance in high-frequency electronics.

Key words

Laser Induced Deep Etching, Through Glass Via, Glass Substrate, Advanced Packaging, High-Frequency Communication

I. Introduction

The evolution of high-performance electronics hinges on advancements in packaging technologies that offer both precision and reliability. Through-Glass Vias (TGVs) have emerged as critical components in this landscape, enabling compact and efficient vertical interconnections essential for 2.5D and 3D integrated circuits. However, the fabrication of TGVs presents significant challenges, particularly concerning the surface roughness of the via sidewalls, which can adversely affect signal integrity in high-frequency applications.

A. Material Properties of Glass

B. Glass is arguably one of the most interesting materials for heterogeneous integration. Whether it is for its RF properties, high surface quality, hermeticity, tunable coefficient of thermal expansion (CTE) or low cost, there are several reasons to favor glass for advanced packaging applications. [2] Unfortunately, and up to now, the processability of glass has not been among those reasons. This is because current glass processing technologies typically induce micro-cracks and stresses which contribute to glass's reputation of being prone to brittle fracture. In contrast, glass without surface defects has excellent

mechanical properties as it can be demonstrated when it is processed by Laser Induced Deep Etching. [1]

C. Surface Morphology and Signal Integrity

Research indicates that the roughness of TGV sidewalls directly impacts electrical performance. High-frequency signals are particularly sensitive to surface imperfections, which can cause signal reflection, scattering, and attenuation. Optimizing the fabrication process to minimize these effects is therefore critical. [3]

II. Methodology

D. LIDE Process Description

LPKF's patented LIDE technology represents a breakthrough in glass micro structuring. LIDE combines TGV formation for high volume manufacturing and sophisticated geometry pattern like cuttings and closed cavities for advanced packaging applications [Fig. 1].

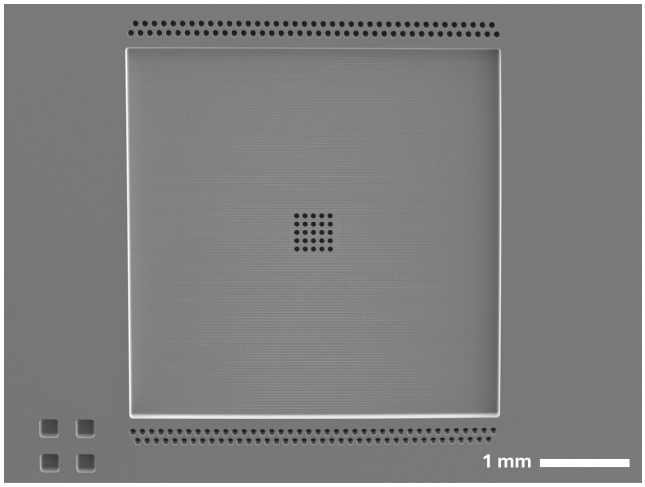

Fig. 1 - SEM image of multiple structures made with LIDE (TGV, closed cavities, blind vias, and TGV in the bottom of the closed cavity)

The LIDE process involves two primary steps:

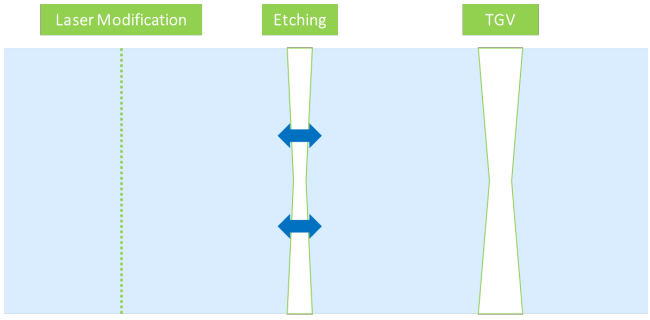

Fig. 2 - Two-step process involves laser modification and etching.

First step - laser modification: A single laser pulse modifies the glass substrate according to the desired pattern. This step does not remove any material but changes the properties of the glass locally. The initial modification is less than 1µm in width and can be described as a chain of blisters. The etch rate along this gentle modification is 100 times higher compared to the rest of the glass material. The laser parameters are optimized with the goal to work with as many glass types as possible.

Second step- wet etching: The entire glass surface is subjected to wet chemical etching. The initial phase of etching is characterized by anisotropic etching along the laser modification which was introduced during the laser modification step. The modified regions etch anisotropic until all material which was modified is removed and forms a through hole of below 3µm. During the initial etching glass type and etching condition determine how steep the sidewalls of the through hole will be, creating an individual process window for each glass type [Fig. 3].

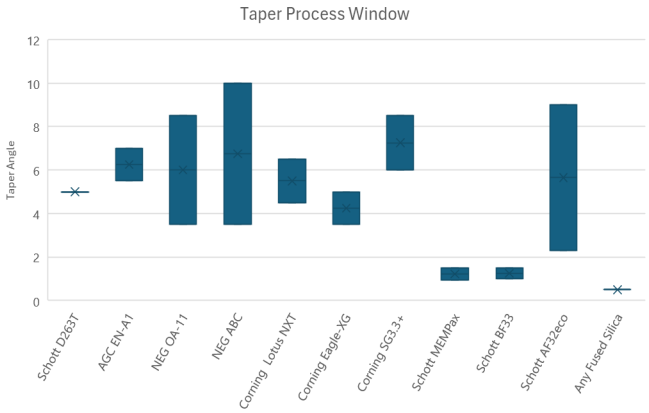

Fig. 3 - Glass dependent taper angle under standard etching conditions from LPKF's Vitrion glass manufacturing service

E. TGV Sidewall Roughness

The roughness of a via sidewall is the result of multiple factors including the type and shape of the initial laser modification, glass type, etching condition, etching time, and more.

For this experiment we used two different glass types of Schott AF 32 eco and Schott BF 33 with an initial material thickness of 500 µm and introduced them with two different standard etching conditions from our Vitrion manufacturing service. The modified glasses where either etched in HF or NaOH with different Top Target Diameters (TTD).

F. Measurement Techniques

In order to measure the sidewall roughness of TGV's we had to break the glass with a scribe and break technique. This

procedure exposes the cross section of the via.
We measured the cross sections with a Keyence VK-X3000 Wight Light Interferometer Module with a 20 times magnification [Fig. 4].

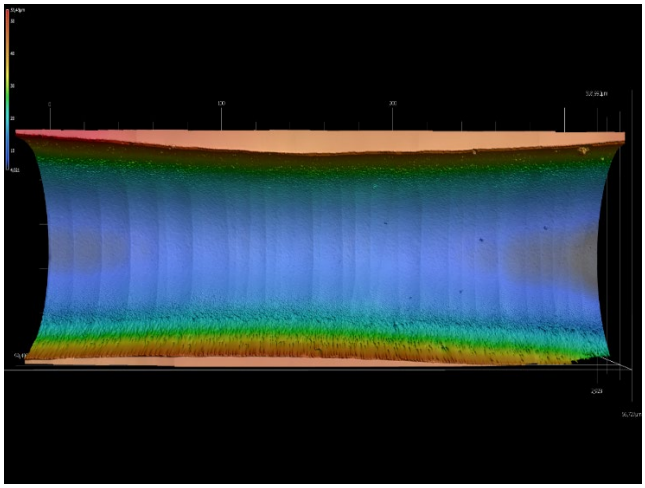

Fig. 4 - Keyence VK-X3000 WLI cross section image a TGV Schott BF 33 TTD of 100 µm

The sidewall line roughness measurement was performed over the full via sidewall length and filtered with a cut-off [Fig. 5] in respect to ISO 4288 (04/98). The measured roughness data will be reported with four different parameters.

The characterization of TGV sidewall roughness is crucial for understanding and optimizing their impact on signal integrity. Various roughness parameters provide a comprehensive view of the surface quality. Average roughness (Ra) is a common metric that indicates the mean surface roughness over a given length, providing a general sense of the overall texture. Maximum height of profile (Rz) measures the vertical distance between the highest and lowest points in a sample length, capturing the extreme deviations on the surface. Ten-point mean roughness (RzJIS) averages the heights of the five highest peaks and the five deepest valleys, offering a balanced view of the surface profile. Root mean squared roughness (Rq), which is the square root of the mean of the squares of the surface deviations, gives a more sensitive measure to occasional high peaks and deep valleys. By analyzing these parameters, we can better understand the impact of sidewall roughness on metallization processes and signal integrity, leading to more reliable and high-performance TGVs in electronic applications.

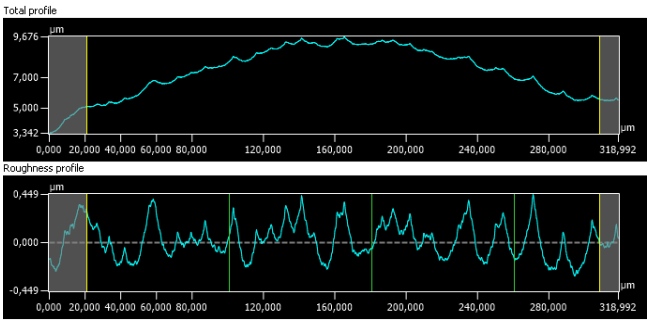

Fig. 5 - TGV sidewall line roughness profile Schott BF 33 etched in HF with a TTD of 100 µm

III. Results

G. Measurement Results

Our measured data indicates that under our standard etching conditions the sidewall roughness decreases over time and approximately reaches a material dependent optimum as shown in Fig. 6 for Schott BF 33 etched in HF.

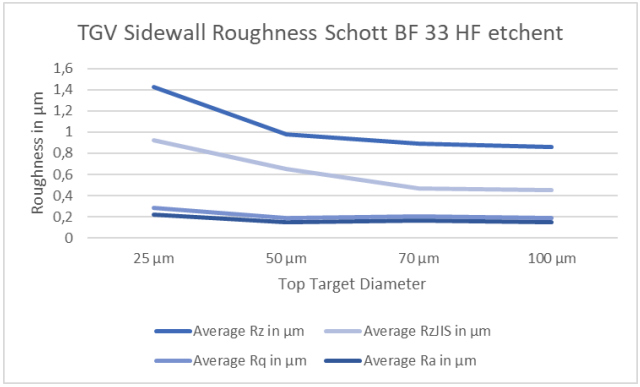

Fig. 6 – TGV sidewall measurements results for HF etched Schott BF 33

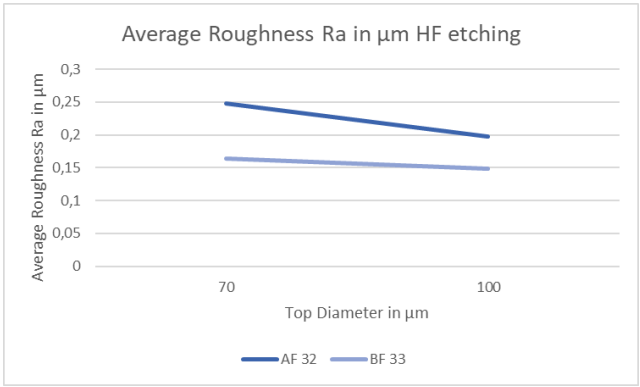

Fig. 7 – Comparison between TGV sidewall roughness Ra measurements between Schott AF 32 eco and Schott BF 33

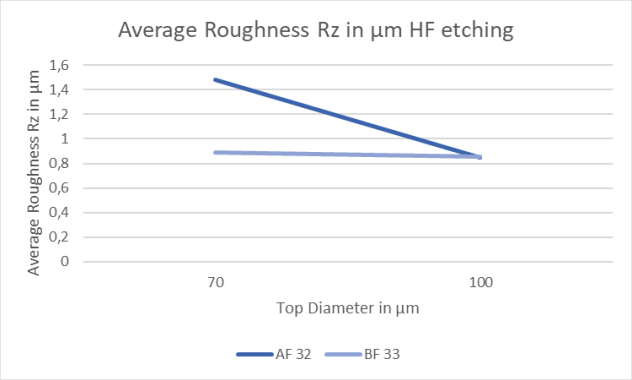

Fig. 8 – Comparison between TGV sidewall roughness Rz measurements between Schott AF 32 eco and Schott BF 33

H. Impact on Signal Integrity

Until this point, we were not able to perform electronical measurements to ensure the effects of different sidewall roughness. The exceptional performance of TGVs produced with LIDE technology in BF 33 with top diameter of 80 µm was already shown [4].

IV. Discussion

I. Using different roughness measurements

Different roughness parameters provide unique insights into how surface quality impacts signal loss in TGVs. Average roughness (Ra) gives a general measure of surface texture but may overlook extreme deviations that can cause localized signal issues. Maximum height of profile (Rz), by measuring the vertical distance between the highest peak and the lowest valley, highlights significant surface irregularities that can lead to increased signal reflection and scattering, causing greater signal loss.

Ten-point mean roughness (RzJIS), which averages the heights of the five highest peaks and the five deepest valleys, offers a balanced view of the surface profile and its potential to cause signal degradation. This parameter helps in understanding the impact of peak-induced scattering and valley-induced attenuation. Root mean squared roughness (Rq), being more sensitive to occasional high peaks and deep valleys, provides a comprehensive measure of overall surface variability. Higher Rq values indicate greater electromagnetic interference and signal distortion.

Together, these parameters enable a thorough analysis of TGV sidewall roughness and its effects on signal integrity. By leveraging the insights from these measurements, we can optimize the LIDE process to produce TGVs with minimal signal loss, thereby enhancing the performance and reliability of high-frequency electronic applications.

J. Optimization of TGV sidewall roughness

In the pursuit of superior performance in high-frequency electronics, the smoothness of TGV sidewalls has become a critical factor. Lower etching rates are instrumental in achieving smoother sidewalls, with high aspect ratios, as they allow for more controlled material removal but come with an increased processing time. Our investigation into a two-step etching process reveals that beginning with a low etch rate during the initial phase helps establish a precise and smooth etching front. This is followed by a faster etching phase to enhance throughput without compromising sidewall quality. This dual-phase approach strikes a balance between achieving the desired smoothness and maintaining industrial efficiency.

There is a significant industrial demand for lower sidewall roughness in TGVs, driven by the need for higher signal integrity and reliability in advanced electronic packaging. Smooth sidewalls are essential to minimize signal loss, reflections, and scattering, which are crucial for maintaining the performance of high-frequency and high-speed electronic devices. As applications in telecommunications, data centers, and advanced computing continue to grow, the requirement for impeccable signal transmission and integrity becomes even more critical. Industries are increasingly recognizing that investing in technologies that deliver smoother sidewalls, such as LIDE, translates to better overall performance and reliability of their products, making it a priority in semiconductor manufacturing.

K. Advantages of LIDE Technology

LPKF's patented Laser Induced Deep Etching (LIDE) technology offers several notable advantages over traditional laser-based processes, establishing it as a superior method for micro structuring glass. One of the primary benefits is the absence of defects. Since the laser modification step in LIDE does not involve material removal, the modified areas remain free of defects such as cracks or chips, ensuring high structural integrity. This technology is also capable of producing high-precision microstructures with fine features and high aspect ratios, making it ideal for advanced electronic applications.[5][6]

Another significant advantage is its compatibility with a wide range of commercially available glass types, eliminating the need for special or custom glass materials. This compatibility extends to various glass thicknesses and sizes, enhancing its versatility across different applications.

Additionally, LIDE technology is both economical and scalable, suited for high-volume production due to its reduced processing time and cost-effectiveness. The process can be finely tuned to meet specific industrial needs, to achieve even higher quality in large-scale manufacturing. This flexibility ensures that LIDE

technology can adapt to the evolving demands of the electronics industry, providing a robust and reliable solution for the precise fabrication of glass microstructures.

V. Conclusion

The evolution of high-performance electronics hinges on advancements in packaging technologies that prioritize precision and reliability. TGVs have become essential for efficient vertical interconnections in 2.5D and 3D integrated circuits. However, fabricating TGVs with smooth sidewalls remains a challenge due to the impact of surface roughness on signal integrity in high-frequency applications.
Glass, with its excellent RF properties, high surface quality, and tunable coefficient of thermal expansion (CTE), is ideal for advanced packaging but has traditionally faced processability issues due to induced defects. LPKF's Laser Induced Deep Etching (LIDE) technology overcomes these challenges by creating high-precision, defect-free microstructures in glass.

Our research shows that LIDE technology, through a two-step process of laser modification and wet etching, produces TGVs with significantly smoother sidewalls, enhancing signal integrity and electrical performance. This method balances precision and industrial efficiency, making it suitable for high-volume production.[3]

LIDE technology stands out for its compatibility with various glass types, cost-effectiveness, and scalability. It addresses the critical industrial demand for lower sidewall roughness in TGVs, ensuring better performance and reliability in high-frequency electronic applications. Future research will focus on optimizing LIDE for extremely thin glass substrates and further integration with semiconductor manufacturing processes, solidifying its role in the future of electronic packaging.

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