Optimizing Flip Chip Packaging for High Density Bump via Mold Flow Simulation with Through-Holes

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Abstract

Flip-chip packaging techniques have become essential for electrical components, particularly in fine-pitch packages where bump sizes are small and high density under the chip. These techniques enhance thermal performance and bump connections while addressing concerns about mold voids.

However, the high bump density and limited pitch in flip-chip techniques will lead to potential defects, including mold voids. To efficiently reduce voids, incorporating an extra runner in the package for void venting is one effective solution.

This study investigates the effects of through-hole size, molding resistance, and mold flow performance using an advanced methodology. This methodology considers govern equations such as the viscosity model, curing reaction, and Finite Element Method (FEM) analytical method, with a focus on the structure design to predict or evaluate defects occurring in molding process, particularly mold voids and the weld risk. One of the major challenges in this approach is controlling the distance and density of bump pitches on the substrate of bonded spheres while attached spheres to package.

The results demonstrate that a through-hole size of 0.2mm exhibits better performance in terms of potential mold voids with 44 units per strip, and 68 units for a 0.3mm through-hole size. Melting behavior under chips for void venting was clearly observed in specific areas. Additionally, the filling percentage, influenced by flow status, can be used to predict the mold flow risk. Base on FEM analytical, structure modification, and recipe optimization, ~~the~~ risk areas or positions can be identified and mitigated during the substrate or layout process.

The adoption of high-density bump technology has significantly advanced our packaging process, particularly as devices become smaller, especially in the case of safety devices where reliability and testing are subject to harsh conditions. Even packages with micro voids undergo rigorous testing procedures to ensure optimal performance and reliability.

Key words

Fluid kinematics, Components aspect ratio, Molding process, Mold voids, Bump density

I. Introduction

Advanced packaging techniques, characterized by high bump density and fine pitch under the chip, have become crucial in meeting the demands of modern multi-functional packaging solutions such as high bandwidth memory (HBM), high-performance computing (HPC), and 3DIC. These applications require higher data transmission speeds and higher frequencies, which have led to a reduction in the size of interconnect bump joints between the chip and substrate. These high-density interconnections do not include bump ratios, as well as chips and fine-pitch interposers.

This study presents a numerical assessment of the effectiveness of molding through bumps technology.

Nowadays, semiconductor manufacturers have put in a great effort to improve the production effectiveness of design for manufacture (DFM). In the process evaluations, if the package of flow capability inadequate usage of bumps leads to such dense ratio around the through via.

The high aspect ratio (HAR > 10) of through-package via (TPV) structures was studied by J.H et al. [1]. These structures enable electrical interconnects for high pin count

packages. This high density induces obvious molding resistance. Furthermore, the fields of microfluidics and optics in this design enable novel TPV functions. J.C et al. [2] mentioned that air trapped at the periphery of the lead frame causes worse flow interference between the high density of the lead frame and the tight EMC area. H.Y. [3] recommended that copper metallization was successfully plated along the sidewall with mold compound filler of either 20μm or 5μm, completing the bottom and side walls to achieve a continuous copper layer.

Typically, the bump density of packaging is considered uniform, but it is influenced by the structure and flow directions, as indicated by T.C et al. [4]. In addition, wafer-level packaging (WLP) or 3DIC packaging solutions, which include multi-layers through via in molding, or non-uniform pitch have been studied by J.H et al. [5]. The advanced packaging solution of via pass-through, while considering via size, leads to high performance in molding, would be separated by four diameters in this study.

II. Governing equations

A. Viscosity Model

In general, the viscosity of the epoxy molding compound must be processed at molding temperature with specific conversion rates and time limits. To describe the rheological properties of epoxy resins, we propose the Castro-Macosko model [6].

$$\eta\left(\alpha, T, \dot{\gamma}\right) = \left(\frac{\eta_0}{1+\left(\frac{\eta_0 \dot{\gamma}}{\tau^*}\right)^{1-n}}\right)\left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{C_1 + C_2 \alpha} \quad (1)$$

$$\eta_0 = A exp\left(\frac{T_b}{T}\right) \quad (2)$$

$$T_b = \frac{E_a}{R} \quad (3)$$

The model shows here of η is the viscosity, α is the reaction conversion, T is the temperature, γ is the shear rate to describe the material boundary connections, τ^* is the model constant and also indicates the shear stress rate, $1 - n$ is the pseudoplastic in the melt slope behavior, α_g is the gel point of the degree conversion, and A, E_a, C_1, C_2 are model parameters.

B. Curing Reaction

The thermoset EMC curing status after the filling process and during the curing procedure is considered and the kinetic governing equation with described chemical conversion we used was studied by Kamal and Ryan [7].

$$\frac{d\alpha}{dt} = (k_1 + k_2 \alpha^m)(1 - \alpha)^2 \quad (4)$$

$$k_1 = A_1 exp\left(-\frac{E_1}{RT}\right) \quad (5)$$

$$k_2 = A_2 exp\left(-\frac{E_2}{RT}\right) \quad (6)$$

Amount the time and viscosity interactions, in this study, where k_1 and k_2 are the rate constants of Arrhenius equations, m is empirical constants, E_1 and E_2 are the apparent conversion activation energies, R is the universal gas constant.

C. Bump Resistance and Through Via

The molding wave in the such of different structure causes multi-layers and non-uniformity, in this work, the through via located in the middle of the package to filling closer the wall as a free surface in our considerations is also proposed a model Bernoulli's principle:

$$\frac{P_1}{\rho} + \frac{V_1^2}{2} + g z_1 = \frac{P_2}{\rho} + \frac{V_1^2}{2} + g z_2 \quad (7)$$

$$V_2 = \sqrt{2g(D_1 - D_2)} \times \Delta T_\mu \quad (8)$$

Where P is the filling pressure at the through via entry boundary, ρ is the density of the fluid at all points in the fluid, V is the fluid flow speed at through via, g is the acceleration due to gravity, z_1 and z_2 are the elevation of the point describe through via at top and bottom, D_1 and D_2 are the through via diameter of upward and downward, ΔT_μ is the viscosity when filling is closed to transfer time above 80%.

III. Molding experiment and simulation setting

The real packaging process of flip-chip with bumps will impact mold resistance, so we set up such area of high and low resistance based on the bump density.

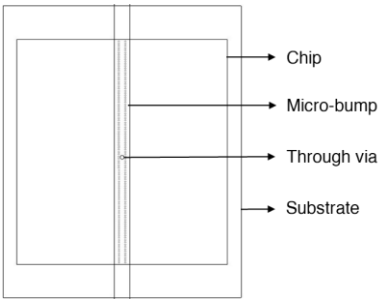


Fig. 1. Strip model and unit package boundry condition.

As shown in Fig. 2, this package uses a densely packed bump area located only in the middle of the chip, with both sides remaining empty to provide a strong contrast. The package includes a chip, high-density micro-bumps, one through via, and a substrate.

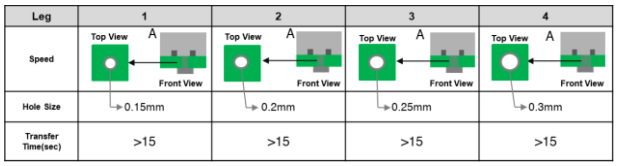


Fig. 2. Strip model and unit package boundry condition.

The limited change in the melting wave of the bump area is apparent. In Fig. 3, we consider different via sizes, such as 0.15mm, 0.2mm, 0.25mm, and 0.3mm, through the via to the bottom. These variations result in good performance in air trapping.

Material and Molding Recipe

Thorough to the structures in such a scenario, the EMC and molding recipe significantly influence mold void trapping.

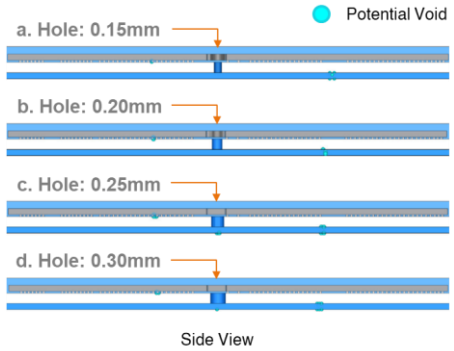


Fig. 3. Mold void of through via in vent(mm)

In general considerations, mold voids in the through via vent show potential voids remaining in the strip vent, with 0.25mm and 0.3mm via posing a higher risk.

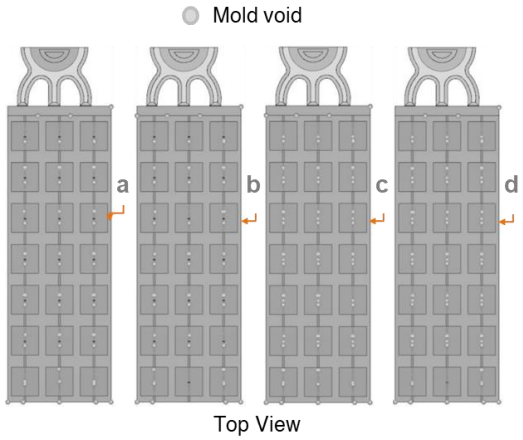
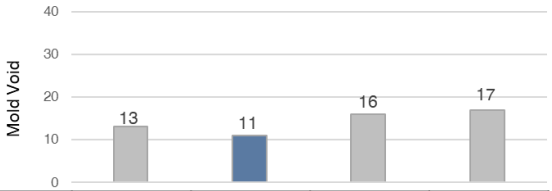


Fig. 4. Simulation of mold void position.

Fig.4 shows the top view of the model, also demonstrated the through via filling, the each devices of chip were follow the flow resistance which area is more smoothly, and the thickness roughly corresponding to the average thickness of each of the field which's under the chips and to account for the potential effect on the flow balance between strip rows. Gray points are shows potential mold void during melting wave on each packages.

TABLE I. THROUGH VIA MOLD VOID RESULT



Legs	1	2	3	4
Hole	0.15	0.20	0.25	0.30
Strip Mold Void(ea)	13	11	16	17

The condition of EMC and Recipe would be a challenges to minimize mold void. We developed methods to solve filling imbalances and air trapping.

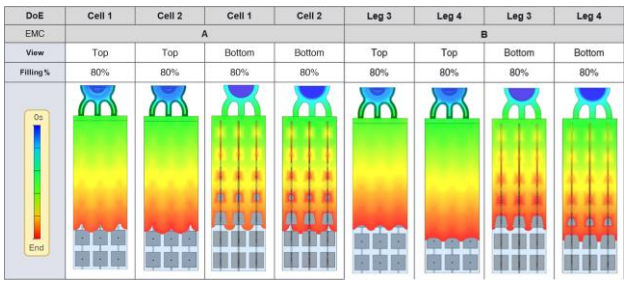


Fig. 5. Filling performance comparison(%)

Different EMCs (A and B) were compared, showing filling percentages of 80%, with variations in transfer time and material viscosity during and after the molding process. It is clear from the simulation results that the cells 2 and 4 exhibit unbalance filling and air trap at vent side.

DoE	Cell 1			Cell 2			Cell 3			Cell 4		
EMC	A			B			A			B		
Velocity(mm/s)	6	4	3	6	4	4	6	4	3	6	4	4
Transfer time(sec)	>15			<15			>15			<15		
Mold void(unit)	10			10			9			8		

Fig. 6. Simulation condition with material. Molding speed, transfer time, also results of potential mold void

The molding recipe in this study, based on real molding and common experience for transfer molding process is listed in Table I. Molding temperature, a general rule for Flip Chip (FC) devices, and transfer pressure were considered. Comparing EMC-A and EMC-B with respect to molding time, the results show that EMC-B, with a shorter transfer time, results in better mold voids.

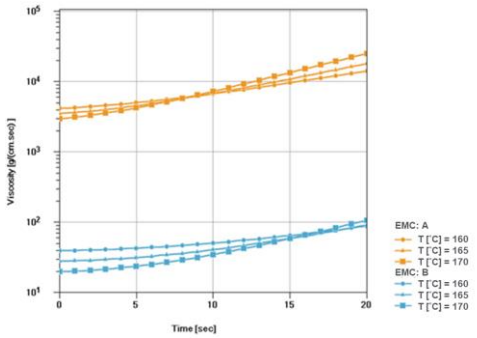


Fig. 7. Mold void occurred in the central of package after reflow by X-ray measurement.

Moreover, as shown in Figure 7, when comparing short transfer times, the viscosity curves of two EMCs during filling were analyzed and used for potential void prediction. the EMC-A showed high viscosity and short ramping between viscosity and time considerations. In contrast, EMC-B showed lower viscosity, ranging from 0 sec to 20 sec transfer time within 100 g/(cm · sec), an order gap is one for general rules of different material properties in semiconductor field.

Conclusion

The goal of this article is to evaluate HBM or HPC devices through via in molding, providing insights into structure, material and molding recipe suggestion for mold void enhancement. Lower EMC viscosity generated at higher flow rates, for the range of mold void improvement we proposed simulation results in our study.

1) *Through via diameter (mm):* 0.2mm of through via shows better performance of mold void result, 0.25 and 0.3mm results worse mold void in vent.

2) *Molding recipe:* the transfer time between over 15 sec and less than 15 sec is based on viscosity curve of reaction kinetics, keep an order within total processing time in molding it is seen that the value of viscosity has limited change due to the temperature of the time curving.

3) *Material between EMC-*A *and EMC-B:* in this work, we select a standard rules of an order to improve the mold void defect, but the key factor is through via was obviously.

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