Fan-Out Embedded Bridge with TSV (FO-EB-T) Package Solution for enhancing HPC application

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Abstract

No one can deny we are definitely in Artificial Intelligence (AI) generation as it's now immersing in all the necessities of our daily life, which effect and become every single part of our behavior. By accelerating the development of leading-edge assembly package combine with new generation high-bandwidth memory (HBM) that the speed can be even increased to 8Gbps, a much higher efficient AI chip can be achieved in enhancing the high-performance computing (HPC) application.

Assembly of Fan-Out Embedded Bridge (FO-EB) chiplet package adopts organic interposer with embedding bridge die which can be aggressively replaced by silicon bridge die with through-silicon-via (TSV) technology to be named as FO-EB-T. This 3D packaging removes the silicon interposer with the benefit of cost effectiveness and directly connects chips with different functions in the form of TSV. The high performance accommodates reducing package height, enhancing design flexibility, shortening the chip transmission path to reinforce chip operation speed. Besides, in order to effectively integrate different functions and process chips to meet the needs of high computing power, low latency, and low power consumption for Server AI computing, Self-driving cars, Networking etc., not only to breakthrough in packaging technology, but the methods of connecting chips and even the material used to connect will be the focus of technology development. In this paper, the selectivity study in terms of the interface connection is covered in pathfinding. The workability with integrated passive device (IPD) added was evaluated to verify the electrical voltage stabilization for package of FO-EB with TSV. Also, the module bonding on substrate method requirement for large Chip Module (CM) was studied as well.

Key words

HPC, Fan-Out Embedded Bridge (FO-EB), TSV, FO-EB-T.

I. Introduction

As silicon scaling closer to physical limit, future reduction of the gate oxide does not lower down the cost per transistor. But the demand of higher functionality and lower cost of electronic devices will never be coming to the end. What the electronic industries do is to break down a large die to a chiplet-based devices for improving yield and lower the total cost. Chiplet package thereby become a key technology to continue Moore's law. The multiple chiplet packages can be horizontally/vertically stacked on Si interposer using TSV (2.5D) or on an organic interposer to build up Fan-Out Multi Chip Module (FOMCM) and Fan-Out Embedded Bridge (FO-EB). In theory, the chiplet approach is a fast and less expensive way to assemble various types of third-party chips, such as I/Os, memory and processor cores, in a package. In order to further enhancing the power delivery and projecting the development of high-end GPU application, TSV (Through-Silicon-Via) is integrated to interconnection die or embedded bridge die to be named as FO-EB-T (FO-EB + TSV = FO-EB-T) as Fig. 1. This leading-edge package can be even formed as a heterogeneous integrated package (HIP), which can primarily fulfill the critical requirement of High performance computing (HPC) by the chip integration of high-bandwidth memories (HBM) and GPU or ASIC dies.

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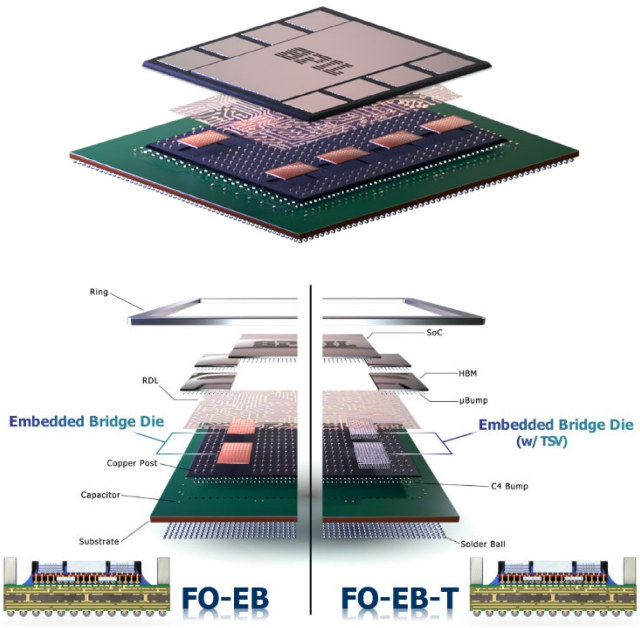

Fig. 1 FO-EB-T structure illustration

Moreover, the flow feasibility evaluation by ICD (Interconnected Die or bridge die) with TSV is critical in process capability development. The workability with numbers of IPD embedded for stabilizing voltage/current was evaluated as well.

II. Process development for ICD (Interconnection Die) w/ TSV (Sn connection vs. Cu connection).

In the launch stage of FO-EB-T, the process path finding by using different interconnection is considered. As shown in the process flow of Fig. 2. The build-up of ICD with TSV in different connection between the interface of ICD and C4 were generated.

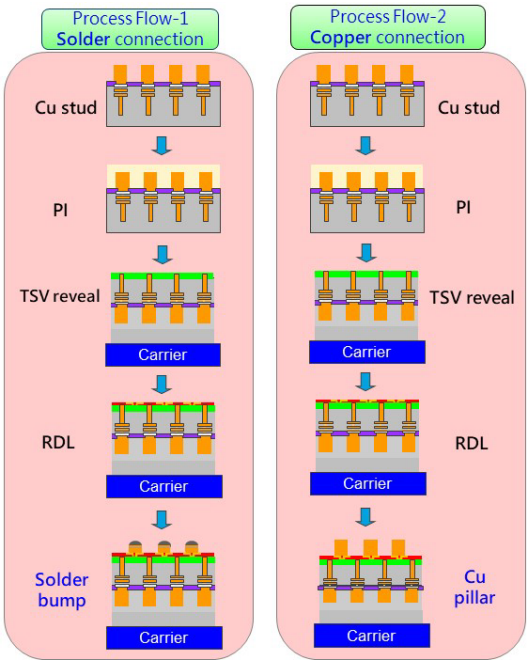

Fig. 2 Process flow ICD with TSV
(Solder connection vs. Copper connection)

Both flow-1 and flow-2 are same in the beginning steps, including firstly the bridge die with Cu stud was fabricated. Next to PI process is to let TSV revealed and then RDL stacked. The main different process stage is after RDL, the interface portion between ICD structure and C4 part. One in flow-1 is by Solder bump. The other in flow-2 is by Copper pillar/Cu stud. The Fig. 3 reveal the detailed stacked-up interface structure of ICD with TSV in the FO-EB-T package. In the solder bump connection, the u-pad is still needed along with the processing of Cu Post, which is for the joint of solder bump afterward. While the u-pad is unnecessary in Cu pillar connection.

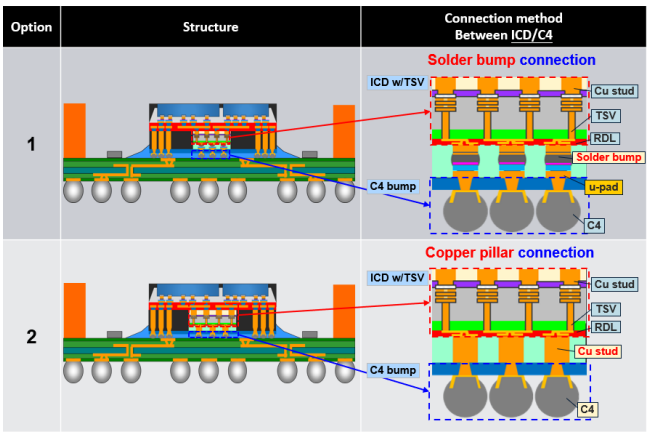

Fig. 3 ICD w/ TSV structure &
connection method between ICD/C4

In Cu connection feasibility study, the process DOE

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result still showed the problem of ICD die shift remaining, but the interface between TSV, ICD BS (back-side) & C4 are all in connected as described in side view and layer stacking layout of Fig. 4. However, the risk caused by not fully overlapped between the interface of ICD BS & C4 will be easily inducing crack since this unstable structure. The feasibility study by confirming the shift space and enlarging the bump size of ICD BS was evaluated. Further cross-section can be used for judging the join performance. It's even more accuracy by setting up O/S measurement pin to adjust the offset.

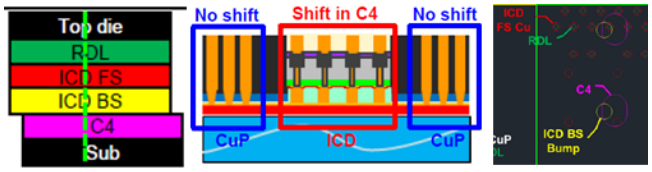

Fig. 4 Side view and layer stacking of TSV, ICD BS & C4

In short summary from workability and risk perspective, Solder connection is higher workable than Copper connection. Also, the risk level of Solder connection is low due to easier control by traditional die bonding while Copper connection is difficult to control via sidewall profile. That's certainly involve the added of cycle time and cost. The further confidence level for Solder bump connection is shown as Fig. 5 of reliability TCJ 3000x pass without IMC void.

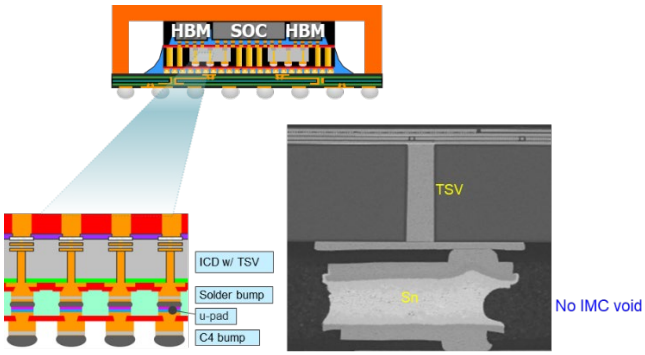

Fig. 5 TCJ 3000x pass on FO-EB-T w/ Sn bump connection.

III. Workability evaluation for stabilizing the voltage and current with IPD added.

In order to develop high-end GPU application and enhance power delivery, this cutting-edge FO-EB-T package was innovated bring out and with integrated passive device (IPD) added for the consideration of stabilizing the voltage and current. From the perspective of signal protection and AC noise reduction, the workability evaluation with numbers of IPD was put in design of experiment. As description of Fig. 6 showed the lateral structure of IPD embedded location, the design put IPDs in two area. One is within Molding-1, under RDL and between the location of ICD (bridge die). The other is located in Molding-2 of top dies (SOC / HBM) area and beside the component. From AC noise diagram result shown in Fig. 7[2]. If package FO-EB-T without IPD was set as baseline and with IPD as comparison, it's obvious that this evaluation with IPD added is able to gain positive

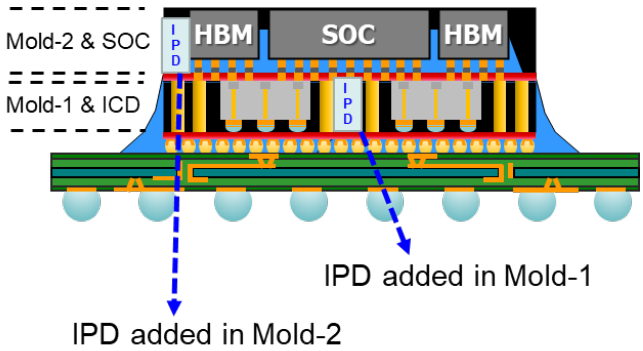

Fig. 6 Lateral profile of IPD embedded

improvement for AC noise. The in-house data showed it even can reach 40% AC noise reduction[4] and also concluded that the improvement % is rely on the distance between SOC to IPD. Namely IPD in Mold-1contribute more than IPD in Mold-2. This is critical message as well for stabilizing the voltage and current in design.

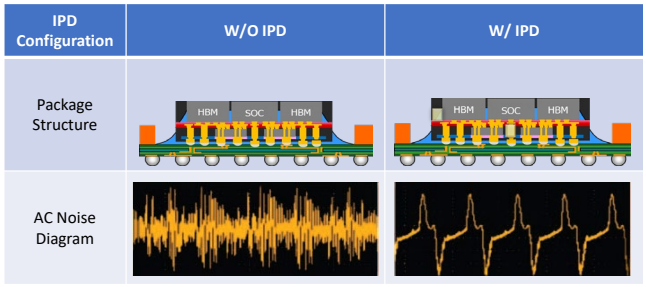

Fig. 7 AC noise improvement with IPD added

In addition to evaluate the workability with numbers of IPD, this study also checked the chip module (CM) warpage performance with HBM (real/dummy) and IPD/passive

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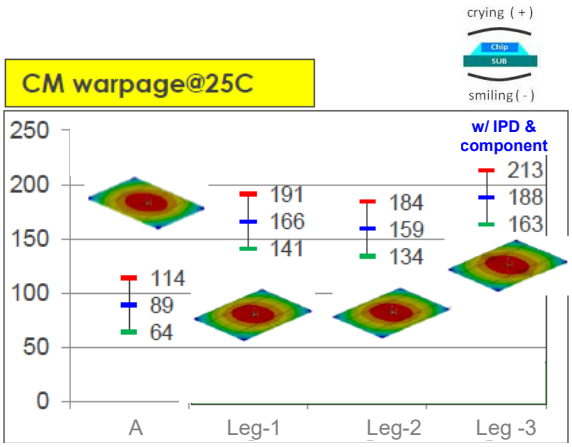


Fig. 8-1 CM warpage performance(@RT) with HBM and IPD/passive component embedded

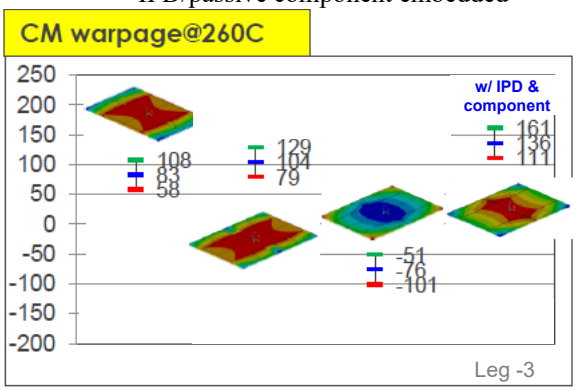


Fig. 8-2 CM warpage performance(@HT) with HBM and IPD/passive component embedded

component embedded as shown in Fig. 8. Leg-A is as baseline of FO-EB package compare to FO-EB-T package by leg-1, leg-2 and leg-3. Leg-1 is with real HBM type. Leg-2 is comparable using dummy HBM. Leg-3 had IPD and component embedded as well as real HBM. Moreover, the package size for both test vehicles of FO-EB and FO-EB-T are all around 5500 mm2 with a chip module size around 3000mm2.

Three warpage behaviors in FO-EB-T have been found in Fig. 8 of CM warpage performance. Firstly, warpage trend to worse than FO-EB due to GPU size is enlarged. Secondly, adding IPD and component would induce higher CM warpage due to larger CTE mismatch among IPD, component and EMC. Thirdly, Different CM warpage behavior between FO-EB-T w/ real HBM (Crying mode in HT) & dummy HBM (Bare Si, Smiling mode in HT).
Therefore, it's recommended to use real HBM for processing. On the other hand, the TCB (Thermal Compression Bond) have to be considered adopting to against warpage on big chip module size.

IV. AB2 DB method requirement evaluation for large Chip Module

One of process challenge in FO-EB-T is module warpage control. In order to fulfill the requirement of large GPU and accommodate the trending of great size Chip Module (CM), the machine handling and process capability of die bonding have to be enhanced to meet the specification.

The Moire's preliminary analysis showed that there is a great contrast between warpage at room temperature and high temperature for the structure of large-size chip module under layer-by-layer stacking. In addition to suppressing CM warpage through Jig optimization in traditional Die Bond (DB) + Mass Reflow (MR), it's also performed new technology development for DB and found that Thermal Compression Bond (TCB) is not limited by warpage on large-scale CM. TCB can effectively bond the CM to the substrate through stand-off height (SOH) control, and its cycle time performance is also equivalent to traditional DB.

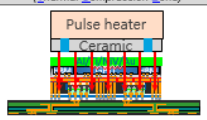
DB Method	MR (Mass Reflow)	TCB (Thermal Compression Bond)
★★★ Best ★★ Good ★ Bad Diagram		
Heater type	Air	Pulse
CM WPG control	★ (w/o compress)	★★★ (CM replacement w/ compress)
CM size	≦ ~1600 mm2	> ~3000 mm2
Throughput	1X	1X

Table 1. DB method_MR vs. TCB

The summary table for comparison of MR vs. TCB was showed as table 1. DB method_MR vs. TCB. Also, through the large-scale CM development of test vehicle, it defines the DB method (Fig. 8 DB selection rule) to be used in AB2 (CM bond on substrate process) corresponding to different CM sizes in the future.

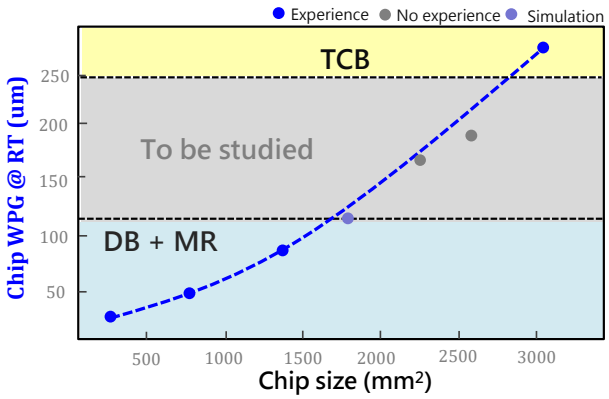


Fig. 8 DB Selection Rule

The CM of test vehicle was composed by 1 SOC and 8 HBMs together with TSV bridge dies. Along the way of the TCJ 3000x, u-HAST and HTSL were passed without delamination and crack found, FO-EB-T had demonstrated reliable structure [2]. As the key interface cross-section shown on Fig. 9, it reveals good joint on ubump, RDL, Cu Stud. NO any non-wetting and delamination found. The interface also showed the Cu Post and C4 bump are all in well adhesion and joint. All the positive result were proven that FO-EB-T should be a solid solution for high performance computing application.

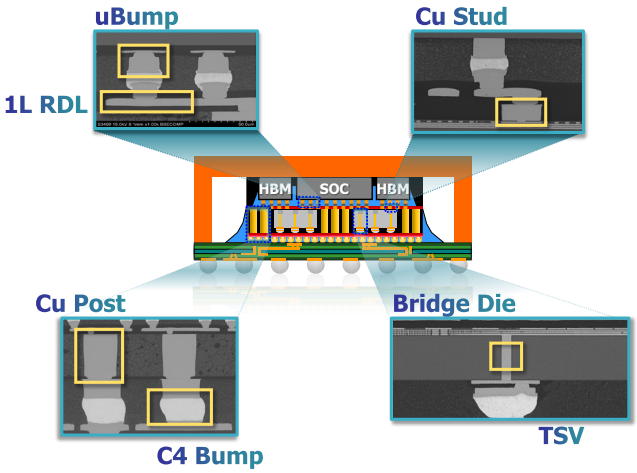


Fig. 9 FO-EB-T Readiness_key interface x-section

V. Conclusion

According to the investigation in this study, FO-EB-T package would suffer a lot of challenge during the process and reliability test due to the new die treatment process flow and new connection structure method between ICD/C4 in finding a reliable path. With lots of simulation support, FO-EB-T package would have a process warpage guidance to understand the scheme of HBM, IPD and component design-in. With the reliability verification collection, this study had completed the structure and process establishment of FO-EB + ICD with TSV as well as new technology development of AB2 DB and selection criteria for defining DB and CM sizes.

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