Megachip: An Advanced Packaging Solution for Chiplet Integration

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Abstract

We present our development of a novel heterogeneous chip-tiling approach that enables the realization of extremely large-area integrated circuits (ELAICs) or "Megachips"- containing tens of closely spaced small chiplets that are interconnected via redistribution layers (RDLs) fabricated using a lithographic process on top of the tiled chiplets. The concept of the Megachip approach is to interconnect small specialized chiplets, into a large, single-chip-like monolithic integrated circuit. Multiple heterogeneous chiplets can be interconnected within layers that redistribute, or reroute, the electrical inputs and outputs (I/O) to enable chiplet-to-chiplet (C2C) communication. This architecture relies on chip-like electrical traces having narrow line width (~1-2 µm) and close C2C spacing (~5-20 µm) to achieve high I/O density, high bandwidth, and low-latency circuits. A Megachip has a chip-like silicon content (about 99%), allowing highly stable and inexpensive fabrication of a heterogeneous system-on-chip with chip-like wiring densities. Megachip tiling with mix-and-match die is well suited to meet the high-end electronics requirement of smaller form factors, higher performance, and increased packaging flexibility.
Key words: chiplets, heterogeneous integration, Megachip, ELAIC, parallel interfaces.

I. INTRODUCTION

The saturation of Moore's law-related lithographic scaling in high-density semiconductor integrated circuits has greatly impacted the energy-efficient system design required to provide an increasing computing capability for our data-intensive future. Advanced packaging architects are exploring heterogeneous assemblies of specialized chips (called "chiplets") as an alternative way (i.e., "More-Than-Moore") to meet the computing demands of increasing power and performance in ever-smaller packages. **Figure 1** shows advanced packaging trends for heterogeneous chiplet integration. There is a need to develop advanced packaging architecture-based approaches to bridge the gap between back-end of line (BEOL) wafer fabrication and bump/µbump based advanced packaging. To accomplish this, new packaging technology requires accommodating more chiplets with smaller chip-to-chip distances and higher I/O densities while being pushed into smaller form factors and higher heat dissipation. Consequently, the packaging industry is moving toward lithographical (bumpless) approaches as solutions for tiling more chiplets into a single package. Tiling tens to hundreds of known-good chiplets near one another and creating a chip-like lithographical wiring (e.g., BEOL) and chip-like silicon content (i.e., no-gap assembly) are highly desirable for creating next-generation parallel interfaces with very short channel interconnects between chiplets to achieve high bandwidth, low latency, and heterogeneous computing architectures. However, this has yet to be demonstrated. Herein, we report the implementation of such a chiplet-based tiling approach for parallel architectures **[1]**.

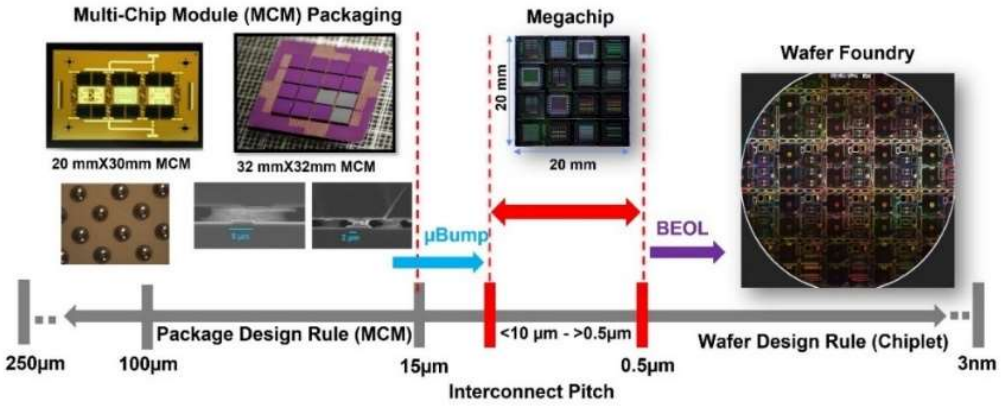

Figure 1. The extremely large-area integrated circuit (ELAIC), also referred to as a "Megachip," bridges the gap between advanced packaging (e.g., bump and µbump based multi-chip module [MCM]) and backend-of-line (BEOL) wafer fabrication. The Megachip concept [**1**] uses a bumpless lithographical approach to interconnect chiplets.

Over the years, many integration approaches such as Si-interposers (2.5D) with redistribution layers (RDLs)[**2**], Si-interconnect fabric[**3-4**], 3D chip stacking[**5**], bridge chip[**6-7**], embedded dies within package substrate**s** [**8-9**], embedded multi-die interconnect bridges (EMIB)[**10-11**], wafer-level packages (WLP)[**12-15**] and panel-level packages (PLP)[**16**] have become the preferred packaging technologies to support high-speed serializers/deserializers (SerDes) or parallel architectures to meet the requirements of higher functionality in ever-smaller packages, particularly when coupled with the use of different technology node chiplets. System-level multi-chiplet integration has also emerged [**17**] to mitigate the growing concerns regarding the yield and cost of small process node chiplets. These approaches include multi-die system-on-chip (SoC) [**18**], system-in-package (SiP)[**19-20**], SiP-interposer-SiP[**21**], and package-on-package solutions[**22**].

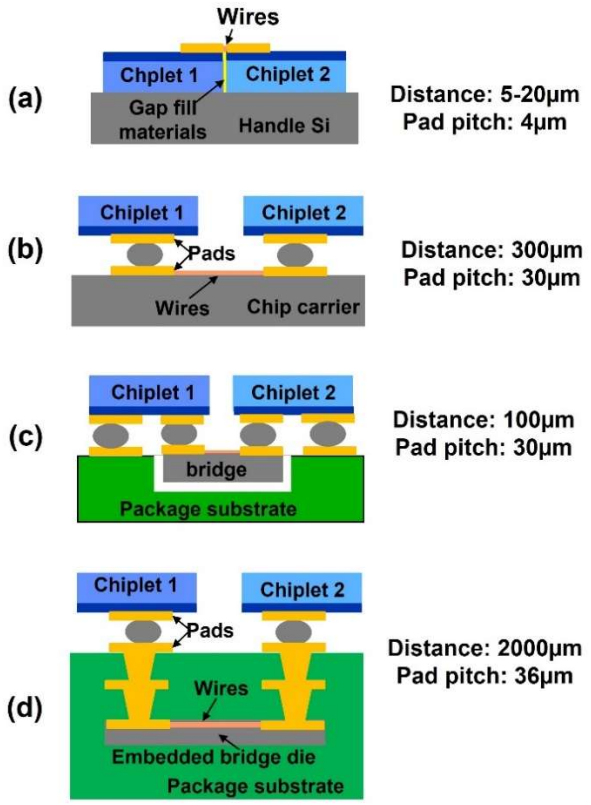

Figure 2: Cross-sectional view schematics of ELAIC Megachip and traditional advanced packaging: (a) Megachip reconstruction scheme with 5−20 µm C2C communication distance and 4 µm I/O bond pad pitch, (b-c) 2.5D technology and bridge die scheme with 100-300 µm communication distance and 30 µm bond pad pitch, and (d) embedded die interconnect bridge scheme with 2000 µm communication distance and 36 µm bond pad pitch. For 2.5D(fig.2b) and bridge die(fig.2c), 100-300 µm communication distance assumption based on die-to-die separation + keep out zone from die edge to bump + bump height. For embedded die interconnect bridge (fig. 2d), 2000 µm C2C communication distance based on 2mmX6mm embedded die + substrate via length + solder bump height. Figures **a-d** show the advantage of parallel interface for Megachip reconstruction over 2.5D, bridge die, and embedded die interconnect bridge approaches. The Megachip schematic shows a smaller interconnect length and smaller pad pitch, leading to an order/orders of magnitude improvement in speed (speed = 1/total wire delay) and bandwidth density (bandwidth density: bump density*speed) over the traditional advanced packaging approach [**23**].

This paper describes a novel heterogeneous multi-chiplet tiling approach that enables the realization of an extremely large-area integrated circuit (ELAIC), which we also refer to as a "Megachip," containing tens to hundreds of closely spaced small chiplets interconnected to create systems that perform as a single-chip monolithic device, despite being composed of many smaller heterogeneous chiplets [**1**]. **Figure 2** shows a schematic comparison (e.g., chip-to-chip spacing and pad pitch) between the ELAC Megachip and the traditional best-competing advanced packaging technology. For parallel interfaces, the ELAIC Megachip with narrow gaps (5-20 µm) and a small I/O pitch (2–10 µm) between the chips is a better solution for chip-to-chip communication than 2.5D and bridge technology. A 10 to 100 times reduction in interconnect length/delay/latency and 5-10X smaller interconnect pitch can create a more energy-efficient system.

II. RESULTS AND DISCUSSION

Figure 3 illustrates the Megachip reconstruction process. A 20 mm X 20 mm single chip was diced into sixteen 5 mm × 5 mm chiplets, the bad chiplets were replaced, and the 20 mm X 20 mm single artificial chip was reconstructed using the ELAIC Megachip tiling approach (**Figure 3a-c**). Scanning electron microscopy (SEM), confocal scanning, X-ray, and optical images were used to evaluate the key fabrication/assembly steps, including the inter-chip spacing and planarity, RDL dielectric deposition, via formation, critical feature size, and micro-bumping (**Figure 3d-f**). **Figure 3d** shows the inter-chip spacing between stealth diced chips in the 16-chip ELAIC assembly. The SEM data indicate that the ELAIC fabrication process maintains a narrow gap of 5-20µm between chips. Appropriate cleaning to remove dicing debris, smooth chip edges, and minimize chipping is critical for reducing the chip-to-chip spacing. **Figure 3e** shows an SEM micrograph of fine line circuits deposited on the ELAIC surface. SEM shows 2µm lines and spaces. Lithographically, we can achieve finer line circuits down to 0.8-1 µm lines on the ELAIC surface. This type of fine-line circuit supports a chip-like wiring.

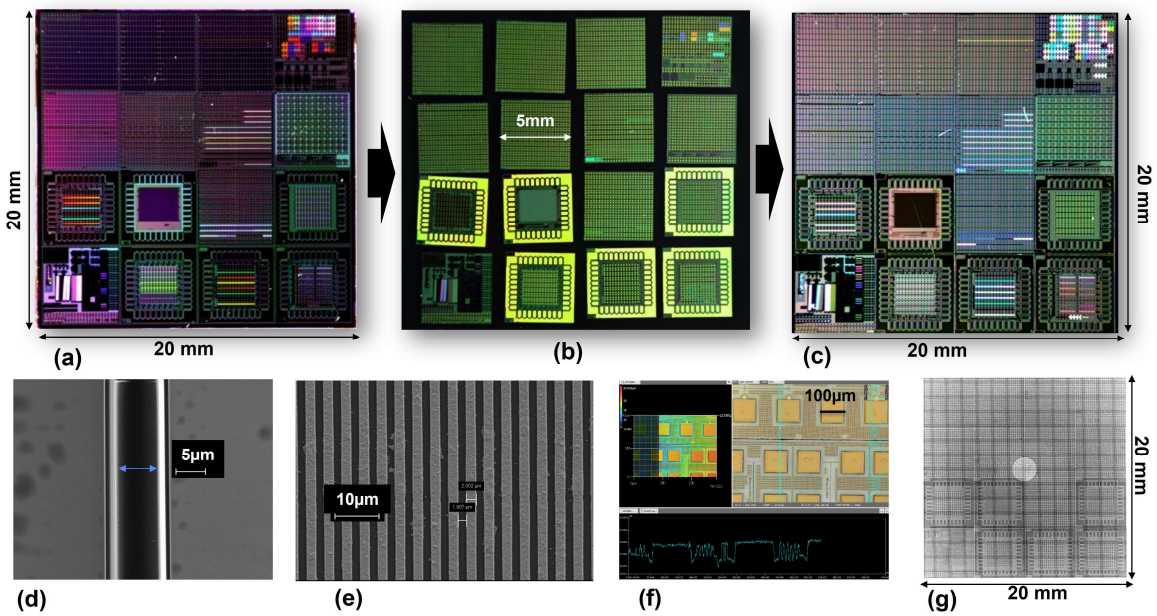

Figure 3. (a) 20 mm × 20 mm single chip prior to dicing, (b) 20 mm × 20 mm single chip diced to sixteen 5 mm × 5 mm chiplets. (c) After damaged chiplets are removed and replaced, the Megachip is reconstructed using known good chiplets. (d) Megachip inter-chiplet spacing (SEM micrograph), (e) SEM micrograph of fine-line circuits on Megachip surface, (f) confocal microscope Z-height scan to measure inter-chiplet co-planarity, and (g) X-ray image of a 20-mm x 20-mm ELAIC Megachip formed by recombining the sixteen 5-mm x 5-mm chiplets into single chip like structures. This image is comparable to single chip X-ray image. The megachip has narrow inter-chiplet spacing (d), chip-like interconnects (e), chip-like inter-chip planarity (f), and chip-like silicon content (g) to support Megachip's tiling; reconstruction produces circuits similar to an undiced monolithic single chip circuit.

Figure 3f shows a representative confocal image of the ELAIC module measured using a 100 nm resolution in the z-axis. Confocal line scans show the Z-height variation along the line as it scans from one chip to another. It is clear from the data that the fabrication process maintained a chip-like inter-chip planarity . We used X-ray imaging to inspect a single chip before dicing and the ELAIC Megachips. The X-ray images of a single chip and ELAIC appear similar [**1**]. Dicing a single chip removes Si from the dicing lane, resulting in a smaller metal-to-metal gap between chips, as shown in the ELAIC X-ray image (**Figure 3g**). Overall, the ELAIC fabrication process produces a highly compact (>99% Si content) chip assembly with 5-20 micron spacing between the chips, and maintains chip-like inter-chip planarity, which is required for finer lines and smaller interconnect lengths for parallel interface with wide I/O, high bandwidth, and low-latency chip-to-chip communication. We developed a variety of ELAIC assembly approaches to optimize the critical alignment between chips. For example, ELAIC devices use an optical or high-resolution microscope for chip-to-chip alignment and an interlock (i.e., LEGO-like) approach to maintain the post-process alignment accuracy. The gap fill and chip surface planarity allowed the selection of various dielectric materials (e.g., PECVD oxide, BCB, silicone, and polyimide) for deposition on the ELAIC surface.

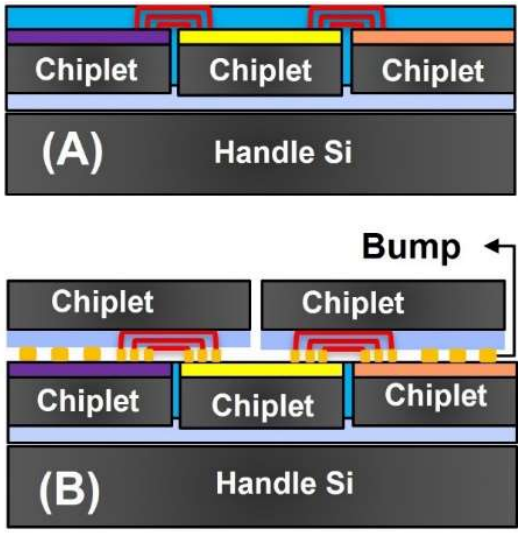

Figure 4:ELAIC Megachip parallel interface concept to minimize chiplet-to-chiplet interconnects distance. **(A)** Lithographically defined interconnects for chiplet-to-chiplet communication. **(B)** Flip-chip integration for parallel interface. Here flip-chip die provides interconnects for parallel interface similar to traditional packaging.

We are currently developing two parallel interface approaches for Megachip (**Figure 4)**. One uses a lithographically defined interconnect (**Figure 4a**) and the other uses a flip-chip bridge die (**Figure 4b**). The lithography approach extends the number of chiplet tiles within a given space by enabling a sufficiently high chiplet-to-chiplet connectivity to allow multiple chiplets to perform as a single-chip monolithic device. Connecting chiplets through the lithographic approach provides high-density interconnects localized between adjacent chiplets, thus enabling a path to increase the bandwidth (Gbps/mm), reduce latency and energy (pJ/bit) consumption. However, connecting chiplets through the flip-chip bridge die process enables an increase in the format size of heterogeneous systems with a reworkable interconnect fabric to address the significant challenges for a scalable computing platform.

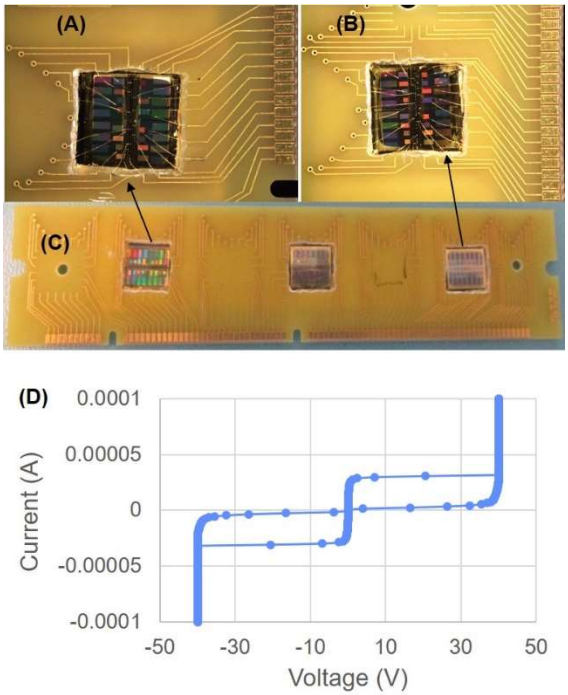

Figure 5: Active circuit demonstration. Figure shows three 10 mm X 10 mm ELAIC samples attached to the circuit card. ELAIC module consists of 4 active devices containing superconducting junctions. These ELAIC devices used PECVD silicon dioxide as dielectric and Ti-Au interconnections for chip-to-chip connection. (A-B) An optical image of 10 mm X 10 mm ELAIC is attached to the circuit card for cold testing. (C) Three 10 mm X 10 mm ELAIC samples were attached to the circuit card for cold testing. (D) I-V curves were used to characterize the switching behavior of JJ-arrays connected through Nb and gold lines. The I-V characteristics of JJ series arrays with up to 20,000 JJs per chip with a drawn JJ diameter of 0.7 µm.

As the next step in chip tiling using a lithographical approach (**Figure 4A**), we investigated both the PECVD oxide and BCB as redistribution layers. We used single and double metal layers for circuit demonstration. Various chips with dimensions of 5 mm X 5 mm, 10 mm X 10 mm, and 20 mm X 20 mm were used to evaluate the circuit demonstration. We used following electrical characterizations to evaluate Megachip fabrication and assembly:

A single metal-layer passive circuit was demonstrated on top of a tiled assembly consisting of sixteen 5 mm X 5 mm-chips. We measured room temperature (RT) resistance of 1-10-µm wide, 5-20-mm long circuit traces between the chips on top of the 16-chip assembly. Additionally, four 10 mm X 10 mm and four 20 mm X 20 mm chip-based ELAIC Megachips were assembled to evaluate single metal layer passive circuits.

A passive daisy chain circuit was demonstrated on top of a 16-chip ELAIC assembly. Two metal-layer daisy chain circuits were created using a multi-layer BCB dielectric. The RT resistance of a passive daisy chain circuit supports a microvia chain through multi-layer BCB[**1**].

Megachip assembly further investigated the interconnection between active chips containing trilayer Josephson Junctions (JJs) for larger system applications, such as quantum processors, readouts, control, and amplifier chips. Active chips can be interconnected to create a multi-die system on a chip. These JJs/active components may be on the same chip or on separate chips assembled on the ELAIC platform. In either case, the first step toward assessing the ELAIC structure with Nb/Al-AlOx/Nb trilayer junctions is to determine the impact of fabrication on the trilayer junction performance. The addition of RDL/build-up layer fabrication to the junction chip may change the critical current, subgap voltage, and other junction properties. In addition, multiple chip assemblies, gap filling, and planarization may affect the stability and junction performance at 4 K. To quantify the effects of fabrication on the trilayer junction, we fabricated an ELAIC assembly (**Figure 5**), in which multiple superconducting chips with trilayer junctions were attached to a single large ELAIC. This allowed us to determine the impact of ELAIC fabrication on the junction characteristics and demonstrate the basic desirable functionalities of multi-die SoCs.

Figure 6 shows sixteen 5 mm × 5 mm lithographically interconnected Josephson Junction (JJ)chip assemblies. This indicates that the circuit traces moved between the chips to interconnect JJ chains. **Figure 6A** shows a representative confocal image of a 16-chip ELAIC. We used a BCB-PECVD oxide dielectric and lithographically interconnected 16-chip ELAIC Megachip. **Figure 6B** shows the optical image of a 16-chip interconnected ELAIC assembled into a

circuit card to measure the I-V curve at room temperature (RT) and 4 K. **Figure 6C** shows the RT I-V resistances for various sections with different numbers of JJ chains of interconnected ELAIC circuits. ELAIC circuit consists of JJ chain, niobium (Nb) trace and Ti/Au traces. Ti/Au vias and traces were used to connect the adjacent JJ chain chips. Nb was resistive at RT. The JJ chain length and associated Nb interconnect dictate the total resistance variation in the individual circuits. Future work will include a fully interconnected Megachip Junction analysis at cryogenic temperatures.

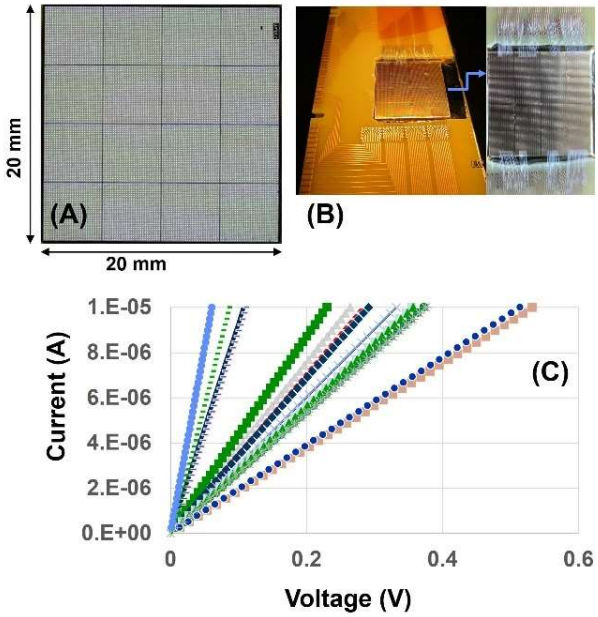

Figure 6: Circuit demonstration of 16-interconnected chip assembly. Figure represents single metal layer passive circuits interconnecting 16 superconducting test chips. (A) Confocal image of sixteen 5 mm X 5 mm chip ELAIC Megachip, (B) optical image of 16 chip ELAIC wirebonded to circuit card, (C) Room temperature I-V plot of 16-interconnected chip ELAIC circuit resistance for different sections. Resistance variation is due to the different widths and lengths of circuits.

In another example, we used a bumped 16-chip ELAIC and flip-chip bridge dies instead of lithography for the interconnection. **Figure 7** (A-C) shows the process flow for interconnecting ELAIC using bridge dies. Each bridge die can interconnect to four nearest-neighbor sections. Initially, we used nine active flip-chip bridge die-interconnected 16-chip ELAIC assemblies (**Figure 7C**) to fabricate active-to-active reworkable large-area circuits. This tiling approach follows the flip-chip bump bonding approach described in **Figure 4B**. Bump-bonded ELAIC Megachip circuits were wire-bonded to the circuit card (**Figure 7D-E**) to measure the I-V curves at RT and 4 K. The initial RT I-V resistance revealed good chip-to-chip connectivity. Cryogenic testing is currently in progress. The Megachip approach uses a reworkable flip-chip bridge die approach (described in **Figure 4B**), which supports the tiling of hundreds of chiplets to create a larger-format reworkable system.

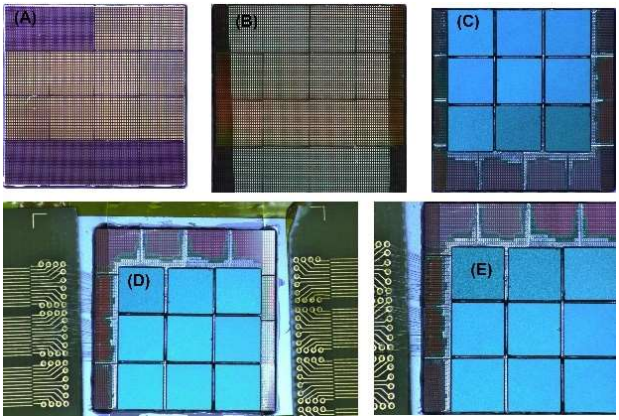

Figure 7: Flip-chip circuit demonstration on top of 16-chip ELAIC assembly. (A) Lithographically defined resist opening for micro-bump deposition to individual 16 chip assembly, (B) micro-bump deposited on ELAIC surface. Here, perimeter chips are partially bumped to access the perimeter chip pad for wire bonding to measure the I-V curve at RT and 4K.(C) 9 chip flip-chip bonded to 16 chip ELAIC surface to interconnect between the chips, and (D-E) Bump-bonded ELAIC wire-bonded to circuit card for connectivity test.

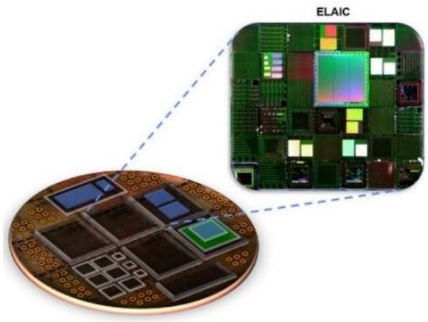

Figure 8: System-on-Wafer (SoW) schematic include ELAIC as part of wafer-scale architecture.

III. FUTURE PACKAGING TRENDS

As we look further out, larger MCMs, chiplets, 2D-2.5D-3D-HBM combination with reworkable micro-bump assemblies will be considered for unique miniaturized advanced packaging solutions. As an option, wafer-scale multi-chip modules (**Figure 8**) can laterally connect ELAIC, chiplets, processor, and memory chips (with or without interposers) with integrated-circuit-scale electrical routing between the

chips and MCM to create system-on-wafer (SoW). This scheme uses wafer-scale MCMs to route power and signals from one chip to another through micro-bump interconnections.

Megachips use parallel interfaces for chiplet-to-chiplet communication within a megachip. We used a bumped Megachip for the Megachip-to-Megachip communication. A bumped Megachip can be directly attached to a wafer (**Figure 8 and 9**) or a package substrate (**Figure 10**). This simplifies the integration approach by eliminating multilevel assembly (2.5D, 3D, HBM, stacked package, etc.) and using a standard universal chiplet interconnect express (UCIe), PCIe (peripheral component interconnect express (PCIe), or embedded bridge die (**Figure 10**) for short (a few millimeters to centimeters) reach communication. For long-reach communication, the ELAIC can use optical and photonic interconnects. A bumped Megachip can use parallel interfaces for Megachip-to-Megachip communication on wafer-scale computing platforms (**Figure 9**). Handle Si of the ELAIC Megachip (**Figure 10**) can have built-in package-level microchannels for liquid cooling lids to address thermal challenges across a broad range of applications.

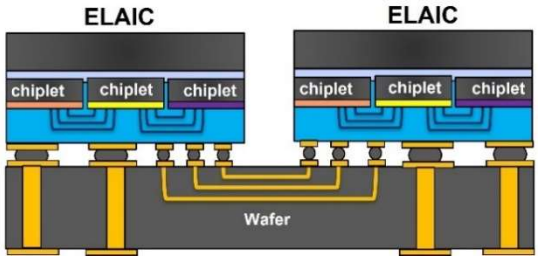

Figure 9: Parallel interfaces for ELAIC-to-ELAIC communication. Parallel interfaces can be used for wafer-scale systems for ELAIC-to-ELAIC or ELAIC-to-chip communication.

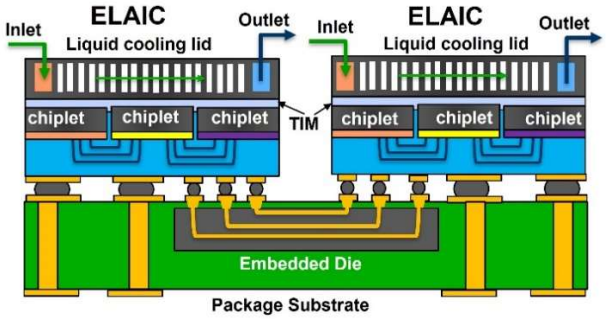

Figure 10: Parallel interfaces for ELAIC-to-ELAIC communication. We can use embedded die within a package substrate for parallel interfaces for ELAIC-to-ELAIC or ELAIC-to-module communication.

We assembled various ELAIC Megachip configurations using 5-mm x 5-mm to 20-mm x 20-mm chips in order to test the chip surface planarity, chip-to-chip spacing, and flip-chip integration. **Figure 11** shows various ELAIC Megachips in 2D and 3D configurations as representative examples. The figure shows nine 5 mm × 5 mm chips (Figure 11B), thirty-nine 5 mm × 5 mm and 10 mm × 10 mm chips (Figure 11C) and two hundred fifty-six (256) 5 mm × 5 mm chip assemblies (Figure 11D) to create a 2D ELAIC array. Flip-chip bonding using a 2D array can be used to create a 3D array of chip assemblies. For example, flip-chip bonding of 20 mm X 20 mm Si-chip with sixteen 5 mm X 5 mm chip-based ELAIC Megachip assembly (Figure 11E) provides a solution to fabricate large-area imagers [**1**]. Similarly, flip-chip bonding with multiple bridge dies with a sixteen 20mmX20mm chip-based ELAIC Megachip assembly (Figure 11F) provides a solution to interconnect a large area (80mmX80mm) circuit.

IV. CONCLUSIONS

Our novel heterogeneous chip tiling is a transformative approach that enables the fabrication of heterogeneous Megachips with tens to hundreds of chiplets interconnected via BEOL-like lithography or a flip-chip bridging process. Megachip technology provides increased I/O density and reduced interconnect length between chiplets for high-bandwidth, low-latency parallel interfaces. This lithographical integration technology enables the creation of advanced heterogeneous Megachip structures that address the need for increased chiplet integration in emerging computing (e.g., AI, HPC, servers), mobile, and networking applications.

Megachip addresses two challenges in the semiconductor industry: expanding next-generation chiplet integration options, and reducing integration costs and the time needed to develop chiplet based systems. The potential for mix-and-match IC schemes will serve as a critical advantage that will provide yield enhancements, and power and performance benefits for many high-end electronic systems.

Megachip circuits can be useful for aggressive interconnect pitch scaling of a parallel interface with more physical wires within a given area for true process node interchangeability. Furthermore, Megachip provides an integrated heat sink (i.e., a built-in package lid with microchannels) that allows for a superior cooling capability for high-power systems. Thermally efficient Si floor plan for higher power density multi-die SoC design. This allows active-to-active bonding (mix-and-match chiplets), thin bond-line thickness thermal interface material (TIM), reduced chiplet-to-chiplet thermal resistance, and thermal crosstalk between neighboring chiplets.

Ultimately, the ELAIC Megachip solution will allow for a wide trade space in terms of cost and partitioning for each application, and will carve out a path toward large-scale heterogeneous fabrication. For example, Megachips can have chips/chiplets from different foundry processes and different technology nodes to improve mix-and-match capabilities and package performance. It also provides scalability for placing many chips on the ELAIC platform and designing it to package many different functionalities together, thereby demonstrating that it is a viable approach for building larger systems.

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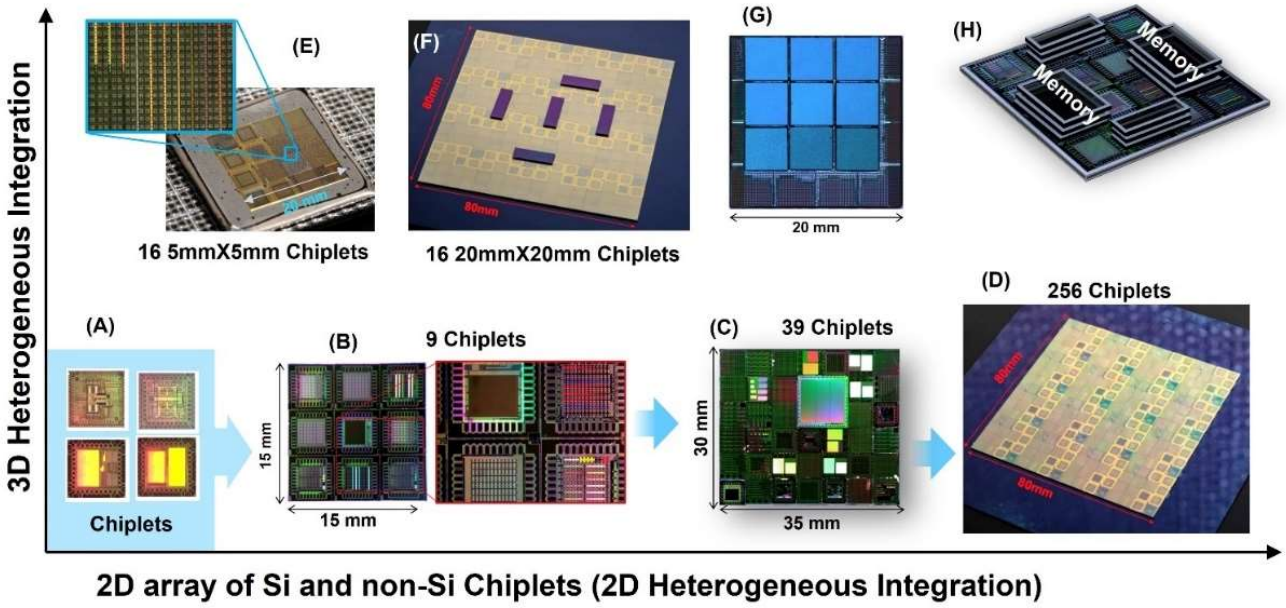

Figure 11: ELAIC Megachip overview. Application of ELAIC Megachip in 2D, 2.5D and 3D space. The ELAIC Megachip circuit combines known good die together to make systems that perform like an extremely large single chip. Figure shows scalability of the ELAIC fabrication process, with assembly sizes ranging from 9 chips to 39 chips to 256 chips. (A) Four 5-mm x 5-mm known good chiplets prior to ELAIC assembly. (B)Nine 5-mmX5-mm chip ELAIC assembly and enlarge view of 9 chip assembly. (C) 5-mmX5-mm and 10-mmX10-mm chip assembled together to create 39 chip ELAIC Megachip. (D) Two hundred fifty six (256) 5-mm x 5-mm chip assembly. (E) Flip-chip ELAIC Megachip. 20-mm x 20-mm 16 chip ELAIC assembly flip-chip bonded to Si-die and underfilled to make a flip-chip ELAIC, Si etched from flip-chip die and stop at oxide surface of flip-chip die. Figure shows Si-less flip-chip ELAIC Megachip and corresponding enlarged image looking through the oxide surface. (F) 80-mm x 80-mm ELAIC Megachip. Sixteen 20-mm x 20-mm chips flip-chip bonded to bridge die to create 80-mm x 80-mm ELAIC Megachip. Next step: remove Si from flip-chip bridge die (similar to Figure 11E) and stop at oxide layer. Si-less bridge die interconnect with 2-6 µm layer thickness, necessary for creating the finer pitch ELAIC assembly. (G-H) Active -to-Active bonding for making various flip-chip (G), 2.5D,3D and HBM (H) configuration.

REFERENCES

[1] R. N. Das *et al*., "Extremely Large Area Integrated Circuit (ELAIC): An Advanced Packaging Solution for Chiplets," *2023 IEEE 73rd Electronic Components and Technology Conference (ECTC)*, Orlando, FL, USA, 2023, pp. 258-265, doi: 10.1109/ECTC51909.2023.00051.

[2] J. Sharda, M. Manley, A. Kaul, W. Li, M. Bakir and S. Yu, "Thermal Modeling of 2.5D Integrated Package of CMOS Image Sensor and FPGA for Autonomous Driving," *2023 7th IEEE Electron Devices Technology & Manufacturing Conference (EDTM)*, Seoul, Korea, Republic of, 2023, pp. 1-3, doi: 10.1109/EDTM55494.2023.10102948.

[3] S. Jangam, A. A. Bajwa, K. K. Thankkappan, P. Kittur and S. S. Iyer, "Electrical Characterization of High Performance Fine Pitch Interconnects in Silicon-Interconnect Fabric," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2018, pp. 1283-1288, doi: 10.1109/ECTC.2018.00197.

[4] S. Jangam and S. S. Iyer, "Silicon-Interconnect Fabric for Fine-Pitch (≤10 μm) Heterogeneous Integration," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 5, pp. 727-738, May 2021, doi: 10.1109/TCPMT.2021.3075219.

[5] Y. Zhang, X. Zhang and M. S. Bakir, "Benchmarking Digital Die-to-Die Channels in 2.5-D and 3-D Heterogeneous Integration Platforms," in *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5460-5467, Dec. 2018, doi: 10.1109/TED.2018.2876688.

[6] https://www.3dincites.com/2021/07/iftle-491-ibm-simplifies-si-bridge-technology/

[7] H. Braunisch, A. Aleksov, S. Lotz and J. Swan, "High-speed performance of Silicon Bridge die-to-die interconnects," *2011 IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems*, San Jose, CA, USA, 2011, pp. 95-98, doi: 10.1109/EPEPS.2011.6100196.

[8] R. N. Das, F. D. Egitto, B. Bonitz, M. D. Poliks and V. R. Markovich, "Package-Interposer-Package (PIP): A breakthrough Package-on-Package (PoP) technology for high end electronics," *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, Lake Buena Vista, FL, USA, 2011, pp. 619-624, doi: 10.1109/ECTC.2011.5898577.

[9] R. N. Das *et al*., "Fabrication and electrical characterization of embedded actives and passives for system level analysis: Toward Size, Weight and Power (SWaP) reduction," *2012 IEEE 62nd Electronic Components and Technology Conference*, San Diego, CA, USA, 2012, pp. 1593-1598, doi: 10.1109/ECTC.2012.6249049.

[10] L. P. Tan, S. S. Lee and K. H. Wong, "Design and Implementation of EMIB Testing on 2.5D FPGA Transceiver," *2016 IEEE 25th Asian Test Symposium (ATS)*, Hiroshima, Japan, 2016, pp. 127-127, doi: 10.1109/ATS.2016.62.

[11] R. Mahajan *et al*., "Embedded Multi-die Interconnect Bridge (EMIB) -- A High Density, High Bandwidth Packaging Interconnect," *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, USA, 2016, pp. 557-565, doi: 10.1109/ECTC.2016.201.

[12] C. Tseng, "InFO (wafer level integrated fan-out) technology" 66th Electronic Components and Technology Conference (May 2016), pp. 1–6.

[13] A. Cardoso, L. Dias, E. Fernandes, et al. (2017). "Development of novel high density system integration solutions in FOWLP-complex and thin wafer-level SiP and wafer-level 3D packages. 67th Electronic Components and Technology Conference (May 2017), pp. 14–21

[14] Fan-out Wafer-level-Packaging *Edited by* John H. Lau Springer ISBN 978-981-10-8883-4 ISBN 978-981-10-8884-1 (eBook) https://doi.org/10.1007/978-981-10-8884-1

[15] Advances in Embedded and Fan-Out Wafer-Level Packaging Technologies *Edited by Beth Keser and Steffen Kroehnert, WILEY 2019,* https://lccn.loc.gov/2018034374

[16] T. Braun *et al*., "Panel Level Packaging - A View Along the Process Chain," *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, USA, 2018, pp. 70-78, doi: 10.1109/ECTC.2018.00019.

[17] Rabindra N. Das, Frank D. Egitto, John Lauffer, Barry Bonitz, Bill Wilson, Francesco Marconi, Mark D. Poliks, and Voya R. Markovich, "3D-Interconnect Approach for High End Electronics," *IEEE Electronic Components & Technology Conference Proceedings*, 2012, 1333-1339.

[18] R. Viswanath, A. Chandrasekhar, S. Srinivasan, Z. Qian and R. Mahajan, "Heterogeneous SoC Integration with EMIB," *2018 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, Chandigarh, India, 2018, pp. 1-3, doi: 10.1109/EDAPS.2018.8680869.

[19] R. N. Das, F. D. Egitto, J. M. Lauffer, E. Chenelly and M. D. Polliks, "Versatile Z-axis interconnection-based coreless technology solutions for next generation packaging," *2013 IEEE 63rd Electronic Components and Technology Conference*, Las Vegas, NV, USA, 2013, pp. 1728-1733, doi: 10.1109/ECTC.2013.6575808.

[20] R. N. Das *et al*., "Resin coated copper capacitive (RC3) nanocomposites for system in a package (SiP): Development

of 3-8-3 structure," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 591-598, doi: 10.1109/ECTC.2009.5074073.

[21] Rabindra N. Das, F.D. Egitto, S.G. Rosser, E. Kopp, B. Bonitz, R. Rai, "3D Integration of System-in-Package (SiP) Using Organic Interposer: Toward SiP-Interposer-SiP for High-End Electronics" *46th International Symposium on Microelectronics (IMAPS)*, 531-537(2013).

[22] A. Yoshida, J. Taniguchi, K. Murata, M. Kada, Y. Yamamoto, Takagi, et al., "A Study on Package Stacking Process for Package-on-Package (PoP)", *Electronic Components and Technology Conference (ECTC)*, May 2006, ISSN 0569-5503.

[23] C. C. Hu, M. F. Chen, W. C. Chiou and D. C. H. Yu, "3D Multi-chip Integration with System on Integrated Chips (SoIC™)," *2019 Symposium on VLSI Technology*, Kyoto, Japan, 2019, pp. T20-T21, doi: 10.23919/VLSIT.2019.8776486.