Laser Assisted Bonding for Flip Chip Interconnection of Very Large Chips

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Abstract

In recent years, laser-assisted bonding (LAB) has emerged as a promising means to address specific flip-chip assembly issues associated with conventional mass-reflow (MR) and thermo-compression bonding (TCB) processes, for example chip warpage reduction. However, studies have predominantly focussed on small to medium sized chips. For memory, processor, and interposer applications, chip sizes may be much larger. The ability to effectively distribute laser energy across such larger interconnection areas is practically unexplored.

This paper investigates LAB behavior for a 25mm x 26mm silicon chip comprising Cu pillar/SAC solder interconnects, with a particular focus on the size of the optically generated homogeneous laser beam.

A heat transfer study was first conducted to estimate the relationship between chip surface temperature, which can be measured and controlled during the LAB process, and actual joint temperature, the latter requiring a special thermocouple assembly module. The responses allowed the determination of an appropriate range of LAB profile parameters for assembly development.

Assembly results reported revealed that beam size extension beyond the chip region is critical to achieving repeatable defect-free interconnection of such large chips. This relationship was additionally supported by thermal finite element modelling (FEM) that demonstrated that the impact of convective effects at the chip periphery on solder joint temperature distribution, and remediation of same by beam size enlargement, became increasingly important with increasing chip size. It was further demonstrated that, despite the larger beam size and its effect on substrate surface temperature, post assembly chip warpage was reduced by about 50% using LAB as compared to the MR process. Finally, microstructural comparisons between LAB and MR validated that initial intermetallic compound (IMC) formations are significantly reduced on these large chip assemblies, in line with previous studies on smaller chips.

Key words: Laser-assisted bonding, flip-chip, solder, large chip, beam size, thermal simulation.

I. Introduction

The mass reflow (MR) process, where the entire assembly is uniformly heated in a convection type reflow furnace, is most commonly used in industry for chip interconnection due to its high productivity and the self-aligning effect of solder joining [1], [2]. Unfortunately, this approach is not without issues. First, the organic substrate is free to warp, which can cause mis-alignment and assembly defects such as non-contacts or bridging. Initial substrate warpage becomes more significant with coreless substrates, which are used for optimal cost-performance. This problem is further exacerbated as chips become larger and their interconnection geometries become smaller. A second issue relates to the difference in coefficient of thermal expansion (CTE) between chip and substrate, where heating and cooling of the entire assembly results in important deformation and stresses. This can lead to assembly defects such as post-solidification delamination of the chip dielectric layers, commonly known as "white bumps" owing to their light coloration observed during post-assembly ultrasonic inspections [3], [4], [5]. These same stresses can also reduce long-term reliability of the assemblies [6].

To mitigate these issues, an alternative approach known as thermal compression bonding (TCB), uses pressure and heat that is primarily localized to the chip region [7], thereby minimizing substrate heating and thus reducing the stresses induced by CTE mismatch [8], [9], while additionally planarizing the chip-substrate interface. However, TCB suffers from its own set of concerns, such as reduced throughput and expensive bonding systems, despite efforts to improve its performance [8], [9]. In addition, solder extrusion during the application of pressure and heat in the TCB process can create bridges between chip terminations or reduced spacing, the latter leading to reliability issues.

A third approach, laser-assisted bonding (LAB), was therefore introduced [10]. Here, a homogenized rectangular laser beam provides a uniform radiation across the entire top surface of the silicon chip. This energy is mainly absorbed by the silicon chip then channeled to the solder termination interfaces, thereby melting the solder to form the interconnections. As the heat is locally applied to the chip region and only for a span of a few seconds, thermomechanical stress and deformation are minimized. In addition to reducing assembly warpage, LAB offers an extremely short assembly time compared with TCB [11], thereby approaching manufacturing throughputs comparable to MR [12].

Work to date on the LAB process has predominantly focussed on small and medium sized chips. This study therefore seeks to understand the effects of adapting the LAB approach to the very large chip sizes of interest to IBM. As such, we present the development approach, and particular issues encountered, for a large chip LAB set-up. In resolving these issues, a particular effort is made to understand, using both construction analysis and finite element modelling (FEM), the specific impact of chip size. Additionally, we seek to confirm whether the previously heralded advantages of LAB over MR remain evident for a very large chip.

II. Experimental Procedures

A. Test vehicle

The test vehicle, TVG, consists of a silicon (Si) chip comprising 32000 copper pillar type bumps and an organic substrate comprising a blanket thin Ni-Au surface finish. The latter was employed as the available laser set-up was not equipped with chip-substrate alignment capabilities at the time of this study. Additional details, including dimensions, are provided in table 1.

Table 1 Test vehicle details

Test vehicle information		
Chip	Chip size	25 x 26 mm^2
	Chip thickness	780 µm
	Bump pitch	130 µm
	Cu pillar height	44 µm
	Solder height	28 µm
	Bump composition	Sn1.8%Ag
Substrate	Total thickness	1,4 mm
	Substrate size	63 x 63 mm^2

B. LAB set-up and experimental approach

The LAB process was performed in an air atmosphere with a Laserline Inc. laser soldering system at various powers and timeframes. This laser system consists of a 980 nm continuous wave (CW) laser source with an 800 W maximum power and homogenizing optics capable of beam size adjustment between 8mm and 45 mm in the x and y directions. The reflow profile temperature is adjusted primarily by laser power and LAB duration and ideally includes a period of silicon surface temperature maintenance, also known as a "plateau" or "dwell", to ensure proper temperature distribution. This "dwell" determines the time spent above the SAC solder melting temperature of 217°C (TAL, "Time Above Liquidus"). The reflow temperature profile of the silicon chip surface was measured using the IR camera that is integrated in the laser system. To calibrate this surface temperature to actual solder joint temperature, a thermocouple kit is used, as shown in Figure 1. This device is equipped with probes placed at the interface between the chip and the substrate at both the center and corners of the chip.

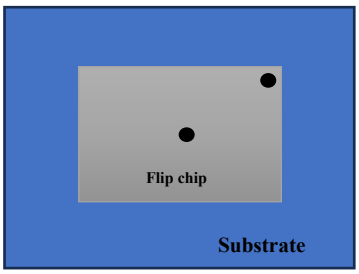


Figure 1 *Thermocoupled test vehicle*

In order to optimize the assembly process, different profiles were used during reflow tests, varying maximum temperature and TAL.

In that our current laser set-up was in an air rather than inert atmosphere, reflow tests were carried out using a Deltalux NRF-S14 water soluble flux. Two different means of flux deposition were employed: manual deposition of a thin layer of flux on the substrate surface and manual flux "dipping" of the chip solder bumps.

Assembly samples were first characterized by optical inspection of peripheral interconnections and x-ray imaging in order to assess both wettability and bridging. Select samples were cross-sectioned for scanning electron microscope (SEM) observation of intermetallic compound (IMC) and microstructural behavior. Chip warpage characterizations were carried out using a Nikon laser interferometry system.

C. Simulation

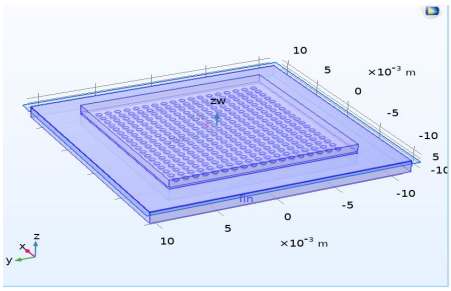


Figure 2 *Front view of a flip chip with solder bumps on a NiAu substrate*

Finite element analysis (FEM) using COMSOL software was employed to evaluate the impact of laser beam size on the temperature distribution of the solder joints, and thus analyze the influence of natural convection on the corners and ends of the assembly. Figure 2 illustrates the structure of the flip chip assembly developed in this simulation study. To maintain reasonable computational times, chip sizes of 12mm, 16mm and 20mm square were used then the results were extrapolated to 26mm square to emulate the experimental TVG chip conditions. Interconnection pitch was maintained at 130µm throughout. For each chip size, two beam sizes were simulated, the first being similar to the chip size (+ 1mm) and the second being much larger (+10mm). A simple temperature profile (no plateau) was applied, with a temperature rise phase of 1.7 seconds for each scenario, reaching 275°C at the center of the chip. Convection was applied to the first three rows on each side of the chip to represent the effect of convection on the peripheral solder interconnections. The physical parameters of the materials used in the model are defined in Table 2. Surface boundary conditions on the silicon chip are given by:

$$\vec{n}\left(k\frac{dT}{dt}\right) = h(T_{amb} - T) \quad (1)$$

With $\vec{n}$ as the normal vector, h as the convective heat transfer coefficient and T_{amb} as the ambient temperature.

Table 2 *Material properties*

	Si	FR4	Cu	SAC 305
Density (kg/m)	2329	1900	8960	7370
E (GPa)	170	26.9	117	38.7
ν (Poisson's ratio)	0.28	0.39	0.35	0.4
α (ppm/°C)	2.6	7	17	21
Thermal Conductivity (W/m*K)	16280[W/m]/T	0.3	385	62
Specific Heat (J/kg*K)	700	1369	385	232

III. Results and Discussion

A. LAB temperature profile development

Figure 3 shows the temperature difference between the chip surface and the solder

interconnections at the center and at one of the corners. A difference of 72°C is observed.

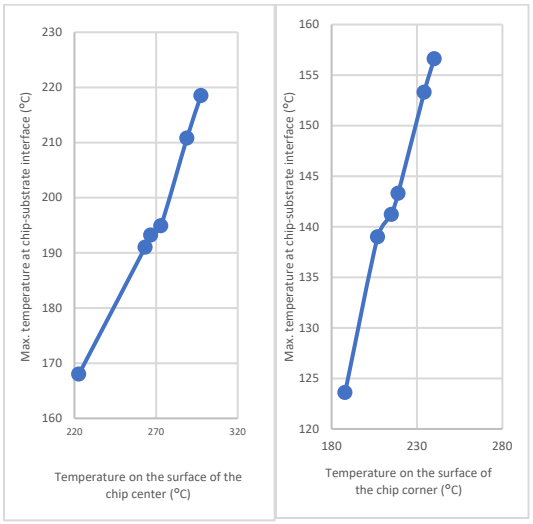


Figure 3 *Variation in temperature between chip surface and chip/substrate interface at (a) chip center and (b) one chip corner*

at the center of the chip (figure 3a). This can be explained by the short LAB heating period used in this test combined with the fact that the TVG chip is 780µm thick. To compensate, the profile was adjusted to ensure a sufficient dwell time to allow heat transfer through the chip. It was also noted that the temperature difference at the chip corners were even greater, reaching about 80°C (figure 3b). This suggests a convective impact from the surrounding ambient air on the peripheral solder joints despite using a laser beam size 1mm larger than the chip. While such a beam size to chip size ratio may be appropriate for smaller chips, it appears that a larger chip may require a higher ratio to ensure a homogeneous thermal distribution. Such beam size adjustment is consistent with the work of Braganca and Kim [13]. Given these results, a nominal profile was proposed as shown in Figure 4, and the laser beam size was adjusted to 36mmx35mm, thus extending beyond each chip edge by 5mm. IR temperature measurements determined that this beam size extension increase results in a 10-15°C increase in substrate temperature, which was not considered significant.

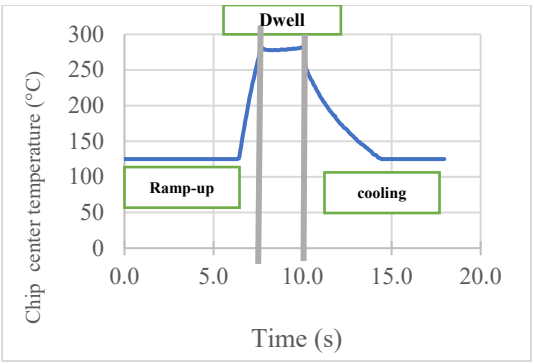


Figure 4 *Temperature profile for LAB reflow.*

B. Optimization of LAB assembly process parameters

Table 3 summarizes the conditions and results of an assembly design of experiments where surface temperature and TAL were varied. Beam size was kept constant at 36mm x 35mm and a substrate fluxing approach was used.

Table 3 *Results of assembly design of experiments*

TAL/Temp	270	275	280
3,5s		Good Wetting Some Bridging	Good Wetting Some Bridging
4,5s		Good Wetting Center Bridging	Good Wetting Significant bridging
5,5s	Partial Wetting No Bridging		

The results suggest that a 270°C chip surface temperature did not permit sufficient solder melting at the periphery of the large chip, even with a TAL of 5.5 seconds. On the other hand, at 275°C and 280°C, with TAL's of 3.5 and 4.5 seconds, full wettability was achieved, as illustrated in figure 5a, so a TAL of 5.5s was deemed unnecessary at these temperatures. However, all conditions showing good wettability exhibited various degrees of solder bridging (figure 5b). A repeatability experiment using a 275°C surface temperature and a 3.5s TAL on 4 consecutive assemblies validated the DOE results, exhibiting perfect wetting but some solder

bridging. A representative cross-section is shown in Figure 6.

Despite attempts to minimize flux volume by applying as thin a layer as possible to the substrate, this method was not sufficiently uniform to prevent the formation of flux-induced solder bridges between the interconnections on a blanket Ni/Au substrate.

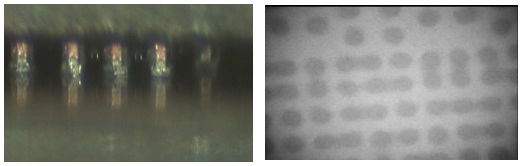


Figure 2 *a) optical inspection of LAB assembly on Ni-Au substrate, b) X-ray inspection of solder bridges.*

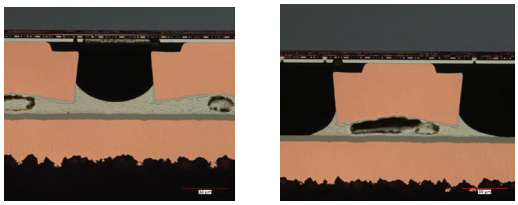


Figure 3 *SEM cross-sectional images of solder joints for TVG assembled by LAB at 275°C peak and 4s TAL using substrate fluxing showing a) solder bridging and b) solder voiding.*

Some solder voiding is also observed in the cross-section, which is an additional indication of uneven flux distribution. To this end, additional tests were carried out using a manual "dipping" method which results in flux deposition only on the chip solder bumps. The dipping flux method enabled successful reflow on the corners and ends of the chip, even when a lower TAL of 2s was employed (figure 7).

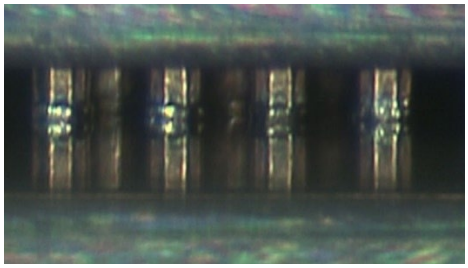


Figure 7 *Optical inspection of solder joints obtained after a LAB test on a Ni-Au substrate using flux dipping, 275 °C peak temperature and 2s TAL.*

More importantly, X-ray images (figure 8) confirmed a complete absence of bridging across the entire large chip surface.

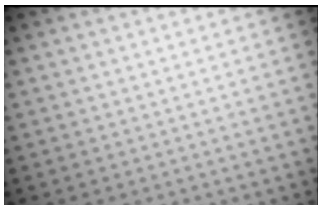


Figure 4 *X-ray inspection of TVG assembled by LAB at 275°C peak and 2s TAL using flux dipping.*

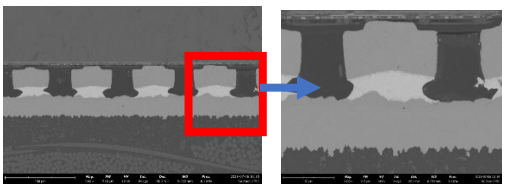


Figure 5 *Cross-sectional SEM images of TVG assembled by LAB at 275°C peak and 2s TAL using flux dipping.*

Cross-sectional SEM images (figure 9) confirmed the optical and X-ray observations. In addition, the flux dip method appears to have eliminated the solder voiding phenomenon. Noteworthy as well is the shape of the joints, which show a narrowed diameter in the middle of the solder joint, which can be attributed to the use of a blanket Ni/Au surface, that enabled solder spreading, albeit less so than with substrate fluxing.

Given this series of experiments, recommended conditions for achieving satisfactory assembly are summarized in table 4.

Table 4 *Recommended LAB conditions for TVG chip assembly.*

Flow deposit method	T°C peak at the center of the chip	TAL (s)	Beam size (mm x mm)
Dipping	275°C	2s	36mm x 35mm

C. Comparison between Mass Reflow and Laser Assisted Bonding

To compare warpage effects between the MR and LAB processes, 4 parts were assembled using the LAB process and 6 parts using the MR process. The reflow parameters used by the LAB process were 275°C peak, 4s TAL 4s and 35mm x 36mm beam size. The MR parts were assembled per known MR process parameters for this TVG chip,

using the same Ni/Au 'blanket' substrates as used for the LAB assemblies.

Table 5 *Warpage comparison of the MR and LAB processes on TVG flip chip assemblies.*

	MR	LAB
Number of chips	6	4
Average (µm)	134,6	64,5
Standard deviation	1,2	4,9

As seen in Table 5, the average warpage with the LAB process was 64.5µm, while those with MR showed an average of 134.6 µm. Despite the higher standard deviation for the LAB process, the difference is significant and can be explained by the fact that LAB heating is essentially localized to the chip rather than the substrate, even with a beam size that is 10mm larger than the TVG chip. This reduces thermomechanical stress and warpage, in line with the work of Jang et al [15] on the effects of differences in CTE between chip and the substrate. The latter demonstrated a reduction in warpage from 40µm after MR to 17µm after LAB for a 6 x 6 mm^2. Unlike LAB, MR reflow heats the entire assembly to reflow temperature, generating greater CTE mismatch induced stresses. It's worth noting that studies on warpage of such large chips are uncommon in the literature.

In order to compare the impact of each process on microstructure, we first established the baseline state of the chip solder bumps before assembly. Figure 9 shows images obtained after cross-sectioning a TVG chip, highlighting a Cu_6Sn_5 IMC layer thickness of around 2.4 µm at the solder-Cu pillar interface which is generated during reflow of the electroplated bump.

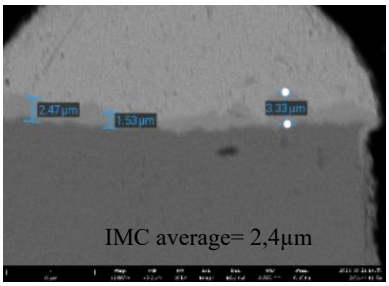
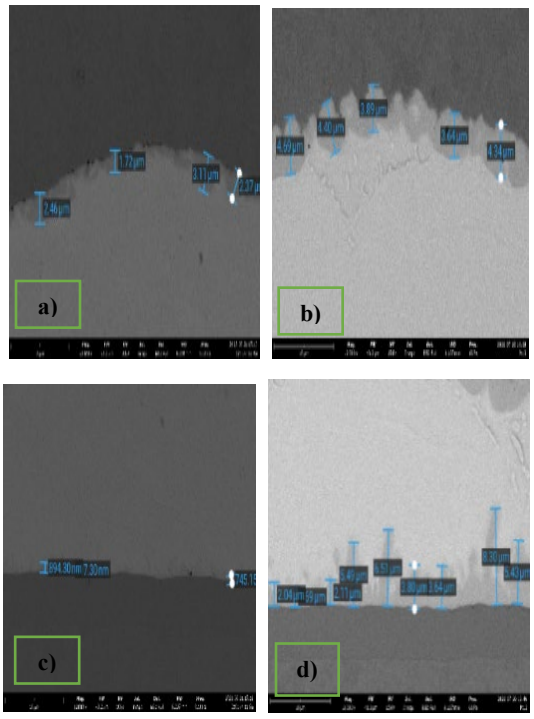


Figure 9 *Cross-sectional image of TVG chip showing Cu_6Sn_5 IMC thickness.*

Figures 10a and 10b show images of these same interfaces after LAB and MR assembly. The morphology of the IMC layer at the interface of samples are notably different. In the case of MR reflow, the Cu_6Sn_5 layer has a uniform, extended morphology along the entire length with an



c) d)

Figure 6 *SEM image of IMC layers at copper pillar interface using a) LAB and b) MR and at Ni-Au substrate interface using c) LAB and d) MR*

average thickness of about 4.2 µm, representing an increase of 1.75 µm over that observed on a pristine chip. On the other hand, after LAB reflow, the IMC thickness did not noticeably change, remaining at about 2.4µm.

On the Ni-Au substrate side (Figures 10c and 10d), an IMC layer of around 4.6 µm has developed in the case of MR, the composition of which is identified as $(Cu,Ni)_6Sn_5$. For LAB, average IMC thickness is around 1µm, which is similar to that observed by MinHo et al. [16]. These significant differences in IMC between LAB and MR are consistent with the fact that the LAB reflow time is very short compared to MR.

Microstructural observations of the solder matrix showed no notable difference in Sn grain sizes between the LAB and MR assemblies which is in contrast to the study by Hiroshi Nishikawa et al [17] that showed that the size of the primary β-Sn phase was smaller for the LAB process than for MR.

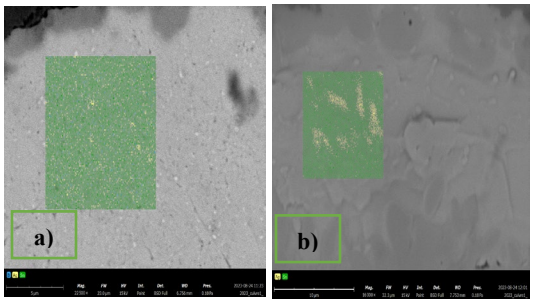


Figure 7 *SEM image of Ag3Sn grain morphology and size in bulk solder after a) LAB and b) MR*

On the other hand, as seen in figure 11, the Ag_3Sn formations in the bulk solder are considerably larger after the MR process than those obtained after LAB. This could be an indication of agglomeration in the case of MR. which could be explained by the longer TAL and slower cooling rate inherent to MR. These results are in line with the literature, where Dutta et al [18] reported that for SAC solder, Ag_3Sn particles in the solder matrix undergo Ostwald ripening, particularly at temperatures above 125°C. In that such ripening was found to degrade solder joint mechanical properties, it can be induced that the solder joint matrix formed by the laser process would be stronger than that formed by MR. However, this would need to be validated by mechanical testing such as chip shear or nano-indentation.

D. IMC thickness across the large chip

Using the same cross-sectional samples of figure 10, IMC thickness measurements at the Ni/Au interface were taken at various locations across the TVG chip. It was found that said thickness at the center of the chip was around 1.9 µm, while at mid-chip and at chip edge, thickness was only around 0.9 µm. The higher IMC formation at the center of the chip is in line with our observations in section IIIA that temperature differences between surface and solder joint are lower at the center of the chip than at the periphery, despite the enlarged beam used to ensure good wettability at the periphery. It is proposed that a convection effect affects the chip ends originating from the ambient air surrounding the assembly in our installation. This notion is discussed in more detail in the simulation section.

E. Numerical simulations

As a baseline for validating our FEM simulation of LAB reflow, we determined the temperature variation (ΔT) at the chip surface (Figure 13). The result of 4°C corresponds well with the temperature variation obtained experimentally.

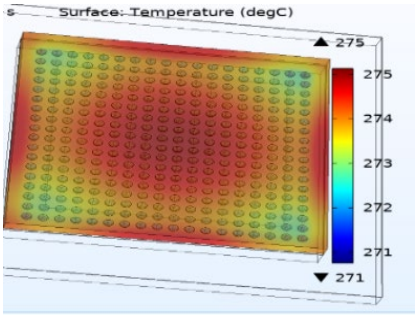


Figure 8 *FEM simulation of temperature distribution on the flip chip surface.*

We then determined the influence of air convection as a function chip size (figure 14). Here, the laser beam size was similar to the chip size. While the observation that temperature variation between center and corner solder joints increases with the contribution of convection is an expected result, a more interesting finding was that this temperature variation is much greater as the chip size increases. This supports the challenges encountered of balancing bridging and wetting defects when assembling the large TVG chip without enlarging the laser beam size.

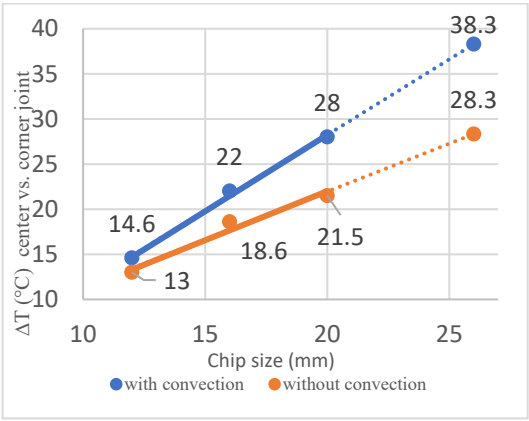


Figure 9 *FEM determined variations in the temperature between center and corner joints as a function of chip size and presence of convection.*

Such results are also in line with the study by Bracanga et al [13], who demonstrated that during reflow, the solder bumps at the beam extremities do not receive the same amount of energy as those further away from the extremities.

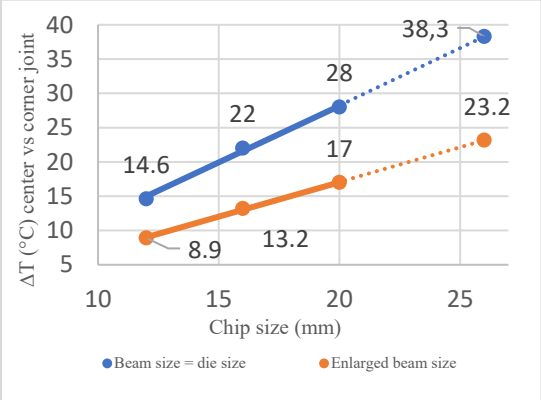


Figure 10 *FEM determined variations in the temperature between center and corner joints as a function of chip size and laser beam size.*

We next used the simulation, including the previously described convection effect, to determine the impact of beam size. Figure 15 shows that enlarging the laser beam size to 10mm larger than the chip size reduces the temperature variation between the center and corner solder joints. Further, this reduction is more significant as the chip size increases. In the case of extrapolation to the 26mm size of the TVG chip, it is interesting to note that, without an enlarged beam, the 38.3°C variation represents a maximum temperature of 269.1°C for the joints in the center of the chip and a minimum temperature of 230.8°C at the peripheral joints. This minimum temperature, which is close to the SAC reflow temperature, could lead to wetting problems at the periphery. On the other hand, any attempt to raise peripheral temperatures by increasing surface temperature would have the effect of raising the temperature of the center joints, which could induce solder bridging. By instead sufficiently enlargening the beam, the temperature gap is reduced to only 23.2°C, representing a minimum temperature of 245°C, well above the SAC melting point and hence validating the results observed in our DOE using the 36mm by 35m beam size.

IV. Conclusion

This study demonstrated the effectiveness of the LAB process for large flip chips, identifying critical factors that could affect the quality of flip-chip interconnects. In particular, it was discovered that a sufficiently large beam size is essential for successful assembly of the large (26mm x25mm) TVG chip. This requirement was validated by FEM analysis which showed that larger chips suffer from larger temperature variations between their center and peripheral solder joints, at least with thick (780µ) chips.

Comparisons of a thus optimized LAB process to a standard MR process, both on the large TVG chip assembly, demonstrated that the advantages of the LAB process observed in the literature are indeed extended to such large chip sizes, specifically a 50% lower chip warpage and a 5X reduction in initial interfacial IMC formation.

It is recommended to validate whether the developed LAB process for a large chip, and its observed advantages, translate to improved reliability. As such, future work will focus on a more suitable LAB prototyping set-up with large chip alignment capabilities and an inert atmosphere, followed by appropriate stress testing, in particular high temperature storage and thermal cycling.

V. Acknowledgment

The authors gratefully acknowledge the facility support provided by the Institut Interdisciplinaire d'Innovation Technologique (3IT) and the Centre de Collaboration MiQro Innovation (C2MI). The university authors are part of LN2. a joint international Research Laboratory (IRL 3463) funded and co-operated in Canada by Université de Sherbrooke (UDS) and in France by CNRS as well as ECL, INSA Lyon, and Université Grenoble Alpes (UGA). It is also supported by the Fonds de Recherche du Québec en Nature et Technologie (FRQNT). The authors also acknowledge funding provided by the Natural Sciences and Engineering Research Council (NSERC) of Canada and Prompt Quebec. Finally, we would like to thank Geneviève Beaulieu for her cross-sectional analysis expertise and Laserline Inc. for their technical and equipment support.

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