An Open Chiplet Ecosystem for Constructing System-in-Package with Universal Chiplet Interconnect Express™ (UCIe™)

Debendra Das Sharma
Intel Senior Fellow, Intel Corporation, 2200 Mission College Blvd.,
Santa Clara, CA 95052, USA
Email: Debendra.das.sharma@intel.com

Michael Mingliang Liu
Intel Foundry, Intel Corporation, 2200 Mission College Blvd.,
Santa Clara, CA 95052, USA
Email: Michael1.liu@intel.com

Abstract

Chiplets connected on package, referred to as system-in-package (SiP), has become mainstream across the compute continuum. Universal Chiplet Interconnect express™ (UCIe™) is an open industry standard offering significant bandwidth, power-efficiency, and latency improvements over other interconnects. The entire industry has rallied behind UCIe and driving it forward to solve the challenges in computing while deploying UCIe for a wide range of usage models. UCIe is poised to enable innovations at the package level the way PCIe and CXL has driven innovation at the platform level.

Keywords

Chiplet, Packaging, Interconnect, UCIe, PCIe, CXL, System-in-Package (Sip), System-on-Chip (SoC)

I. Introduction

Gordon Moore posited that the number of transistors in an integrated circuit will double every two years [1] that became popularly known as "Moore's law". In the same paper, he also predicted the "Day of Reckoning": *"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."* That day is already here! Today, we see on-package integration of multiple dies in mainstream commercial offerings such as client CPUs, server CPUs, GP-GPUs, etc.

There are many drivers for on-package chiplets. With the recent slow-down of Moore's law and growing compute demand, we have seen advanced packaging technology deployment in volume commercial products (e.g., client CPU, Xeon, GP-GPUs) to meet the insatiable computing demand. This has resulted in the deployment of multiple chiplets packaged together instead of large monolithic dies. In addition to overcoming the reticle limits, delivering the required memory bandwidth, and addressing yield / cost challenges of large dies with advanced processing nodes are the other motivators for chiplets. Chiplets also enable bespoke solutions with time-to-market advantages due to reuse of existing chiplets and only designing new chiplets with new or improved functionality.

Computing demand continues to grow. There are evolutionary applications such as data analytics, infrastructure as a service where a doubling of performance every 2 years meets the need. Revolutionary applications such as supercomputing and AI demand a 10x growth every year. We will continue to see imbalances in computing infrastructure between heterogeneous computing, memory bandwidth, memory capacity, interconnect bandwidth, and interconnect latency in a power-constrained environment. Advanced packaging technology [6,7] holds the key to delivering the increasing computing demand through mix and match components for the next few decades in the most power-efficient manner.

Universal Chiplet Interconnect Express™ (UCIe™) [2,3] is an open industry standard interconnect, offering high-bandwidth, low-latency, power-efficient, and cost-effective on-package connectivity between heterogeneous chiplets,

spanning cloud, edge, enterprise, 5G, automotive, high-performance computing, and hand-held solutions. UCIe offers PCI-Express® (PCIe®) and Compute Express Link™ (CXL™) protocol support natively to take advantage of the existing hardware and software infrastructure for making the open chiplet based SiP a reality [2, 3, 4, 5, 8, 9, 10, 13, 14].

Figure 1 shows a SiP using chiplets connected with the UCIe interconnect. The UCIe vision enables a SiP designer to pick chiplets from an open ecosystem, manufactured in any foundry, and assembled by any OSAT (outsourced semiconductor assembly and test) to deliver the desired performance. This is similar to how systems are assembled in an open and composable platform today from various components using PCIe and CXL [4, 5, 10, 14]. Effectively, with UCIe, the SiP is the new SoC and the package is the platform of innovations, where composable systems can be constructed bringing in the platform level innovations of the past few decades to the package level.

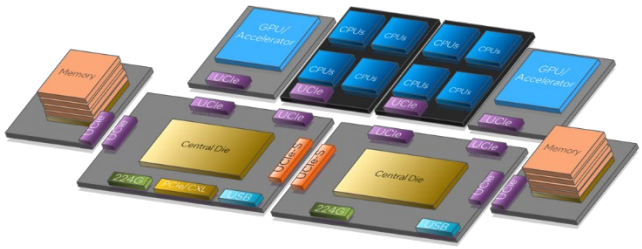


Figure 1: SiP construction using UCIe Chiplets

II. Ingredients of a Successful Standard

Figure 2 demonstrates the necessary conditions for a standard to be widely deployed. This is based on our experience in driving successful industry standards such as Peripheral Component Interconnect Express (PCIe) and Computer Express Link (CXL).

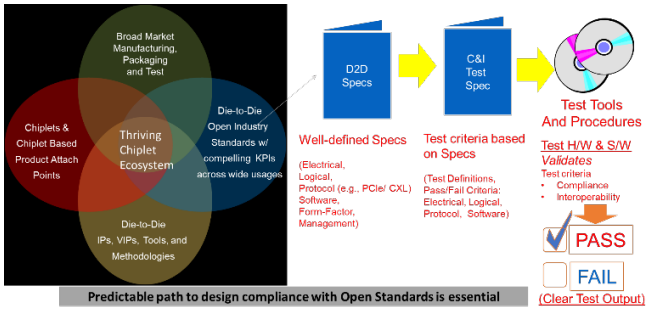


Figure 2: Ingredients of a successful and broad interoperable chiplet ecosystem

An open industry standards body defining a specification is a critical component for wider deployment as companies invest in technologies where they can openly participate. Any company can join UCIe and member companies drive its evolution. Thus, like PCIe and CXL, companies can invest in the technology without worrying about the viability of the technology, since it is backed by a broad ecosystem. Compelling key performance indicators (KPIs) catering to a wide range of usages is essential. It is also important to have a complete specification that comprehends all the layers of the stack for ensuring interoperability. As we will see later, UCIe meets these requirements. On-package integration of chiplets has matured commercially across different manufacturing, assembly, and test companies. This maturity removes another obstacle for adoption.

UCIe is the result of industry leaders with expertise in chiplet integration working together to develop a common standard so that multiple chiplets from different sources can interoperate seamlessly. This will drive a thriving open chiplet ecosystem.

III. UCIe 1.0 and UCIe 2.0 Overview

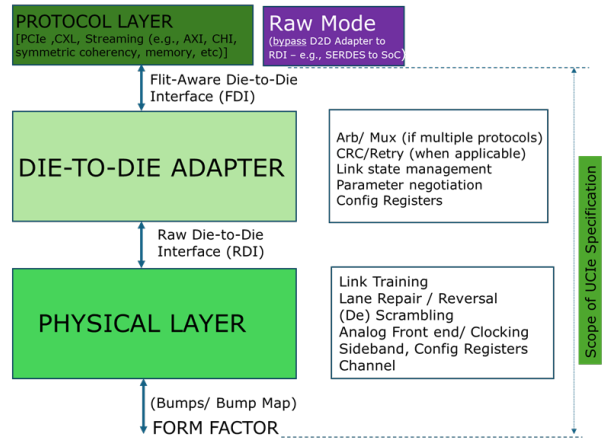
UCIe 1.0/1.1 is a layered protocol (Figure 3a) [2, 3, 6, 8, 9, 11, 12, 13]. The physical layer (PHY) defines electrical signaling, clocking, link training, sideband handshake, circuit architecture, etc., UCIe supports different data rates, widths, bump-pitches, and channel reach to ensure the widest interoperability feasible (Table 1). The basic unit is a module which comprises of 16 or 64 single-ended, unidirectional, full-duplex data lanes, one single-ended lane for '*valid*', one single-ended lane for tracking, and a differential forwarded clock; in each direction for the main-band (Figure 3b). The sideband in each module consists of 2 single-ended lanes (one data and one 800 MHz forwarded-clock) per direction. The sideband interface is used for status exchange to facilitate link training, link management, test, register access, and diagnostics. Multiple modules (1, 2, or 4) can be aggregated to deliver more performance per link.

The die-to-die (D2D) adapter is responsible for reliable delivery of data through its cyclic redundancy check (CRC) and link level retry mechanism [2, 3, 8, 9, 11, 13], when needed. It defines the arbitration across multiple protocol stacks if present. A 256-byte flow control unit (FLIT) defines the underlying transfer mechanism when the adapter is responsible for reliable transfer.

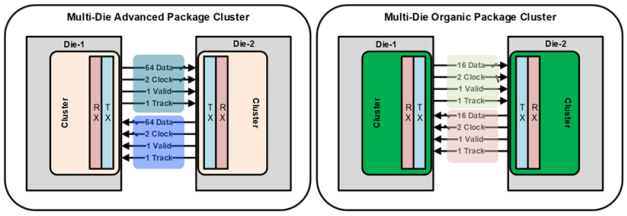
UCIe maps PCIe and CXL protocols natively as those are widely deployed at the board/ rack level across all segments of compute. This is done to ensure seamless interoperability by leveraging the existing ecosystem. With PCIe and CXL, SoC construction, link management, and security solutions that are already deployed can be leveraged for UCIe connections.

The usage models addressed are also comprehensive: data transfer using direct memory access, software discovery,

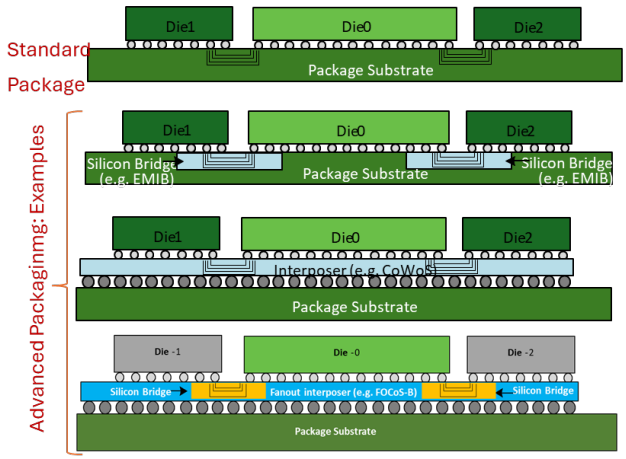
error handling, etc., are addressed with PCIe/ CXL.io; the memory use cases are handled through CXL.Mem; and caching requirements for applications such as accelerators are addressed with CXL.cache. UCIe also defines a "streaming protocol" which can be used to map any other protocol [2,13] for scale-up applications.



(a. Layering Approach of UCIe 1.0/1.1 Specification)



(b. UCIe Module showing main data path)



(c. 2D and 2.5D Packaging Options with UCIe 1.0/1.1)

Figure 3: UCIe 1.0/1.1 Approach to Layering and Packaging

UCIe defines two types of packaging, standard and advanced, as shown in Figure 3c and the bump-pitch, channel reach, and performance metrics described in Table 1. The standard packaging is for cost-effective and flexible packaging whereas the advanced packaging offers high bandwidth density with low power.

UCIe 1.1 is built on top of UCIe 1.0 with enhancements for the automotive usages (preventive monitoring of link health), enabling streaming protocol to use the full stack, area optimization for advanced package for lower bump pitches, and enhancements for compliance testing [13].

Table 1:Key Metrics of UCIe 1.0/1.1

Characteristics / KPIs	Standard Package	Advanced Package	Comments
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	
Target for Key Metrics			
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u for AP; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Bit Error Rate (BER)	< 10^{-27} below 16G for UCIe-a; 12G for UCIe-S; else < 10^{-15}		Probability of a bit error
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

Table 1 provides the target performance metrics of UCIe 1.0/1.1. The bandwidth density is 2 to 3 orders of magnitude higher whereas the power efficiency and latency is an order of magnitude lower than external SERDES based links such as PCIe/CXL. The low-power state transition with UCIe is sub-ns whereas external SERDES is several micro-seconds, resulting in better dynamic power management.

The UCIe 2.0 Specification addresses two broad areas to drive a thriving open chiplet ecosystem. The first addresses manageability, debug, and testing challenges arising in any System-in-Package (SiP) construction with multiple chiplets in a holistic manner. This solution extends beyond the UCIe 1.0 interface, using UCIe 1.1 enhancements, in a fully-backwards compatible manner. The second area deals with vertically integrated chiplets with exceptionally fine pitches (9µm down to approximately 1µm, and potentially lower) using technologies such as hybrid bonding interconnects, which we will refer to as "UCIe-3D".

IV. Usage Models Supported by UCIe

UCIe supports two broad usage models [2, 3, 5, 8, 9, 11, 12, 13]. The first is SiP construction to deliver power-efficient and cost-effective performance, as shown in Figure 1. Components attached at the board level such as memory, accelerators, networking devices, modem, etc. can be integrated at the package level with applicability from hand-held to high-end servers with dies from multiple sources connected through different packaging options even on the same package.

The second usage (Figure 4) is to provide off-package connecvity using different type of media (e.g., co-packaged optics, electrical cable, mmWave) using UCIe Retimers to

transport the underlying protocols (e.g., PCIe, CXL) at the rack or even the pod level for enabling resource pooling, resource sharing, and even message passing using load-store semantics beyond the node level to the rack/ pod level to derive better power-efficient and cost-effective performance at the edge and data centers.

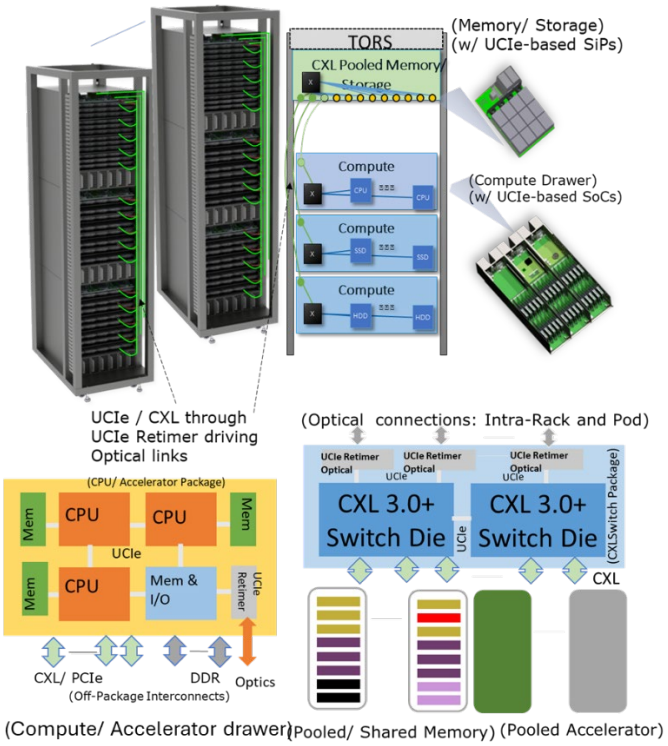


Figure 4: UCIe-Retimer based co-packaged optics delivering pooling, sharing, and fabric level connectivity at Rack/Pod level

V. Conclusion

There are many challenging problems that the industry needs to solve to realize the vision of an open plug-and-play chiplet based ecosystem with UCIe [12]. Testability, manageability, compliance, security, form-factor, and debug are the areas that will need more innovation as learnings from the first set of UCIe implementations come through. We already have several hooks in the specification to address these aspects at the interconnect level (e.g., loopback, margin, fault reporting, sideband, etc.), but several other challenges exist especially at the package level. Some chiplets may not have external package pin connectivity in a SiP, posing significant controllability and observability challenges. For die testing, while we can probe bumps, we cannot do the same for micro-bumps especially as we move towards 25u bump pitches. Debugging will pose a challenge when we cannot put a logic analyzer or scope inside the package. Upgrading firmware for chiplets needs to be done in the field securely without impacting operations. We need to develop a common standardized solution for all these challenges using a combination of external package pins (e.g., JTAG, SMBus, PCI-Express, DDR, USB, etc.) working in conjunction with the main UCIe data path or dedicated UCIe-standard (including sideband only) links connecting all the chiplets in a SiP [12]. The other area where UCIe needs to deliver is vertical chiplets [12], delivering another 2-3 orders of magnitude improvement in bandwidth density and power improvements to address the insatiable demand for power-efficient performance in this AI-era.

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