Substrate Warpage Study for Heterogeneous Packages

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Abstract

Warpage formation in semiconductor packages is generally known to occur from coefficient of thermal expansion (CTE) mismatches between multilayered materials with different properties. The different properties of each printed circuit board (PCB) layer will yield different expansion rates, which will lead to significant high warpage formation under the reflow temperature. The presence of significant warpage will further induce opened solder joint risks, solder joint collapse for flip chip ball grid arrays (FCBGAs) and so on. Package warpage is an important factor that impacts board assembly yield, delamination, solder joint fatigue reliability, and other thermal stress issues. Reducing warpage is a primary concern when trying to enhance the service life of a package.

For years the IC industry has been driven by Moore's Law assumption that the functionality that fits on a single die will double every 18 to 24 months. As minimum dimensions have shrunk from 14 to 10nm and now toward ~3nm, it could be assumed that die size should shrink accordingly. However, with network applications, this assumption has been disproven. For modern FCBGAs, the scale of die and package for networking applications are increasing dramatically. The metal heatsink not only provides thermal emission out of the package but also manages the warpage of a large FCBGA. A large (72 x 72 mm test vehicle) FCBGA is package level reliability (PLR) qualified with a rigid and heavier heat sink. However, when the package is mounted to a PCB, the BGA solder balls melt during reflow since they are not able to uphold the heavier package. This results in low standoff height and solder bridging because the balls flow and connect to adjacent ones. The deviation from Moore's law and the addition of heatsinks to networking packages, along with other heterogeneously integrated technologies, have a significant impact on system-level warpage. Various package design strategies are discussed in this paper that can be included to control these new sources of warpage.

Introduction

With the network application for built-in artificial intelligence (AI) increasing, heterogeneous integration is necessary to put many different technology pieces into a single, advanced package. This tendency is no longer optional as high-performance computing in networking is getting faster and faster from 100/200G to 400G and beyond. Those pieces could vary significantly and not just consist of silicon dies. In the past, with 2.5D, when the combination of different die and high-bandwidth memory (HBM) were discussed, it was not called heterogeneous integration (HI). It was just called a silicon interposer design. Today, the umbrella of advanced packaging includes 2.5D, fan-out, or even 3D-IC packaging, and integrating any of the pieces together is heterogeneous integration. Bus criteria become complex and sophisticated so that requirements for these data paths are featured in following ways.

- I/O count➔Trace line/space (L/S) and layer count
- Signal speeds➔ Dielectrics.
- Terminations➔ Construction approaches
- Die-die spacing➔Power Delivery or Distribution Network (PDN)

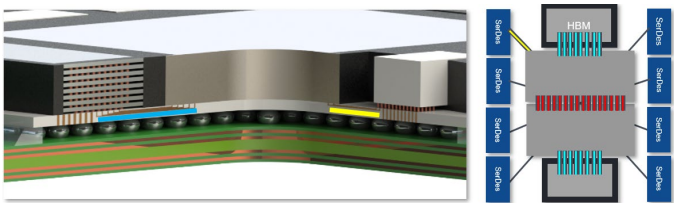


Figure 1. I/O distribution of heterogenous integration package.

Many high-performance computing (HPC) companies are addressing these changes.

The typical structure of 2.5D with one application-specific integrated circuit (ASIC) die + several HBMs, is inevitable getting a larger package size.

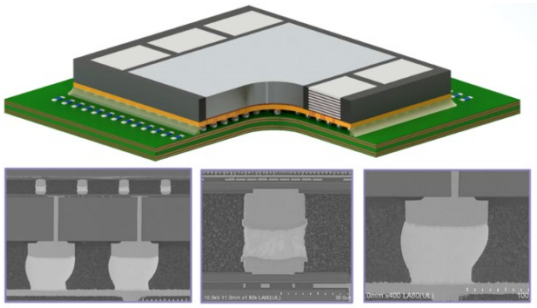


Figure 2. Amkor 2.5D Through Silicon Via (TSV) Chip on Wafer (CoW) FCBGA.

In addition, the substrate layer count is increased and the core thickness as well to address warpage concerns. Meanwhile, chiplets packaging cobbles up the substrate's built in Ajinomoto build-up film (ABF)-based dielectric constant (Dk)/dissipation factor (Df). Dielectric loss depends on current frequency and the Dk and Df of dielectric materials insulating the conductive materials. As the frequency increases, dielectric losses tend to increase, and the general approach to reduce these losses is using low Dk and low Df materials. Hence, low Dk and Df materials with good adhesion to the smooth surface of copper are required for high frequency PCBs.

Test Vehicle and Experience for SMT

A test vehicle consisting of a 72-mm x 72-mm package has been evaluated to understand the correlation between warpage behavior/magnitude and surface mount technology (SMT) defects. Although package warpage meets a JEDEC spec range (+230~-140 µm) with the recommended reflow profile for large body size, the SMT house struggles in mitigating SMT defects. See Table 1. Most of defects revealed ball grid array (BGA) shorts at the package corners. The improvement contains not only a revised SMT reflow profile (Figure 3) but also package warpage mitigation. In contrast to conventional large flip chip BGAs (FCBGAs), the large scale of heterogenous packaging is useful to combine substrate knowledge with multiple factors.

Table 1. Board Mounting Result

Phase	Total Qty	Reject Qty	Reject %
Trial A	800 ea	24 ea	3%
Trial B	855 ea	14 ea	1.6%

* Note: 30-days term between trial A and B.

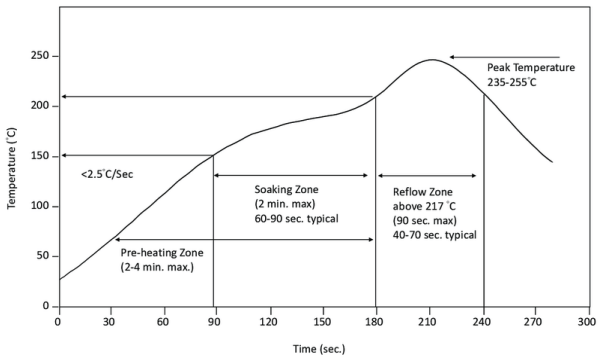


Figure 3. SMT reflow profile.

SMT board conditions in Figure 3 include:

- Outer dimension: 700 x 220 mm²
- PCB thickness/layer count: 5.2 mm/36 layers
- PCB pad finished: ENIG (ElectrolessNickel Immersion Gold)

In 2.5D chiplets structure with a Through Silicon Via (TSV) interposer, warpage behavior using shadow Moiré measured how module and bare substrate influence the warpage of the finished package (see Figure 4).

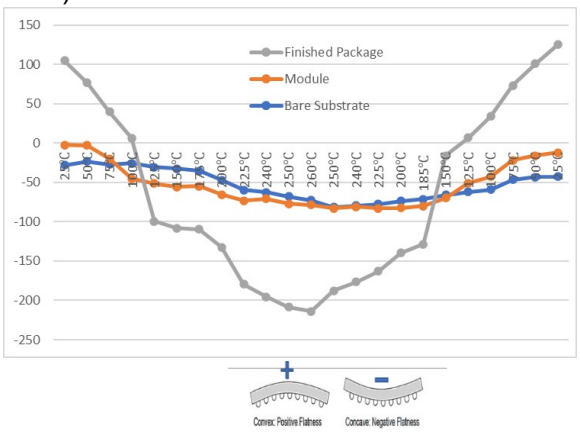


Figure 4. Shadow Moiré warpage. [µm]

In the transition from room to reflow and back to room temperatures, the warpage is shaped crying to smiling then back to crying on the condition of both module and bare substrate maintains smile warpage. Figure 4 shows the test setup. The **Shadow** Moiré process is:

1. Load the sample to the sample loader located in heating chamber.
2. Heat a sample with a programmed temperature profile and measure the warpage at specified temperatures.
3. Calculate the warpage value.

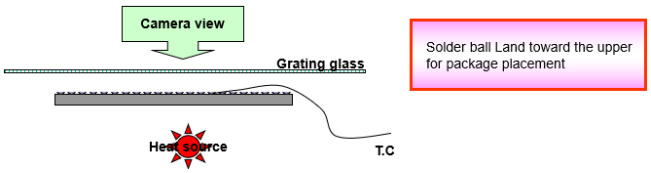


Figure 5. Test setup for temperature profile test.

The measurement points (in °C) are:

25 – 50 – 75 – 100 – 125 – 150 – 175 – 200 – 225 – 240 – 250 – 260 – 250 – 240 – 225 – 200 – 185 – 150 – 125 – 100 – 75 – 50 – 25

Figure 4 shows the package attributes. Where:

- Package size: 72 x 72 mm
- Logic size: 26 x 31 mm (full die thikcness)
- HBM size: 10 x 11 mm
- Substrate thickness/layer/build-up/core: 2.0 mm/16 layers/ABF GZ-41/E705GLH 1.2-mm thickness.
- Total package height: 5.65 mm
- Bottom BGA pitch/raw ball size: 1.1/0.6 mm (full grid array)

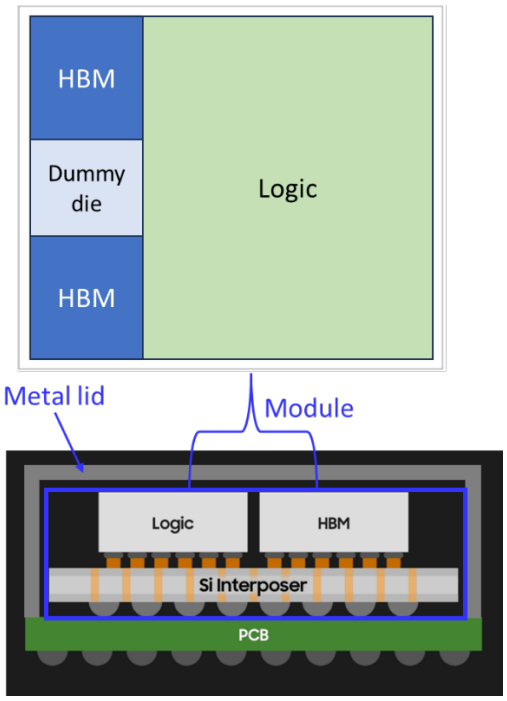


Figure 6. Top/side view of package.

Warpage Prediction by Substrate Analysis

Learning the warpage production of molded flip chips is informative (see Figure 5). This knowledge helps determine which direction/mechanisms can help mitigate warpage, including:

1. Need to consider influence factors like the package type, material properties, stack-up design and process conditions,
2. Total solution should concentrate on the initial stage of package/substrate design,
3. Need for standard guidelines to optimize design work and provide high warpage quality.

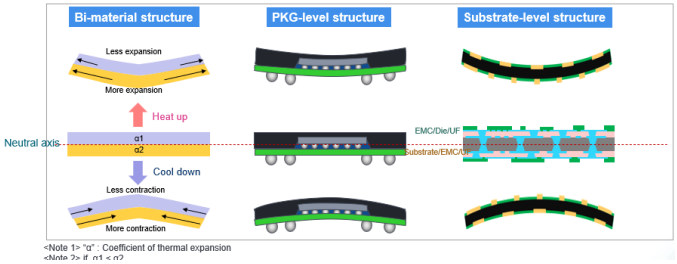


Figure 7. Warpage mechanism.

Assumption of CTE magnitude in order: die CTE < Core CTE < ppg CTE < EMC/UF CTE <PCB CTE<Cu CTE< SR CTE

How to control CTE?

Various factors to consider for improved CTE control are shown in Figure 6.

Structure	Element	To make higher CTE	To make lower CTE
Substrate	Cu	Thicker CuT	Thinner CuT
	Core	Thinner Core T Higher CTE core	Thicker Core T Lower CTE core
	PPG	Thinner PPG T Higher CTE PPG	Thicker PPG T Lower CTE PPG
	SR	Thicker SRT Higher CTE SR	Thinner SRT Lower CTE SR
EMC/UF		Thicker mold cap Higher CTE EMC	Thinner mold cap Lower CTE EMC
Die		Thinner Die T(=EMC vol. up)	Thicker Die T(=EMC vol. up)

Figure 8. CTE management.

Design Concept

Considering the factors in Figure 6, a design concept was proposed that is a hybrid build-up of a multi-layer core (MLC) + ABF as shown in Figure 7. This approach has several advantages aimed at large board computing/HPCs, high-end smartphones, and wearable devices. These include:

1. Better mechanical stiffness and warpage performance due to a pre-impregnated (PPG) material with glass fabric.
    a. Uses thin core to make shorter interconnections among the multi-chip module (MCM) larger body.

2. Improved power delivery (power integrity) performance to numerous transistors due to thicker copper (Cu) on core.
    a. Increases the size of server CPU and GPU. Increases the number of transistors.
3. Improves capacity (thermal and impedance) characteristics due to thicker Cu and PPG.
    a. Makes the distance from ground (GND)
    b. closer for GND efficiency.
4. Increases the functionality of the core due to thin core and PPG's stiffness.
    a. Utilizes the core effectively with embedded components.

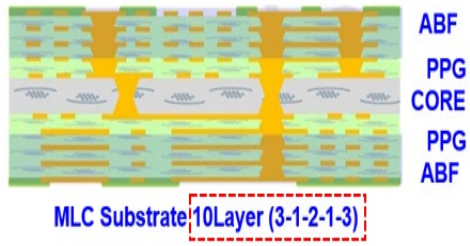


Figure 9. MLC structure.

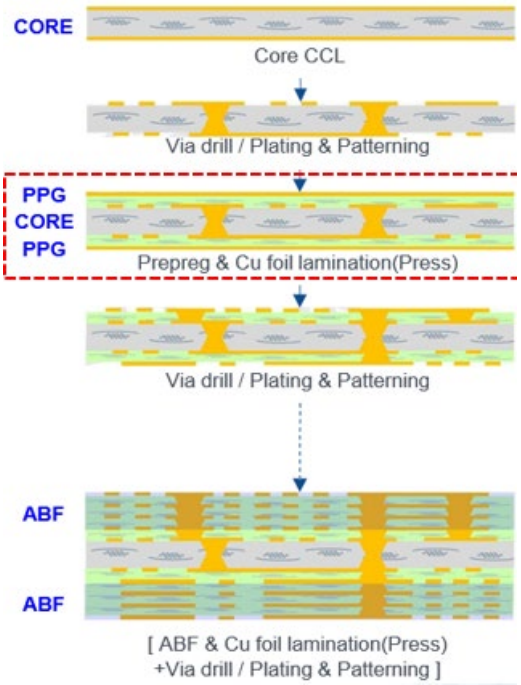


Figure 10. The MLC manufacturing process.

The Lower CTE + Thicker Core

For large body sizes, substrate suppliers are trending toward larger and thicker for warpage mitigation solutions. Before finalizing a large heterogeneous package, warpage simulations were run with existing products to determine which ones are primary considerations for 40x40-mm FCBGAs. Figure 9 and Figure 10 show the factors being considered.

Leg	Core	Core thickness (um)
POR	E705G	820
Leg1	E705GLH	820
Leg2	E705G	1240
Leg3	E705GLH	1240
Leg4	E795GLH	820
Leg5	E795GLH	1240

Figure 11. DOE Legs for warpage simulation.

	Type	Tg (°C)	CTE(α1/α2),ppm	Modulus(E1,E2), Gpa
Die	Silicon	-	2.6	129.5
Solder Mask	SR7300GRB	174	35/115	2.6
ABF	GL102F	153	20/49	13/0.13
Core	E705G	250~270	7.5/3	23/14
Core	E705GLH	250~270	5.5/2.5	29/18
Core	E795GLH	260~290	4.75/2	32/26
UF	NAU-47	110	28/105	9.9/0.13

Figure 12. Core/build-up attributes

Package type		FCBGA
Structure	Body size	40x40mm²
	Die thickness	0.775mm
	Substrate thickness	16L 1.532mm
BOM	ABF	GL102F
	Core	E705G or E705GLH or E795GLH
	Soldermask	SR7300GRB
	Underfill	NAU-47

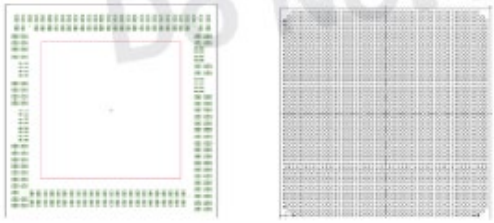


Figure 13. Package look

The specification is 250 µm, but the first build performance is 297 µm~332 µm (Avg. 312 µm) measured by ball scanner with physical finished goods. Figure 11 shows the simulation results.

Leg	Core	Core thickness (um)	Simulated copl. (um)	Meet SPEC. or not
POR	E705G	820	313	No
Leg1	E705GLH	820	280	No
Leg2	E705G	1240	237	Yes for Avg. copl., but potential risk may exist for some samples with Max. copl.
Leg3	E705GLH	1240	204	Yes
Leg4	E795GLH	820	263	No
Leg5	E795GLH	1240	190	Yes

Figure 14.1. Coplanarity results.

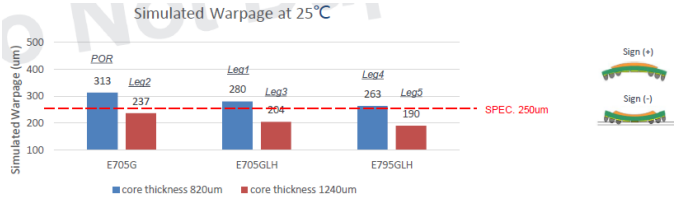


Figure 14.2. Coplanarity results.

Interpretation/Conclusion for the Simulation

Despite E795G(LH) assessed as producing the lowest CTE and shrinkage, it conveys a message that a thicker core helps reduce warpage more than a low CTE core. Since the actual results with physical materials would be differentiated from the simulation, low CTE, low shrinkage and high modulus deserve consideration to make package behavior stiffer and flatter. Eventually, this approach leads to improved package warpage. Figure 12 represents the choice of either higher or lower for CTE, shrinkage and modulus parameters. Typically, the users for large + high layer devices tend to pick E-795G (LH). As of 2024, E-705G(LH) is preferred as the manufacturer available core + lowest CTE while E-795G (LH) has not been seen in production at a substrate manufacturer.

	Condition		E-705G			E-795G	
			E705G	E-705G(X)	E-705G(LH)	E-795G	E-795G(LH)
Glass type	-		E	E & S	S	E	S
Tg	TMA	'C	260	260	260	280	280
	DMA		300	300	300	350	350
CTE	a1 (X,Y)	ppm/C	5.9	4.5	2.8 Improved CTE	4.0	0.7 Improved CTE
	a2 (X,Y)		3.5	2.0	1.5	1.0	0.5
Shrinkage	-	%	0.23	0.23	0.23	0.08	0.08 Improved shrinkage
Flexural Moduls	A	Gpa	33	35	38	38	43 High modulus

Figure 15. Core choice for "R" supplier.

Cu Foil % Balance

One of the FCBGAs encountered bump shorts at 4-corners of a silicon die while the substrate seriously shapes a smile vs. almost zero warpage with a silicon die.

Package/substrate information

- Package/die size: 19 x 19/8 x 10 mm
- Under-bump metallization (UBM) size/bump pitch: 70 * 90/min.130 µm
- Substrate thickness/layer/build-up/core: 0.49 mm/6 layers/ABF GL-102/ HL 832 NSF type LCA/0.2 mm
- BGA pitch/raw ball size/count: 0.5/0.3/almost full grid array

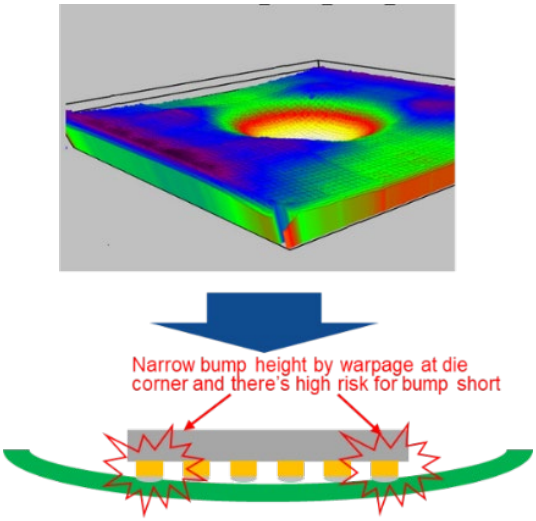


Figure 16. Bump shorts at die corners.

As a result of mapping frequent bump short spots and substrate layer's metallization, certain layers (L3 and L5) have lower Cu foil ration (percentage) than other layers (see Figure 14).

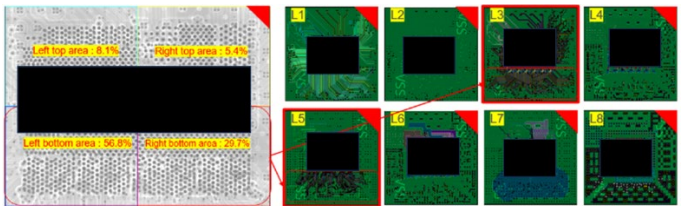


Figure 17. Layers L3 and L5 show a thinner distribution of Cu.

Another finding associated with bump shorts is the smile warpage gets more pronounced when the temperature is raised. Design guidelines dictate a balance across all layers, if possible. Figure 15 shows raw substrate differences between the package (PKG) and the die areas.

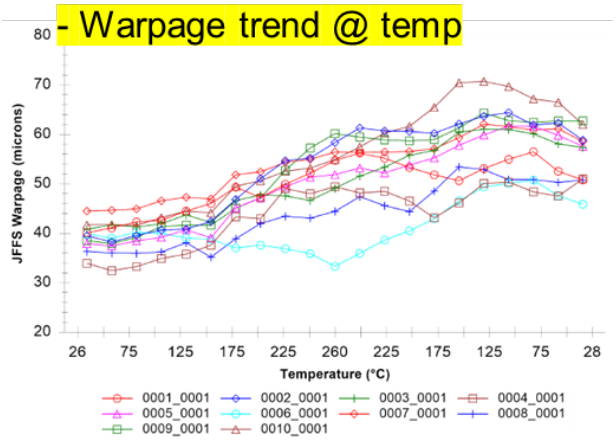


Figure 18.1. Shadow Moiré of raw substrate – entire area

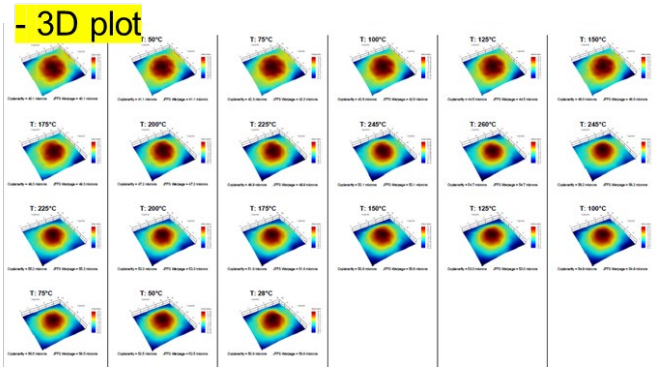


Figure 18.2. Shadow Moiré of raw substrate – entire area

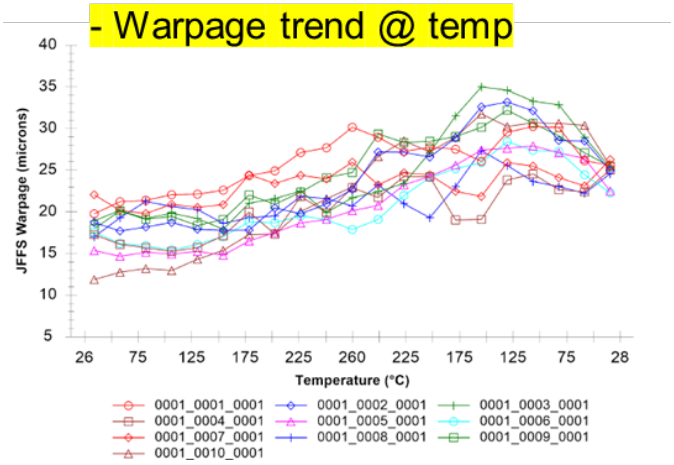


Figure 18.3. Shadow Moiré of raw substrate – die focus

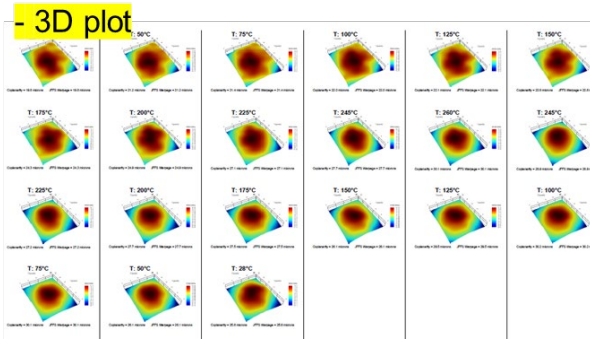


Figure 18.4. Shadow Moiré of raw substrate – die focus

Cu Foil % Imbalance or Tweaking

Instead of using Co foil % balance for the purpose of achieving a flatter substrate to reduce warpage, the imbalance idea is to manipulate warpage behavior by tweaking the Cu thickness with an already established design when the package encounters warpage issues. It is associated with copper's CTE (expanding at high & shrinking at low temperature). Figure 17 shows substrate warpage trends for the different layers in two different phases vs the process of record (POR).

		POR	Phase A	Phase A
SR	AUS-SR1	0.015	0.015	0.015
Lay1	Copper	0.015	0.015	Thick CuT
Lay1-2	GL102F	0.025	0.025	0.025
Lay2	Copper	0.015	0.015	Thick CuT
Lay2-3	GL102F	0.025	0.025	0.025
Lay3	Copper	0.015	0.015	Thick CuT
Lay3-4	GL102F	0.025	0.025	0.025
Lay4	Copper	0.015	0.015	Thick CuT
Lay4-5	GL102F	0.025	0.025	0.025
Lay5	Copper	0.018	0.018	Thick CuT
Core	E705GLH	1.200	1.200	1.200
Lay6	Copper	0.018	Thin CuT	Thin CuT
Lay6-7	GL102F	0.025	0.025	0.025
Lay7	Copper	0.015	Thin CuT	Thin CuT
Lay7-8	GL102F	0.025	0.025	0.025
Lay8	Copper	0.015	Thin CuT	Thin CuT
Lay8-9	GL102F	0.025	0.025	0.025
Lay9	Copper	0.015	Thin CuT	Thin CuT
Lay9-10	GL102F	0.025	0.025	0.025
Lay10	Copper	0.015	Thin CuT	Thin CuT
SR	AUS-SR1	0.015	0.015	0.015

Unit: mm

Figure 19.1. Substrate warpage trend.

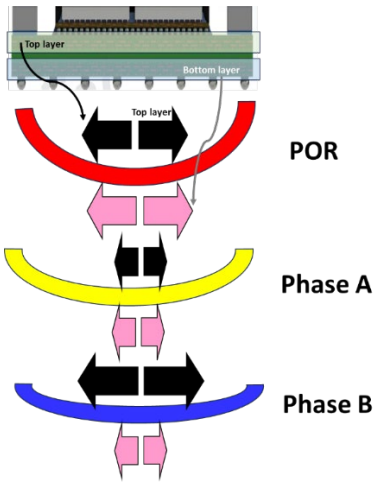


Figure 19.2. Substrate warpage trend.

Copper Core Ball

Separate from the substate approach, copper core balls were proposed to secure/maintain stand-off ball height at the package corners. Typical warpage behavior for large heterogeneous packages occurs when they return to room temperature (crying shape) from peak temperature (smiling shape). In this case, the solder balls at the package's corners get stressed and collapsed more than those at the center of the package. In the worst case, with severely collapsed ball height, solder balls are likely to be bridged at the package corners by crying package warpage. The application of Cu core balls has been used in an interposer Package-on-Package (PoP) design for smartphone applications (see Figure 18). To combine bottom and top interposer PCBs in the environment of fine ball pitch and static collapsed ball height, Cu core balls are mandatory.

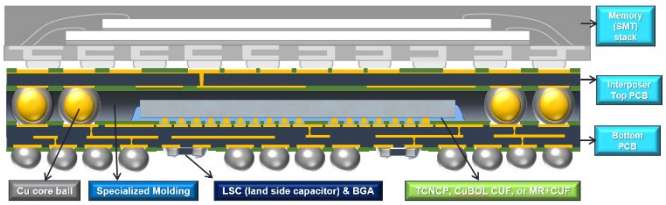


Figure 20. Amkor's Interposer PoP design.

As shown in Figure 19, metal copper balls are plated with nickel (Ni) and then solder on the external layers. This approach is compatible with the existing solder ball process. Since the melting point of copper core is over 1,000°C, it keeps the required standoff dimension after reflowing (see Figure 20).

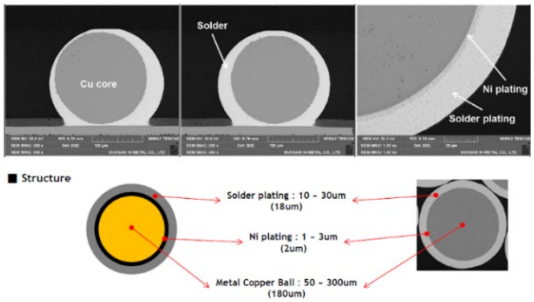


Figure 21. Cross-section of Cu-core ball.

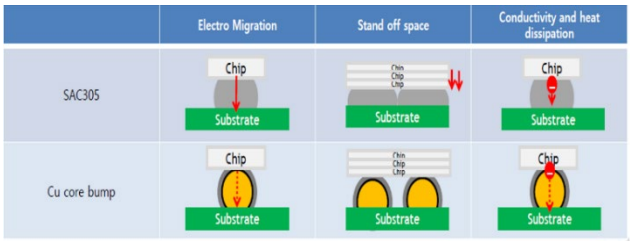
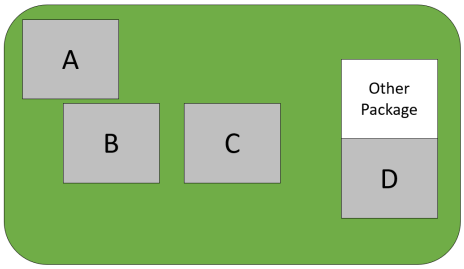


Figure 22. Post reflow collapsed ball comparison.

Board Level Beyond Package Level

When designing a PCB for the end products, it is important to consider how package placement will affect the warpage of the board during the reflow process. Placing the package near other packages, near edges of the board, or even off-center of the PCB could affect the overall warpage of the PCB. Board assemblers should review simulations or other data to determine the best placement of each package on the PCB to minimize board-level warpage. This could reduce any stress placed on certain areas of the board due to warpage around a package's mounting location. Figure 21 shows the results of different board placements and warpage.



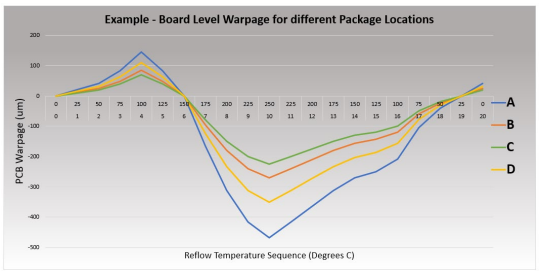


Figure 23. Package warpage on PC board.

Conclusions

Heterogenous integration enables significant functionality increases at the package level, but it will bring additional challenges in controlling warpage. With the various methods of reducing warpage outlined in this paper, package engineers, designers, and assemblers, can better understand how to best utilize recent findings to manage the package. From the silicon designer to the product assembler, everyone needs to consider how they can utilize heterogenous technologies to meet the needs of their customers. This paper has sought to provide additional support on how to combat the downsides that occur as the industry shifts towards a more heterogenous packaging approach.

Finally, the fishbone analysis (Figure 24) pictures what kind of factors are involved in warpage prediction.

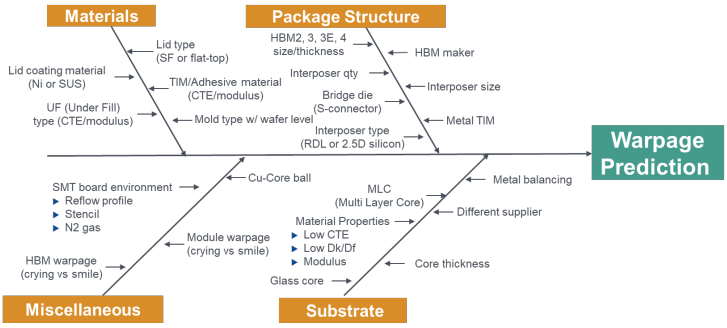


Figure 24. Fishbone analysis

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