Heterogeneous integration structure - FOSub for high end product substrate development

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Abstract

This paper introduces an innovative new structure designed to achieve the highly growth of High speed computing (HPC), especially the application for Generative Artificial Intelligence (Generative AI) and Internet of things (IoT). In the ever-evolving landscape of Generative AI, advancements have been remarkable, albeit accompanied by a growing reliance on Graphics Processing Units (GPUs) and the significance of computational processing systems. Traditionally, both GPUs and CPUs have utilized Ball Grid Array (BGA) boards coupled with either Flip-Chip on Substrate (FOCoS) or Chip-on-Wafer-on-Substrate (CoWOS) packaging. These configurations involved the stacking of multiple layers of substrates to achieve the high speed computational performance. However, this paper presents a novel structure which combine both the Fan-Out Redistribution Layer (RDL) & substrate technology. This breakthrough not only marks a significant leap in the capabilities of substrate manufacturing processes but also enables the attainment of a remarkable line width and spacing of L/S=2/2um. The consequential advantages include reduction in processing time and a substantial enhancement in the overall yield of the manufacturing process. Also, the structure has a mainly improve by the Fan-Out technology, can connect the top die without silicon interposer, and different from the Flip-Chip on Substrate (FOCoS) structure with the solder free connection.

Through the comparison of electrical simulations and actual samples, the study demonstrates that the performance of the new packaging structure is comparable to traditional 4-2-2L BGA boards, with no significant loss observed in the S21 parameter. Furthermore, by employing Fan-Out RDL technology, the number of substrate layers can be reduced, and compatibility with the 4-2-4L FOSub structure is achieved by utilizing Redistribution Layers (RDL) effectively. Encouragingly, reliability tests have been successfully passed, including PKG MSL3/TCT1000 cycle tests, further validating the reliability and stability of the new packaging structure.

Key words

Heterogeneous, Fan-Out, Substrate, FOSub

I. Introduction

The evolution of semiconductor packaging structures shows in Fig.1, IC packaging is closely tied to the demands of end-system products. To meet the trends of multitasking and miniaturization, the direction of integrated circuit packaging technology has mainly focused on higher density, higher pin counts, thinner profiles, and smaller sizes. From the early days of device packaging forms from Lead frame, wire bond, flip chip, system in package, and now on with advance package with 2.5D / 3D structure, such as CoWOS and FOCoS represents a significant leap in semiconductor technology, catering to the burgeoning needs of various high-performance applications such as IoT, AI, HPC, and Automotive. [1] [2]

Decade	Major IC Packaging Inventions
1970s	Dual In-lin Package (DIP), Ceramic Integrated Circuit Package (ICP), Quad Flat Package (QFP), Small Outline Package (SOP), Leadless Chip Carrier (LCC)
1980s	Surface Mount Technology (SMT), Pin Grid Array (PGA), Ball-Grid Array (BGA)
1990s	Quad Flat no Leads Package (QFN), Chip-Scale Package (CSP),
2000s	System-In Package (SiP), Package on Package (PoP),
2010s	Wafer-Level Package (WLP), 2.5D ICs, 3D ICs,
2020+	MCMs, 3D SoCs

Fig 1. The Evolution of IC Packaging

ASE create the FOSub structure (Shown in Fig.2) demonstrates the industry's dedication to pioneering new solutions. The fusion of ASE's Fan-Out technology with a substrate has given rise to an innovative packaging structure that not only improves the substrate's line space capability but also delivers electrical performance that rivals that of conventional packaging substrates.

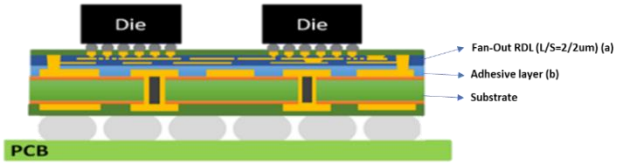


Fig.2 FOSub structure

The FOSub lineup which shows in Fig.3 is a designed to meet a variety of needs for advance packaging, offering different configurations that not only improve line width and spacing but also cut down on manufacturing cycle time. This leads to a significant increase in production yield and introduces an innovative solution for IC packaging.

	FOSub-R	FOSub-C	FOSub-E
Structure			
	Substrate + Fan out RDL	Build up substrate + Coreless substrate	Fan-Out RDL replace ETS substrate layer
Fine Line capability	Yes	-	Yes
Yield improve	Yes	Yes	Yes
Cycle time benefit	Yes	Yes	-

Fig.3 FOSub line up

Building upon the discussion of high-density, high-performance, and High I/O packages, it's important to consider the broader implications of these technological advancements. As package sizes increase to accommodate more layers and complex circuitry, the industry faces the challenge of maintaining high yield rates for fine line multi-layer build-ups. The FOSub structure is a strategic innovation designed to address this challenge.

By integrating Fan-Out technology with Substrate technology, FOSub combines the fine line capabilities of Redistribution Layers (RDL) and high I/O capability with substrates, aiming to enhance the line width and spacing capabilities of the substrate. This not only improves the yield of the circuitry but also targets of large-size, high-density packages with fine line design.

To connection between Fan-Out and substrate involves using an adhesive film for bonding. The Fan-Out wafer is cut, and dies are produced using a face down structure. Then the Fan-Out carrier been removed, and the remaining Fan-Out, after carrier removal, undergoes a heat press bonding process. And for the conductive connection, A specially designed of Connect Via is used for conductive conduction, drilling from the top of the Fan-Out though the adhesive layer to the substrate. And Fig.4 shows the structure that we overcome, the difficulties of heterogeneous materials which has the different absorption for laser drill. Control the via profile with taper ratio >70% and with good via profile shows in Fig.5. And the via has been well filled with plating copper.

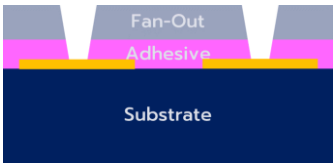


Fig.4 Heterogeneous material drill

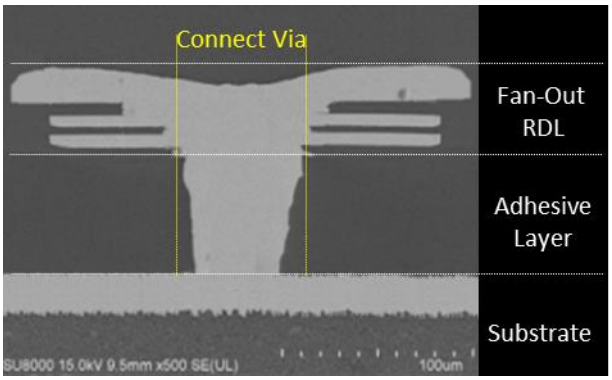


Fig.5 FOSub Connect Via

This Connect Via connects to the Via Pads reserved in the substrate design and is filled through electroplating, establishing a connection between the two structures. As the process flow shows in Fig. 6 (b). After completing the Connect Via electroplating process, the Top Die can be directly bonded onto the FOSub by Flip chip bond. Compared to the FOCoS process show in Fig.6 (a) , which requires a Chip first procedure above the RDL, the risk is significantly lower. [4]

With same process concept, this process can be used at FOSub-C structure, by replacing Fan-Out to Coreless substrate, and also binding Coreless substrate with adhesive layer, connect by Connect via through the adhesive to substrate.

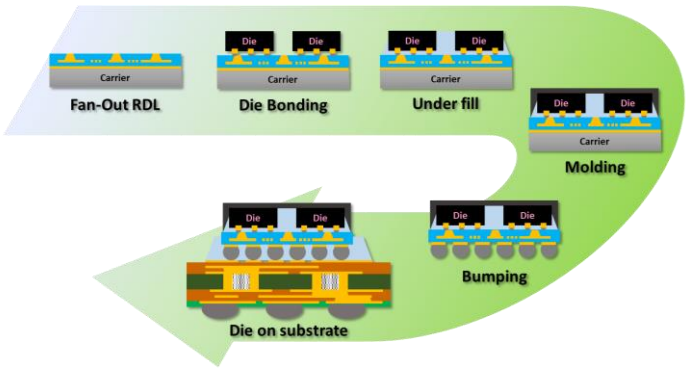


Fig.6 (a) FOCoS process flow

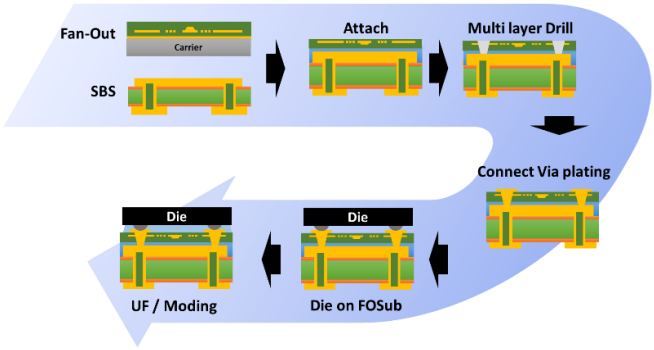


Fig.6 (b) FOSub-R process flow

The FOSub structure involves the separate production of Fan-Out and substrate layers. Through a holistic package redesign, routing is partially shifted to the Fan-Out layer, and the original line design is reduced to L/S=2/2um, allowing a reduction in substrate layer layout space to achieve layer reduction and overall board thickness reduction. Leveraging the high yield of fine lines in Fan-Out processing, with a yield rate exceeding >90%, and combining it with a mature substrate manufacturing process, FOSub can effective improve overall yield. In Fig.7 shows that, based on the yield result for normal substrate and FOSub (RDL yield and substrate yield), larger package shows with larger yield benefit. For example, 90x90mm^2 package size with a yield gap of 45% between FOSub and FCBGA. (Base on FCBGA substrate layer 5-2-5L benchmark with FOSub 2L RDL + 2-2-2L Substrate). [3]

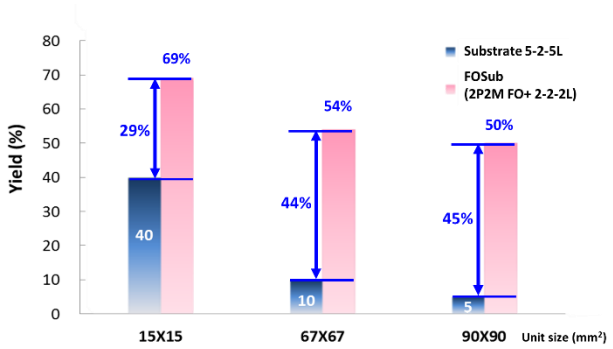


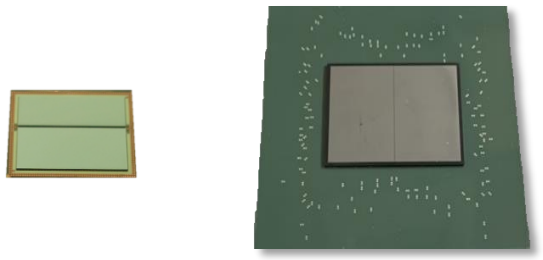
Fig 7. Yield benchmark with FCBGA / FOSub for various package size

FOSub can potentially reduce the overall number of layers required in a package by higher density of Redistribution Layers (RDL) design. This reduction is significant as it not only simplifies the manufacturing process but also contributes to the miniaturization of electronic devices. With the trend towards smaller and more powerful devices, such as wearables and implantable medical devices, the ability to pack more functionality into a smaller space is crucial.

In conclusion, the development of the FOSub structure and its applications represent a significant step forward in semiconductor packaging technology. As the industry continues to evolve, we can expect to see further innovations that will drive the miniaturization and performance of electronic devices, ultimately shaping the future of technology.

II. Large package design

Based on the yield prediction model's outcomes, we design prototype with a larger device to verify yield result. At the previous study, first FOSub concept proven with prototype that utilized a small package size of 14x17mm^2 shown in Fig.8 (a), the test vehicle's package size has been expanded to 67.5 x 67.5mm^2 which shown in Fig.8(b). The design with a 3-2-3L buildup substrate, plus an 2P2M Fan-Out RDL (2 layers of passivation + 2 layers of RDL) attached on the substrate. This test vehicle was processed through the FOSub process flow up to the Top Silicon Die assembly and has passed the precondition package level MSL3 & package level TCT 1000 cycle. The Scanning Acoustic Tomography (SAT) results showed in Fig.9, without delamination or bubble formation. An X-section analysis shown in Fig.10 of this sample revealed the inclusion of 2um RDL lines and the FOSub structure's Connect Via.



(a) 14x17mm^2 FOSub prototype

(b) 67.5x67.5mm^2 FOSub prototype

Fig.8 (a) Small / **(b)** Large package size FOSub test vehicle

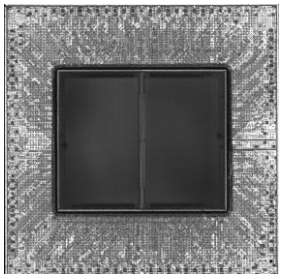


Fig. 9 Pre-Con MSL3 TCT 1000 cycle SAT result

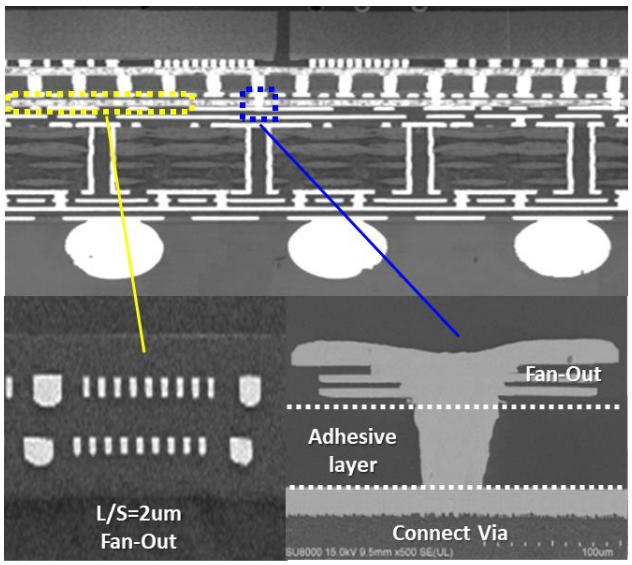


Fig.10 Large package FOSub prototype X-section

The yield results, as shown in Fig.11, indicate that in the case of the first sample build, by fabricating the Fan-Out and Substrate separately, the original 4-2-4L Substrate can be split into a 3-2-3L plus a 2P2M Fan-Out. This approach effectively utilizes the precision of the Fan-Out process to enhance yield. For the standalone Fan-Out, the yield reaches 96.98% for the 2P2M structure measuring 67.5 x 67.5mm^2 with 2um fine lines. When combined with the substrate yield of 65.21%, the overall yield amounts to 71.19%. This is a significant improvement over the 31.42% yield for the 6-2-6L with L/S=12/12um lines, representing an increase of 39.77% for substrate final yield.

	FOSub (3-2-3L + 2P2M)	6-2-6L Substrate
Fan-Out Yield	96.98%	NA
Substrate Yield	65.21%	NA
Final Yield	71.19%	31.42%

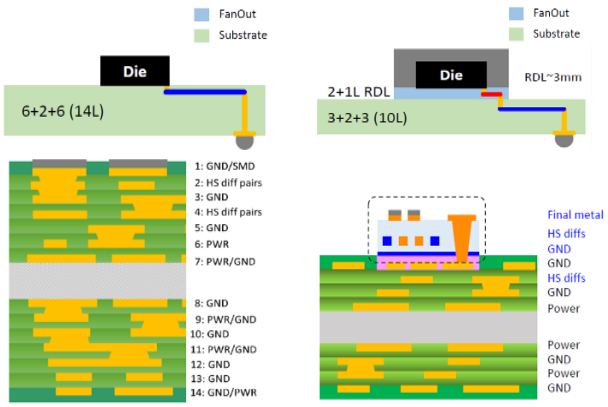
* Fan-Out L/S=2/2um, Substrate L/S= 12/12um
* Package Size : 67.5 x 67.5mm
* Fan-Out Size : 67.5 x 67.5mm

Fig.11 FOSub Yield result benchmark with Normal substrate

III. Electrical performance simulation result

The FOSub structure introduces a novel design to IC packaging, yet its electrical properties still require verification. This paper will conduct electrical simulations and actual measurements on large package samples to compare the electrical differences between traditional FCBGA substrates and the FOSub structure.

The comparison between the two structures, 6-2-6L FCBGA and 3-2-3L with 2P2M Fan-Out RDL, was modeled, with the stacked structure shown in Fig.13. The simulated line segment length is approximately 21mm, and the frequency range selected extends to 50GHz. As seen in Fig.14, there is no significant difference in the S-Parameters between the traditional FCBGA (red line segment) and FOSub (blue line segment).



(a) 6-2-6L Traditional FCBGA

(b) 3-2-3L +2P2M FOSub

Fig.13 FOSub & FCBGA simulation model

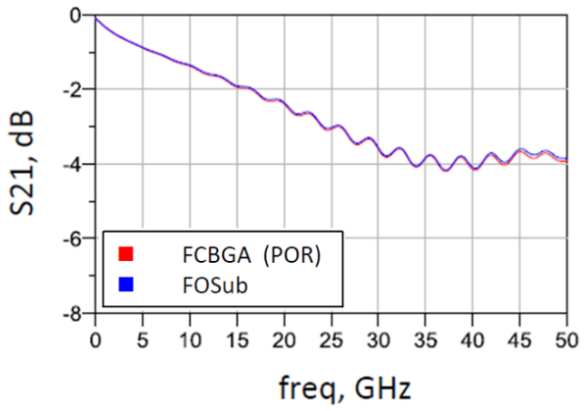


Fig. 14 (a) Return Loss (Die Side)

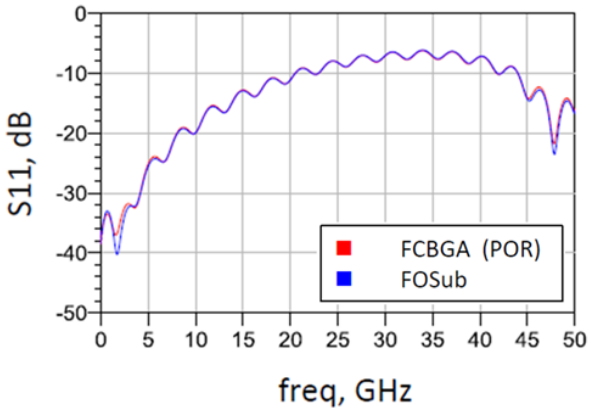
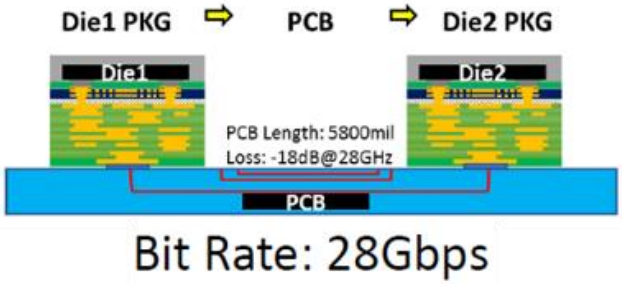
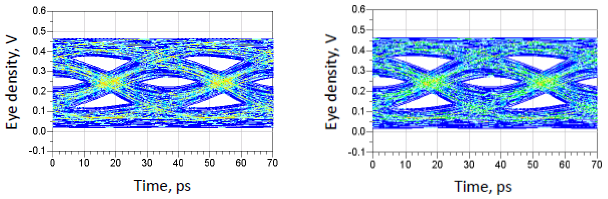


Fig. 14 (b) Return Loss (Ball Side)

Furthermore, eye diagram simulations shown in Fig.15 were conducted to compare with an 18dB PCB loss at a bit rate of 28Gbps, an eye height (EH) of 38mV, and an eye width (EW) of 17.9ps. The results indicate that the eye diagram of FOSub is comparable to that of the traditional FCBGA, with no notable differences observed.





(a) FCBGA (b) FOSub

Fig.15 Eye diagram

IV. Conclusion

This research not only confirms the structural benefits of FOSub but also demonstrates its potential to match or even surpass the electrical performance of conventional packaging solutions. The findings suggest that FOSub could be a viable alternative for high-density, high-performance IC packaging, offering improvements in yield and process efficiency without compromising on electrical integrity. As the semiconductor industry continues to innovate, technologies like FOSub are expected to play a crucial role in the development of next-generation electronic devices.

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