Selecting Strip-Based or Singulated Laminates in Chiplet Packaging

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Abstract
Deciding whether to pursue strip-based or singulated laminate substrates for chiplet packaging has become more important as technological capabilities of both architectures have grown enough to overlap broadly. This paper investigates, analyzes, and prioritizes the factors that impact the relative suitability of laminate-based assembly options for chiplet-based and other advanced packaging. A mathematical model is constructed that compares assembly outputs such as cycle time, material usage and cost for a wide range of inputs, such as package body size, bill of materials and device functionality requirements. The two substrate architectures are compared over these parameters, and crossover points for each input parameter are calculated, delineating which architecture is best suited given any set of inputs.

Key words
Chiplet Packaging, Strip-Based Laminates, Singulated Laminates

I. Introduction

Advanced packaging on laminate substrates has moved from the siloed domains of strip-based flip chip Chip Scale Packaging (fcCSP) assembly versus singulated Flip Chip Ball Grid Array (FCBGA) assembly to a spectrum with ever-increasing overlap. Gone are the days when down-selection was based merely on body size. Meeting the complex design requirements of next-generation devices requires navigating the interplay of far more design variables.

In parallel, the recent trend to deconstruct complex chips into monofunctional chiplets [1] has further elevated the importance of assembly-driven package design. Chiplet-based devices shift the decision point for functional integration from the die design to the package design. For laminate-based packages, this raises the inevitable question of which laminate assembly strategy to adopt between strip-based fcCSP and singulated FCBGA. Among other parameters, substrate type impacts technical capability and yield at both the substrate supplier and the assembly house. It therefore also affects cost through each subsequent step of the supply chain.

The decision to pursue strip-based or singulated substrate assembly takes many variables as inputs, among them body size, substrate layer count, routing density, package bill of materials and die size(s). These package attributes form a large part of the traditional selection method but deciding between strip-based fcCSP and singulated FCBGA also requires oft-overlooked items such as substrate strip yield, assembly yield, and process speed. These metrics, in turn, conspire to drive the imposition of yield minimums required of substrate suppliers by assembly houses. In fact, these artificial minimum yield requirements can be enough to elevate strip-based fcCSP to a higher-cost option than singulated FCBGA. Yet, as chiplet-based multi-functional systems become more prevalent [2] and as both substrate technologies remain equally capable of meeting product performance demands, cost will become the deciding factor in down-selection. In this paper, substrate strip yield, body size, chiplet count and assembly process time are considered as contributing factors toward the down-selection of optimal substrate design between strip-based and singulated laminates.

II. Building a Model

A. Strip-Based Assembly Process Speed

To evaluate when a design calls for strip-based laminates instead of singulated laminates, a simple model of assembly process speed was created. This is intended to be a broad term as it can be used to estimate a single process (such as chip attach, transfer molding, etc.) or an entire assembly process. The variables of an individual assembly process

may change, from the general model, but the rubric remains.

The term *u(x)* represents "assembly speed," the speed at which a given process can be run, in terms of number of units per time. For a strip-based laminate, it is defined as:

$$u(x) = \frac{n(1-x)}{n(1-x)t_p + t_c} \quad (1)$$

where n is the number of units on the strip, t_p is the per-unit process time and t_c is the per-unit average time for loading and unloading the strip after the process has been completed.

As strip-based units are processed in large batches, the per-unit t_c is quite small in practice. The variable x represents the percentage of units on each strip that have yielded out by the laminate supplier, the so-called *x-out*. These are not processed during assembly, and often appear with an X mark on them to indicate they should not be used in assembly. The expression *(1-x)* is therefore the yield of the strip, and it also serves as a minimum specification under which laminate suppliers may not ship out such defective strips.

B. *Impact of Strip Yield on Process Speed*

A commonly required specification of strip designs is a minimum x-out rate. However, substrate manufacturers will often request that the x-out rate of a given strip design be increased (allowing lower yields) to reduce their internal scrap rate. Equation (1) demonstrates that processing speed does not vary linearly with x-out percentage, which opens up the possibility of assembly houses to accept some changes in x-out rate, depending on where the original spec level is set. This can be demonstrated by differentiating (1):

$$u'(x) = \frac{-t_c n}{(t_p n(1-x) + t_c)^2} \quad (2)$$

From (2), $u'(x) < 0$ over $\mathbb{R}$. implying that small values of x are desired, and that *u(x)* therefore reaches a maximum on $x \in [0,1]$ at 0. This is naturally expected, as lower x-out and higher yields allow for faster process time per unit, since more units are processed on a strip for every load/unload cycle, t_c.

Fig. 1 plots u(x), highlighting the real-world domain of [0,1]. Process speed maximum is $\frac{n}{nt_p + t_c}$, while it falls to 0 at $x = 1$, i.e. when all units on the strip are yielded out. The asymptotes fall outside of the real-world domain and can be verified by noting that the vertical asymptote exists at an x-out value larger than 1, and that the horizontal asymptote requires $t_c = 0$, both impossibilities.

As (2) demonstrates and Fig. 1 confirms, the slope of u(x) is less negative near $x = 0$, and more negative near $x = 1$. This means that the impact to process speed is muted when

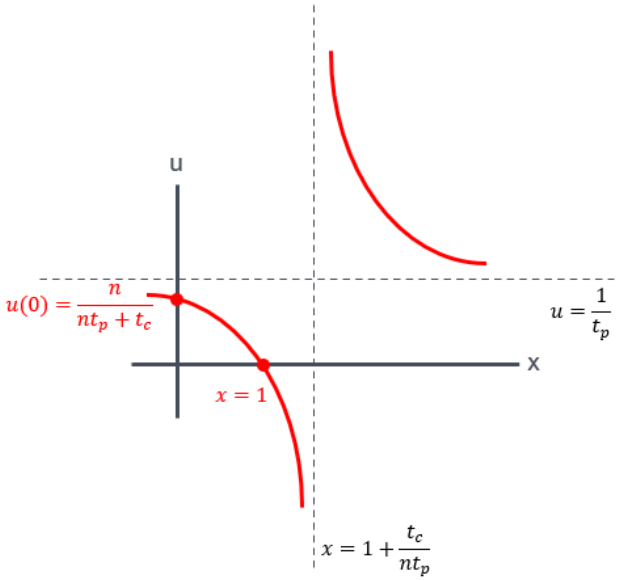

Fig. 1: Process speed as a function of x-out rate, with domain of [0,1] noted.

the x-out rate changes from a low value (higher yield) than when it moves from a high value (lower yield).

This result is important during production ramp stages of package design. Oftentimes, a substrate supplier will request a relaxation of the maximum x-out rate specification, due in part to a number of possible reasons. These include a more challenging design process, a high scrap rate and limited available raw materials. Such requests can be entertained when the process of record (POR) spec level is already tight but may be rejected when the POR spec is already loose.

To illustrate the difference between change requests from tight specs and from loose specs, compare (2) at values of $x = 0$ (100% strip yield) and $x = 0.5$ (50% strip yield).

$$u'(0) = \frac{-t_c n}{(t_p n + t_c)^2} \quad (3)$$

$$u'(0.5) = \frac{-t_c n}{(\frac{t_p n}{2} + t_c)^2} \quad (4)$$

Comparing (3) and (4), note that $u'(0) > u'(0.5)$, and hence that a supplier's change request to lower the strip yield spec from 100% would cause less of an impact to process speed than a similar change request for a device already at a lower yield.

Equations (3) and (4) can be generalized by differentiating (2):

$$u''(x) = \frac{(2t_p^2 t_c n^3)x - (2t_p^2 t_c n^3 + 2t_p t_c^2 n^2)}{(t_p n(1-x) + t_c)^4} \quad (5)$$

At the two edges of the domain [0,1], $u''(x,t) < 0$. In fact, $u''(x,t) > 0$ only when $x = (1 + \frac{2t_p t_c^2 n^2}{2t_p t_c^2 n^3})$, which is outside the real-world domain. So, not only does process speed decrease faster around lower substrate yields, but the rate of change itself increases the further the initial yield is already away from $x = 0$. Supplier requests for yield minimums are best at high initial yields, and they more quickly accelerate to larger impacts on process speed at lower yields.

III. Singulated vs. Strip-Based Processing

A. Impact of X-out Rate on Substrate Construction

Historically, singulated substrates have been used for larger monolithic packages or as interposers for chiplet packages but as processing methods have improved over time, there is a large overlap between the suitability between singulated and strip-based packages based solely on such attributes. And since the x-out rate of a strip-based substrate can have a large impact on process speed, the next step is comparing it to singulated laminate processing, assuming both packages are available at similar prices from substrate suppliers.

Singulated substrate processing speed can be generalized as:

$$u_s = \frac{1}{t_{ps}+t_{cs}} \tag{6}$$

where t_{ps} and t_{cs} represent process time and load/unload time for a singulated unit, respectively. Unlike with strip-based substrates, the yield of singulated substrates does not play a role in the assembly process, though it would have an impact on the substrate cost.

From (1) and (6), the crossover point at which strip-based and singulated units achieve the same process speed can be determined:

$$t_{ps} + t_{cs} = t_p + \frac{t_c}{n(1-x)} \tag{7}$$

When $t_{ps} + t_{cs} > t_p + \frac{t_c}{n(1-x)}$, strip-based substrates should be down-selected, and when $t_{ps} + t_{cs} < t_p + \frac{t_c}{n(1-x)}$, singulated substrates are the better construction.

B. Example Case 1: Strip Yield Spec Reduction

Consider a case where a strip-based design was selected as the POR, but the substrate supplier requests to apply a lower yield minimum to ship out strips to the assembly house. For this exercise, set $t_{ps} + t_{cs}$ to 1.07 seconds, t_p to 1.00s, t_c to 0.9s, gross units per strip, n, to 100, and the POR yield minimum to 90%, so $x = 0.1$. In this initial condition, strip-based design is appropriate, as the left-hand side (LHS) of (7), 1.07s, is greater than the right-hand side (RHS), 1.067s, implying that strip-based process speed per unit is fastest for strip-based assembly.

If the substrate supplier requests a reduction of the strip yield minimum threshold to 80%, then $x = 0.2$, and the RHS grows to 1.075s. Now, the singulated substrate process speed is quicker than strip-based, and such a change would instigate a redesign of the substrate itself, removing the unit design from the strip and procuring it in singulated form instead. In practice, this can be a time-consuming process, as the design must be updated, and new substrates ordered. Either the design must remain in its unoptimized form to meet the program schedule, the team must wait for the new singulated substrates to be designed, ordered and delivered, or the request must be denied to the supplier. In all cases, a concession must be made. To avoid this situation, close work up front between assembly house and supplier is necessary so that realistic yield projections can be made for a given design, driving the correct course between strip-based or singulated substrate design.

C. Example Case 2: Increasing Body Size

Now consider the case where a customer needs to grow the body size of the package but wants to keep costs unchanged. This can occur when a system on chip (SoC) die is split into chiplets and intended to be attached to a single interposer. Since $n = f(b)$, where b is body size, decreases with increasing b, (7) shows that any decrease in n requires an equal increase in $(1 - x)$. This is expressed as:

$$1 - x_{new} = \frac{1-x}{1-a} \tag{8}$$

where a is the reduction in n due to the change in body size, and x_{new} is the new x-out rate required to keep $u(x)$, and hence costs, level after the body size change.

Therefore, if the current substrate strip yield is 70%, so $x = 0.3$, and the increase in body size results in a 10% decrease in n, so $a = 0.1$, the process speed would stay constant if the strip yield increased to 77.8%. The supplier would have to confirm if this increase in yield is possible, given the new interposer design with an added chiplet, or if yields would stay the same (or go lower) in the new package size. If the latter occurs, then costs will necessarily increase from slower process speed (as well as from larger substrate), and it would be wise to revisit whether strip-based interposer is still optimized over a singulated construction (see Case 1).

D. Example Case 3: Chiplets on Singulated Interposer vs. Strip-Based Packages

Finally, consider the case where many chiplets must be packaged and evaluate the implications of assembling them into single or multiple packages, as well as in strip-based or singulated constructions. This situation arises, for instance, when a new chiplet functionality must be added to an existing design, which does not otherwise have enough space to accommodate the design change. Optimizing for the speed of the chip attach process before designing a complex system solution can limit having to evaluate many designs in the engineering build stage, saving process time and material costs.

Now consider a POR design with two strip-based packages - each with two dies.

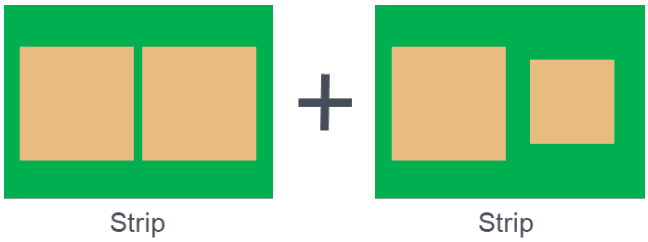

Fig. 2: POR design.

The die sizes in Fig. 2 can be the same or different, and for this example, consider three dies of equal size and one of smaller size. When a fifth chiplet must be added to the POR design, there are four system options to evaluate. Option 1 would be to combine all five chiplets onto one singulated interposer. Assume singulated due to the large body size required to house all five chiplets.

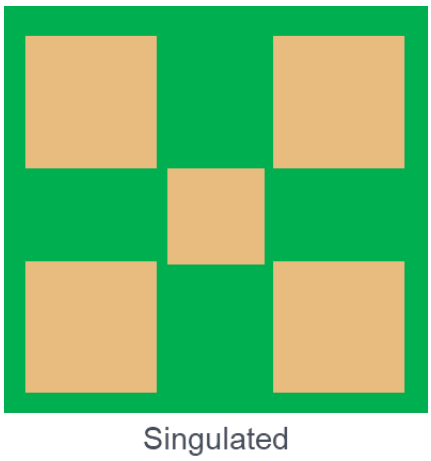

Fig. 3: Option 1 design.

In this case, for each option, optimizing for process time per unit assembled, T_i, is more appropriate instead of its reciprocal, process speed, as has been previously considered. This makes summing the impacts from more than one package in a given solution easier to calculate. That is:

$$T_i = \sum_i \frac{1}{u_i(x)} \tag{9}$$

For Option 1 in Fig. 3, therefore:

$$T_1 = 5t_{ps} + t_{cs} \tag{10}$$

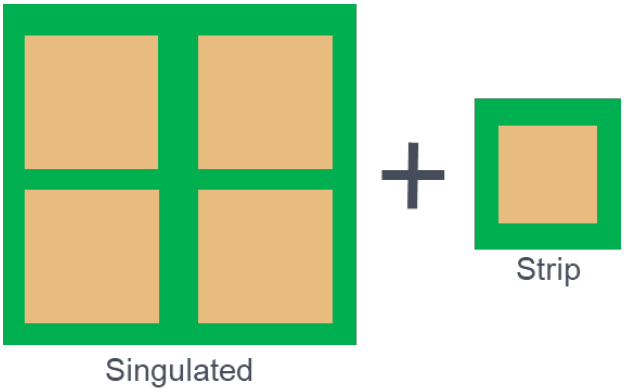

Fig. 4: Option 2 design.

Option 2 splits the system into two packages, one large interposer for four chiplets and one small strip-based package housing the smaller chip, as shown in Fig. 4. This kind of solution may be considered as an alternative to the inordinate cost of Option 1's substrate. Process time is expressed as:

$$T_2 = 4t_{ps} + t_{cs} + t_p + \frac{t_c}{n_1(1-x_1)} \tag{11}$$

where the subscripts on n and x refer to a substrate with one chip.

Comparing Options 1 and 2 and simplifying, we find

$$t_{ps} = t_p + \frac{t_c}{n_1(1-x_1)} \tag{12}$$

Further simplification occurs by noting $t_{ps} \sim t_p$ in the case of a chip attach process. That is, attaching a die onto a singulated substrate takes about as long as doing so onto a strip-based substrate would. The crossover point between Options 1 and 2 therefore satisfies:

$$0 = \frac{t_c}{n_1(1-x_1)} \tag{13}$$

Because RHS is strictly greater than LHS in (13), Option 1 is the faster process and should always be chosen, all other cost parameters being equal.

Next, consider two similar variants, both with two-die strip-based packages but with different three-die package constructions: Option 3 with the larger package on singulated and Option 4 with the larger package still in strip format, shown together in Fig 5.

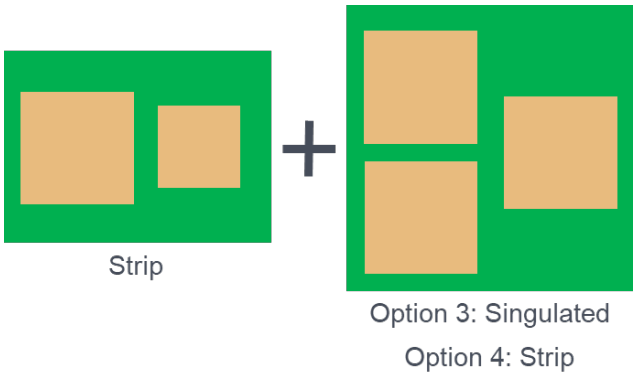

Fig. 5: Option 3 and 4 designs.

First, compare Option 3 to the previously considered Option 2. Again, the price of the larger interposer in Option 2 may require such a comparison, and it will be important to note if there will be an impact to process time and speed. Process time per unit of Option 3 is expressed as:

$$T_3 = 3t_{ps} + t_{cs} + 2t_p + \frac{t_c}{n_2(1-x_2)} \quad (14)$$

Finding the crossover point between Options 2 (11) and 3 (14), gives:

$$t_{ps} = 2t_p + \frac{t_c}{n_2(1-x_2)} \quad (15)$$

Again, RHS is greater than LHS, implying that Option 2 is the optimized approach for design in terms of assembly speed.

Thus far, larger packages with several chiplets are preferable in assembly to smaller packages with fewer dies. Now consider the comparison of two solutions with equal body sizes, but one solution containing chiplets on a singulated substrate and the other on a strip-based substrate.

Option 4 can be expressed as:

$$T_4 = 2t_p + \frac{t_c}{n_2(1-x_2)} + 3t_p + \frac{t_c}{n_3(1-x_3)} \quad (16)$$

Comparing Options 3 and 4, the process time per unit contributed by the two-die strip-based package drops out and results in:

$$3t_{ps} + t_{cs} = 3t_p + \frac{t_c}{n_3(1-x_3)} \quad (17)$$

which, when $t_{ps} \sim t_p$, reduces to:

$$t_{cs} = \frac{t_c}{n_3(1-x_3)} \quad (18)$$

Dividing the load/unload time for strip-based processing by the number of units on the strip will always lead to LHS > RHS, meaning Option 4, the strip-based construction, is always preferred.

III. Conclusion

As chip design continues to migrate from monolithic, large SoCs to smaller, single function chiplets, selecting the proper substrate construction becomes critical. In some cases, incorporating many chiplets onto a single interposer is preferable to separating chiplets into smaller packages to be assembled in strip format. While the assembly processes for each strip-based and singulated substrates may be similar, the speeds at which each process step can be completed is different. Thus, the process speed, which impacts cost, must be considered during the early design phase to avoid being stuck with a suboptimal solution when the product design is frozen.

For strip-based solutions, substrate yields are key parameters for early design decisions. Requests from substrate suppliers to lower spec limits after first builds are more acceptable if the POR spec is tight, but less so when the POR spec is already loose. The impact to process speed accelerates as the POR substrate yield spec moves away from 100%. In some cases, lowering the yield limit spec may even cause a strip-based solution to become less optimal than a singulated solution.

Materials cost, manufacturing complexity and customer preferences will always play a fundamental role in selecting the optimal substrate construction, but assembly speed and per unit process time become more important as the overlap in capability and cost between strip-based and singulated substrate constructions grows.

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