

Investigation for the influences of factors within the Semi-Additive Process (SAP) on nanovoid formation in the Cu-Cu interface by STEM analysis

Kanji Matsumoto, Hisamitsu Yamamoto
C. Uyemura & Co., Ltd.
1-5-1, Degchi, Hirakata
Osaka, 573-0065 Japan
Ph: 81-72-832-8171; Fax: 81-72-832-6559
Email: kanji-matsumoto@uyemura.co.jp

Abstract

Electroless copper deposition is widely used in the electronics industry. In recent years, electronic components tend to be densified as the performance of electronic devices increases. The densification of electronics components means the decreasing of conductor width and spaces formed as the circuit patterns and reducing the diameter of Blind Via Holes used as an interconnect between the circuit layers within the electronic substrates.

If voids exist in reduced diameter BVHs, the reliability of electronics components could decrease. Thus, voids formed in the electrolytic Cu / electroless Cu interface and electroless Cu / inner layer Cu interface and the cause of the formation of voids have been the focus of attention in recent years.

Although there are some studies regarding voids formation in the interfaces of electrolytic Cu / electroless Cu / inner layer Cu for such this reason, factors relating to the formation of nanovoids in the interfaces are not clearly mentioned.

Therefore, the purpose of this paper is investigation for various factors that could cause void formation in the interface. Experiments performed on actual substrates consisting of copper foil, electroless copper layer, electrolytic copper layer and glass epoxy resin are very practical and easy to understand. On the other hand, it will be hard to find out the root cause of void formation owing to too complicated processes for production of these substrates.

We adopted a special method of experiment to prepare samples in order to investigate the effect of just one factor from many factors. This method will be included in the process for preparing actual substrates for the formation of voids. STEM-EDX was used to confirm whether voids exist in the interface or not and the area of electroless copper layer is identified from EDX Ni-mapping results. AES also was used for analysis on surface of inner layer copper. The TEM lamellae were prepared with FIB.

The results obtained from these experiments clarify that the formation of voids was related to the presence of copper oxide on the inner layer copper.

Key words

electroless copper plating, nanovoids, SAP process, reliability, transmission electron microscopy, Printed Circuit Board

I. Introduction

Electroless copper (Eless Cu) deposition is widely used in the electronics industry and it is an essential technology in our daily lives [1]. The product developments have been achieved by miniaturization and densification of the internal electronic components. As long as the progress for electronic products is demanded, these trends will continue. The Printed Circuit Board (PCB) is a representative component among miniaturized components in products. Miniaturization of components means not only reducing the pitches between the conductors on the PCB but also reducing

diameters of Blind Via Holes (BVHs) used for vertical connections between the circuit layers. Recently, the quality of deposits in BVH is getting attention because there is the concern about decreasing of reliability caused by smaller Cu-Cu area in the reduced-diameter vias (Fig.1.1).

The BVH has two Cu-Cu interfaces (Fig. 1.2). One is the interface between Electrolytic Cu and Electroless Cu, the other one is the interface between Electroless Cu and Inner layer Cu. We will discuss the defects, especially the nanovoids, in this region. Additionally, we have divided the voids into three types by the positions of voids (Fig. 1.3).

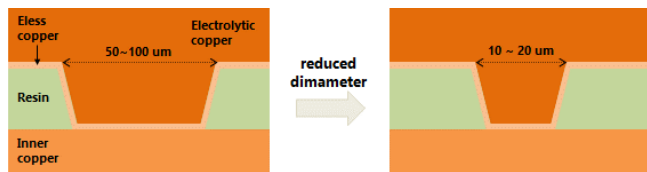


Figure 1.1 Cross section of Blind Via Hole

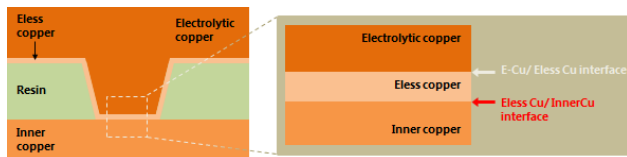


Figure 1.2 Three of Cu layer and two of Cu-Cu interface

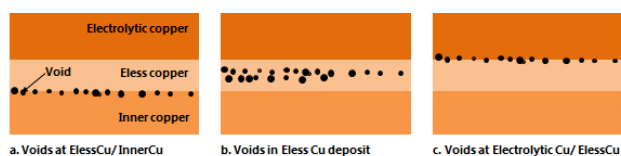


Figure 1.3 Classification for voids by formation position

- voids between Electroless Cu and Inner layer Cu
- voids in Electroless Cu deposit
- voids between Electrolytic Cu and Electroless Cu

In this report, we focus on “a. voids between Electroless Cu and Inner layer Cu” in order to avoid complicating the discussion and make it simpler.

There is the Semi-Additive process (SAP) to form PCB BVHs and most boards are manufactured by this process. We aimed to investigate the influence of various factors, which would be included in the process, on the nanovoid formation for obtaining knowledge for practical situations to manufacture the boards.

We illustrated Fig. 1.4 to indicate the image of the SAP. And we picked up factors that would be included in this process and indicated these factors in Fig. 1.5. From these Figures, it can be confirmed that the process to manufacture the substrate with BVH has various factors. Some studies for voids within BVHs have investigated the cause of void formation with practical substrates having BVHs [2]-[4]. Of course, these studies are easy to understand with practical knowledge. On the other hand, it would be hard to find out the obvious critical factors within the process from experiments using practical substrates because if we use these substrates made through such complicated processes to investigate and observe the Cu-Cu interface in the BVH, it might be that the observation results are affected mutually from factors in the process. Thus, we adopted a special experimental method to investigate only targeted items from the many factors being in the process.

We confirmed whether or not voids were at the interface

between electroless copper plating layer and inner layer copper with Scanning Transmission Electron Microscope (STEM: JEOL, JEM-F200). We also identified the electroless copper layer from Ni mapping results that were obtained by Energy Dispersive X-ray (EDX: JEOL, JED-2300T) in the same TEM and estimated the position of voids. TEM lamellas were prepared by Focused Ion Beam and Scanning Electron Microscope system (FIB-SEM: Hitachi High-Tech, XVision 210DB) and were thinned to 60 – 80 nm thick. In the course of investigation for the cause of void formation, we confirmed that an oxide layer on inner layer copper influenced the void formation, significantly. Therefore, we analyzed the thickness of oxide layer on inner layer copper with Auger Electron Spectroscopy (AES: JEOL, JAMP-9500F).

From the results shown in this report, it was clarified that the most influencing factor on the void formation was copper oxide on initiation surface of reaction during the plating process.

II. Experiment

A. Base conditions for the sample preparation

The basic condition of plating and compositions in a plating bath were shown in table 2.1 and 2.2, respectively. Copper Clad Laminate (CCL) was used as substrates in this report. We used Potassium Sodium L-(+)-Tartrate Tetrahydrate as a complexing agent and operated all plating experiments at 36 deg. C of a plating bath temperature. As we will mention in a later section, the plating process for sample preparation was changed depending on the target of factors to investigate. Additionally, when we plated samples, we followed the special sample plating method mentioned at the next section to prevent the influence from other factors excluding the targets on the void formation.

B. The special experiment method to plate

As mentioned in a previous section, it is necessary to form BVH on a substrate that the substrate is treated through various processes such as to promote adhesion between copper foil and resin, laminate process of resin and laser irradiation process to form BVH, and so on. We guessed if we would use the samples passed through these complicated processes, several factors such as laser condition and laminate condition, etc. were included as uncontrolled experiment parameters in our investigation. Therefore, we used commercially available CCL coupons as substrates. We devised a special method of sample preparation to pick up only the target factors for investigation among the other factors and we used it. We illustrated it in Figure 2.1.

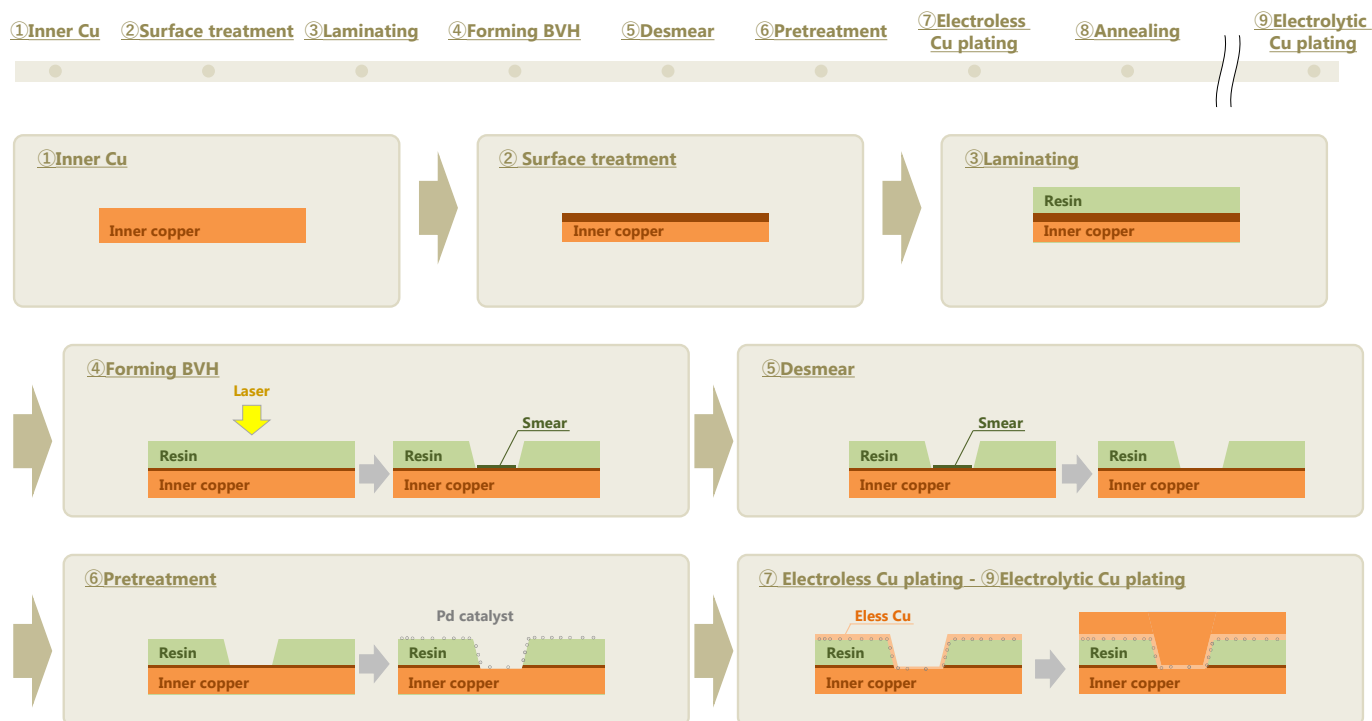


Figure 1.4 Procedure of Semi-Additive process for manufacturing Printed Circuit Board.

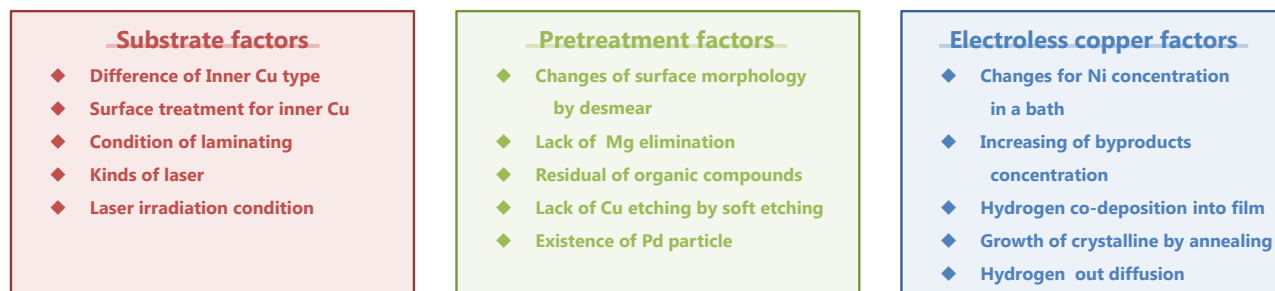


Figure 1.5 Factors in semi-additive process

Table 2.1 Preparation condition for samples

Preparation conditions	
Substrate	CCL (MCL-E-67)
Electroless Cu Bath	Indicated in table 2.2
Bath temperature	36 deg.C
Bath volume	500 mL
Loading factor	1.5 dm ² /L/L
Air flow rate	100 mL/L/min
Rocking	1.3 cm/sec
Cylinder shock	none

Table 2.2 Bath composition

Bath compositions	
Chelating agent	KNaC ₄ H ₄ O ₆ ·4H ₂ O
Copper resource	CuSO ₄ · 5H ₂ O
pH adjusting agent	NaOH
Reducing agent	HCHO
Stress relaxation agent	NiSO ₄ · 6H ₂ O
additive	several

In every experiment indicated in this report, we followed the sample preparation method as shown below:

- 1) Before the sample was immersed in an electroless copper bath, a CCL coupon as a dummy coupon was immersed to start the plating reaction.
- 2) The sample which was passed through the pretreatment process was immersed in the same bath after 5 min from the immersion of the dummy.
- 3) Then, the sample was connected with the dummy immediately as quickly as possible. By passing this step, it became possible to plate with reproducibility a sample even without using the general pretreatment process.

We have called this special sample preparation method “a connected plating method” and we adopted it in this report.

inner layer underneath. It is extremely difficult to identify the electroless copper layer from the other copper layers like the electrolytic copper layer and inner layer copper with just STEM observation. However, it becomes possible to recognize the electroless copper layer from results of EDX mapping images because a typical Rochelle-type electroless copper bath contains Ni^{2+} and the deposit from such a bath should be incorporating Ni^{2+} . In this report, mapping results from EDX analysis, especially Ni mapping images, were utilized to identify the electroless copper layer including Ni ions within the deposit.

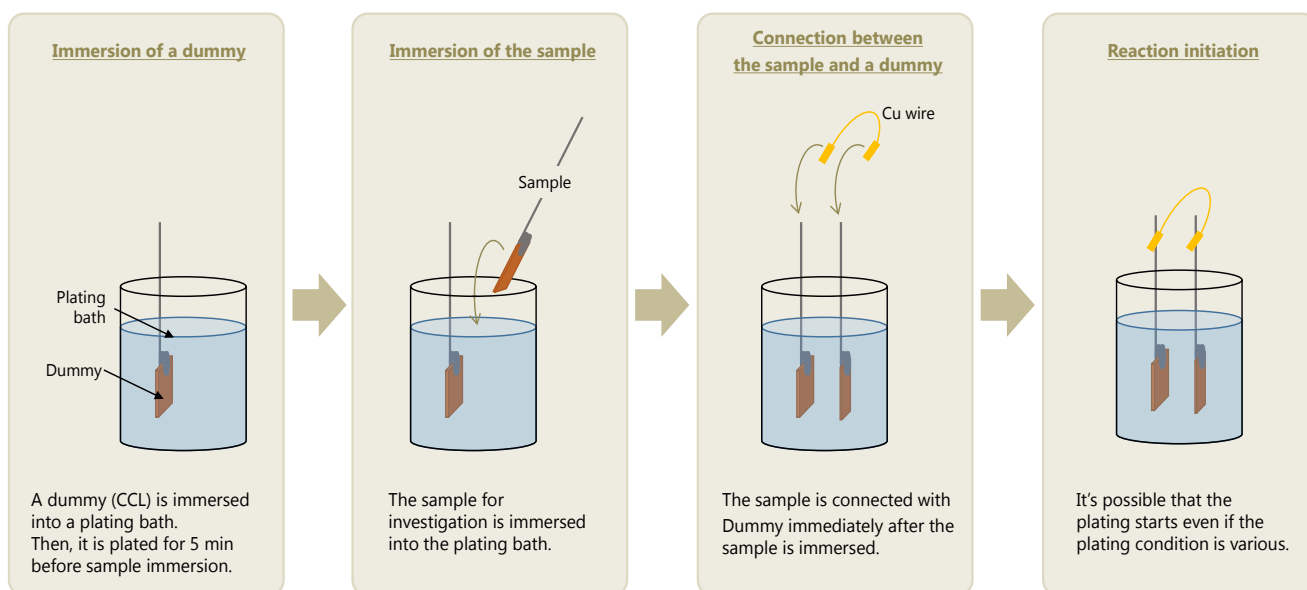


Figure 2.1 Plating method for sample preparation named as “a connected plating method”

C. Process flow about all experiments

As shown in Figure 1.5., the factors relating to void formation can be thought of. Treatment conditions to investigate these factors were indicated in Table 2.3.

D. Methods for characterization

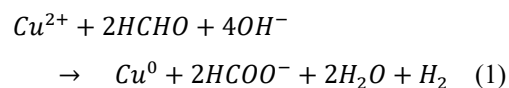
The samples that were prepared following “a connected plating method” and were passed through the treatment process indicated in Table 2.3 were processed with FIB-SEM to obtain TEM lamellas for STEM observation. The obtained lamellas were observed with STEM to confirm whether or not there are any voids at Cu-Cu interface between electroless copper and inner layer copper. Additionally, the compositions of the plating deposits were clarified with EDX analysis. The crystalline structure of an electroless copper plating film grows following the crystalline structure of the

Moreover, the surface of the inner layer copper was analyzed with AES (Auger electron spectroscopy) to investigate the surface state of the inner layer copper at the initiation surface of the reaction. Finally, we considered the influence of the surface state on void formation as quantitatively as possible based on the results of STEM and AES.

III. Results & Discussions

A. The influence of treatment process within SAP

Electroless copper reaction proceeds with (1).



As confirmed in this equation, when Cu^{2+} is reduced by formaldehyde used as a reduction agent from ion to metal

Table 2.3 Treatment process to investigate the cause of void formation

Step	Temp. [deg.C]	Time [min]	Condition	Flesh Cu surface	Desmear	Pd for activation	ALCUP	Annealing	Ni 20%	Ni 200%	Aging bath	150 deg.C 1.0 hr	150 deg.C 3.0 hr	180 deg.C 1.0 hr	180 deg.C 3.0 hr
				#1-1	#1-2	#1-3	#1-4	#1-5	#2-1	#2-2	#2-3	#3-1	#3-2	#3-3	#3-4
Sweller	70	10	---	---	●	---	---	---	---	---	---	---	---	---	---
Resin etching	80	20	---	---	●	---	---	---	---	---	---	---	---	---	---
Newtralizer	35	5	---	---	●	---	---	---	---	---	---	---	---	---	---
Cleaner	40	5	---	---	---	---	●	---	---	---	---	---	---	---	---
Soft Etching	25	2	---	●	---	●	●	●	●	●	●	●	●	●	●
Acid Rinse	25	1	---	●	---	●	●	●	●	●	●	●	●	●	●
Predip	25	2	---	---	---	●	●	---	---	---	---	---	---	---	---
Activator	40	5	---	---	---	●	●	---	---	---	---	---	---	---	---
Reducer	35	3	---	---	---	●	●	---	---	---	---	---	---	---	---
Accelerator	RT	1	---	---	---	---	●	---	---	---	---	---	---	---	---
Annealing	150	60	---	---	---	---	---	---	---	---	---	●	---	---	---
		180	---	---	---	---	---	---	---	---	---	---	●	---	---
	180	60	---	---	---	---	---	---	---	---	---	---	---	●	---
		180	---	---	---	---	---	---	---	---	---	---	---	---	●
Eless Cu	36	60	Normal	●	●	●	●	●	---	---	---	---	---	---	---
			Ni 20%	---	---	---	---	---	●	---	---	---	---	---	---
			Ni 200%	---	---	---	---	---	---	●	---	---	---	---	---
			Aging bath	---	---	---	---	---	---	---	●	---	---	---	---
Annealing	180	60	---	---	---	---	---	●	---	---	---	---	---	---	---

state, occurrence of hydrogen accompanies the reaction. Such hydrogen occurring during the plating reaction will gather on the surface of the reaction and will almost desorb from the surface into an electroless copper bath. But other reports related to an investigation of void formation said that some hydrogen would be incorporated randomly into the film [5].

Some reports had already studied the effect of hydrogen occurring during the plating reaction. Among these reports, Okinaka et al. researched the correlation between incorporated hydrogen in a Cu film and the mechanical properties of the film in detail [6]-[9]. They pointed out in several reports that such hydrogen in a plating film was related to the mechanical properties of the film such as ductility.

In this report which studied the electroless copper deposit, it should be difficult to identify the target factors if the electroless copper reaction would cause the formation of voids at the Cu-Cu interface and in the deposit by itself. Thus, we estimated the influence of the plating reaction on the void formation as we plated the sample through the treatment process followed by #1-1 in Table 2.3. The results were indicated in Figure 3.1.

The electroless copper deposit was obtained on the inner layer copper surface where any organic components and Pd particle for activation were not present since the substrate passed only soft etching and acid rinse but did not pass any processes including organic and Pd. It can be translated that this treatment condition reflects the influence of the plating reaction itself on the void formation.

As results show in Figure 3.1, it could be found that a copper deposit was growing with epitaxial crystalline

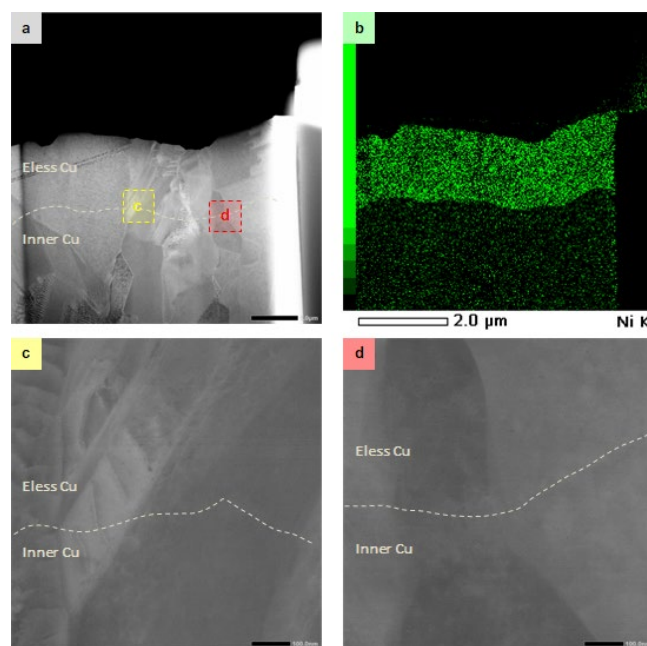


Figure 3.1 the influence of Eless Cu reaction on the voids formation
a) Overall, b) Ni mapping, c) and d) magnified view

from the inner layer copper and none of dark contrast was present which would indicate the existence of voids. Thus, we could conclude that the hydrogen and other factors produced during electroless copper plating were not most critical factors for void formation in the process to manufacture substrate.

Whether the state of copper which was just treated through the Desmear process affected void formation or not was confirmed at the next experiment. As shown in Figure 1.4, there is the process to eliminate residual organic

components, which are generally called smear, left after forming BVH with laser by immersion in a potassium permanganate solution during the SAP. We followed by #1-2 to investigate the influence and indicated the results of this experiment in Figure 3.2. From this observation, the electroless copper film was deposited with good crystal continuity and it did not incorporate any voids even if the film was formed on the copper surface just treated by Desmear process. This result suggested that there is no influence of change on the copper surface after Desmear process on the void formation. We also thought that this result was contributed to enough neutralizer treatment to eliminate manganese being present on the copper surface after the Desmear process.

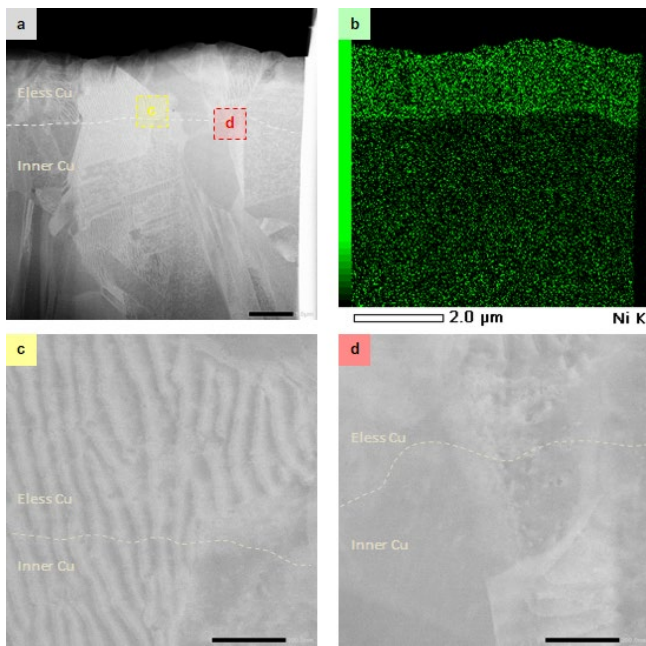


Figure3.2 the influence of Cu surface morphology after Desmear process on the void formation
a) Overall, b) Ni mapping, c) and d) magnified view

There is the process to activate the resin surface by Pd ion or Pd colloid in SAP in order to plate the surface of nonconductor substance such as glass epoxy resin. Therefore, the plating reaction at initiation step also occurred on the surface of Pd being on inner layer copper as well as the surface of resin in the process to form seed layer for adding conductivity. From this background, the influence of Pd being at the initiation step of the plating reaction was confirmed by treatment condition #1-3 and the result showing this influence was indicated in Figure 3.3 as cross-section of the deposit.

It can be observed that the copper film grain was grown with good continuity and any voids at the interface were not between electroless copper film and inner layer copper although Pd ion existed on the surface of the inner copper.

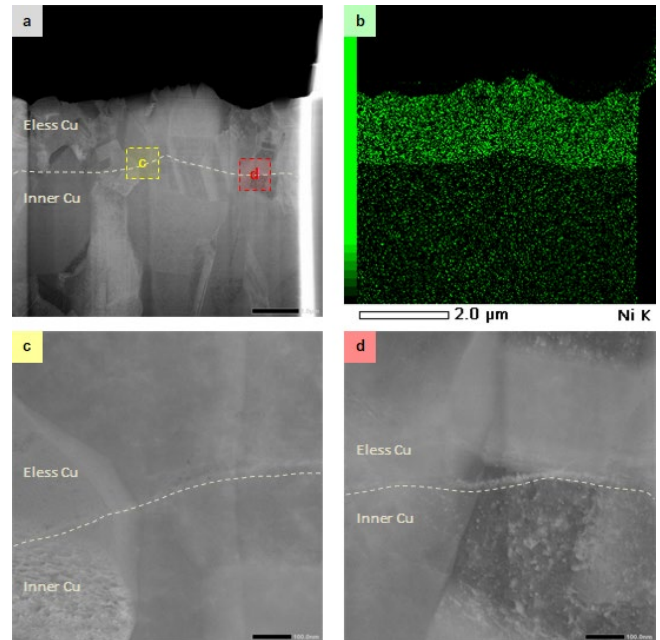


Figure3.3 the influence of Cu surface activated by Pd activator on the voids formation
a) Overall, b) Ni mapping, c) and d) magnified view

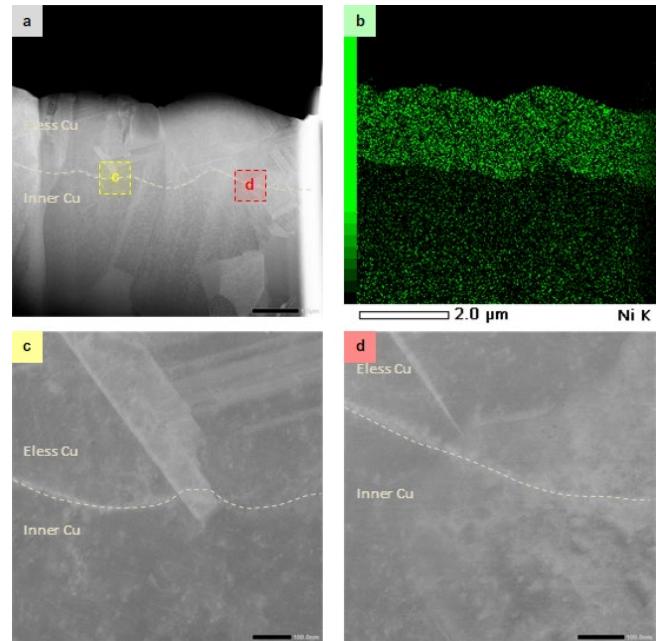


Figure3.4 the influence of ALCUP process on the voids formation
a) Overall, b) Ni mapping, c) and d) magnified view

The result would suggest that the probability to set off nanovoids by Pd activator was low.

Finally, we confirmed the influence of ALCUP process which we recommend for manufacture of the substrates on the formation of voids and showed in Figure 3.4 as this result. As a result of this experiment, any voids were not at the Cu-Cu interface if the substrate were treated with ALCUP

process.

Based on the results of STEM observation (#1-1~#1-4), it could be concluded that the pretreatment process from Desmar to Accelerator did not affect void formation significantly.

In the SAP, the substrate is often annealed at 100 deg. C to 200 deg. C after the electroless copper film is formed. A report written by Okinaka investigated the mechanism for improvement of ductility in electroless copper films as the research investigated the influence of annealing treatment after electroless copper plating [9].

So we investigated whether hydrogen in the film gathered by anneal treatment and voids were set off by it. From Figure 3.5 which was indicated as a result of this experiment, the void formation was not observed at the Cu-Cu interface as same as until now. Therefore, it could be stated that gathering hydrogen did not occur after annealing and was not related to the formation of voids in Rochelle salt baths which were used in this report. The result that the annealing did not affect the any voids formation is consistent with the above report.

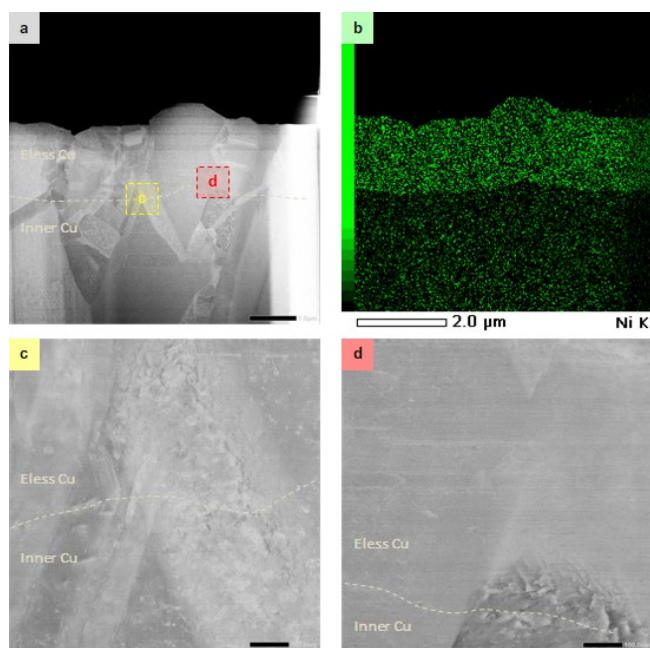


Figure3.5 the influence of Annealing after Eless Cu plating on the voids formation
a) Overall, b) Ni mapping, c) and d) magnified view

B. The influence of Ni^{2+} and byproducts in a bath

Ni^{2+} is contained in the general electroless copper bath which is used in the SAP in order to improve the residual stress of films. Some reports have already investigated the influence of Ni^{2+} on void formation and reliability of BVHs [10]-[13]. Thus, the influence of Ni^{2+} being included in an electroless copper bath on the void formation was also investigated in this report. The influence was confirmed by changing Ni^{2+} concentration from 20% to 200 % of the

standard solution concentration (Leg#2-1, 2-2) and the results of this investigation was shown in Fig.3.6.

In both the case of decreased Ni^{2+} concentration in the bath to 20% of the standard and the increased concentration to 200%, the electroless copper film grew with good continuity in crystalline and without any voids. As a result, we concluded that changing of Ni^{2+} concentration in the electroless copper bath did not significantly affect the void formation because there was no obvious difference between Fig. 3.1 and Fig 3.6.

As mentioned in section 3.A, the electroless copper plating reaction proceeds following equation (1). Formaldehyde used as the reducing agent transforms to formate after reducing reaction from Cu^{2+} to Cu^0 as indicated in equation (1). Additionally, an electroless copper bath which is used to manufacture the substrates is replenished Cu^{2+} consumed by plating reaction and copper sulfate is often used generally as the Cu^{2+} source. Thus, sulfate ion accumulates as the reaction proceeds. These things show that byproducts such as formate and copper sulfate are kept to accumulate in the electroless copper bath used in the field. Therefore, the influence of the byproducts on the void formation was also confirmed in this report and the result is shown in Fig.3.7. From this figure, it appeared there was no influence of accumulated byproducts on the electroless copper reaction except slightly increasing deposition rate and the electroless copper deposit grew without any voids.

According to this result, the probability to cause void formation from accumulated byproducts in the bath would be low.

C. The influence of copper oxide layer on inner layer copper

We have already confirmed that the plating reaction, pretreatment process to plate, and the concentration of Ni^{2+} and byproducts in the bath would not significantly affect void formation by investigation in sections 3.A and 3.B.

Finally, we assumed the existence of copper oxide which was left on the reaction surface at the beginning of electroless copper reaction owing to not enough treatment such as soft etching and acid rinse to eliminate oxide components and we investigated the influence of the residual copper oxide on the surface on the void formation. In this report, annealing under the various condition was adapted as the method to form copper oxide layer on the inner layer copper surface. We also thought that the influence of copper oxide thickness changed by several conditions on the void formation could be considered by this investigation.

First, the CCLs which were annealed under 150 deg. C - 60 min and 150 deg. C - 180 min were plated and then cross section of them were observed. The results were shown in Fig.3.8.

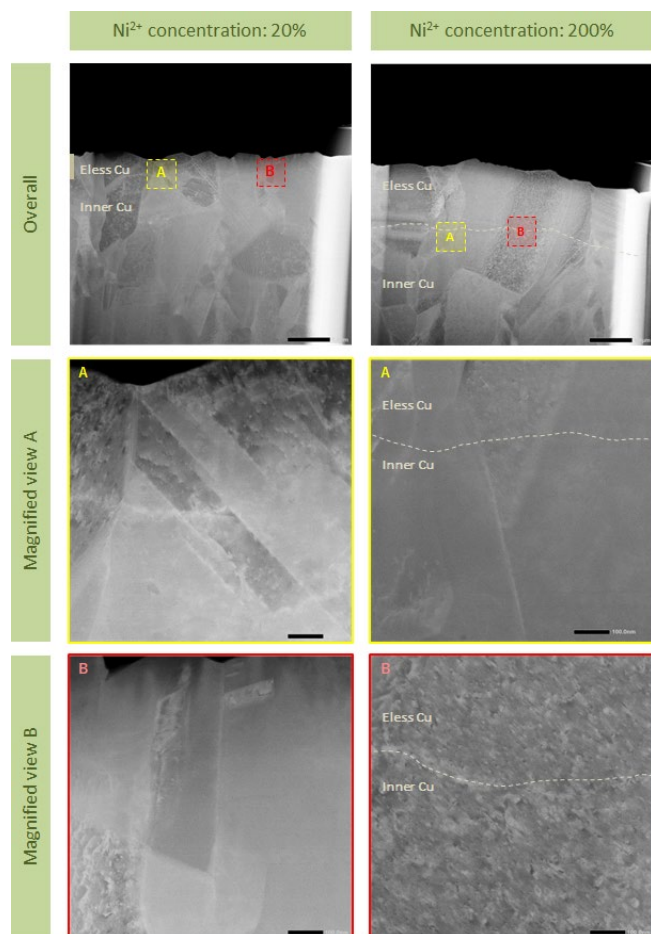


Figure 3.6 the influence of Ni^{2+} concentration in a bath on the voids formation

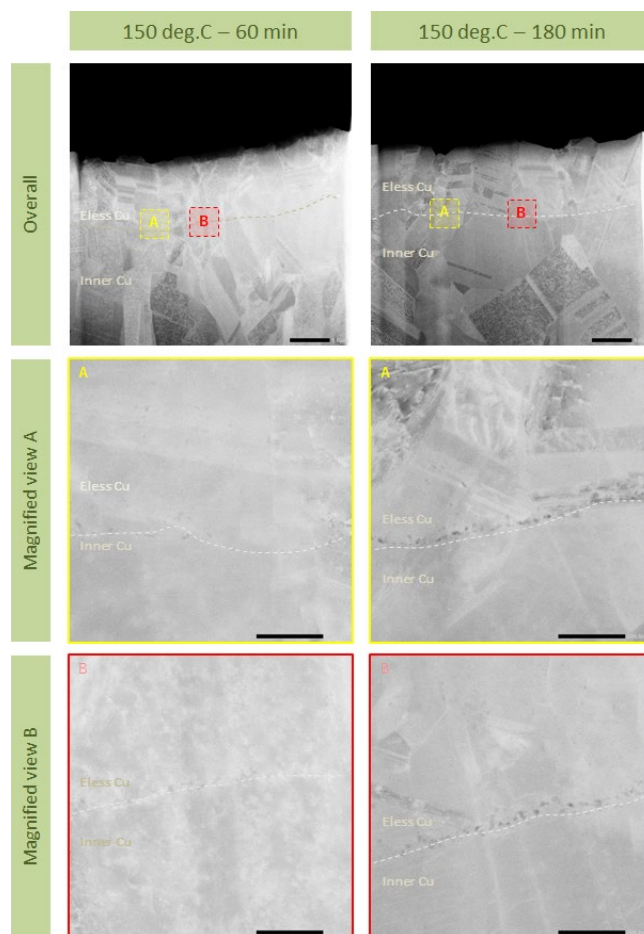


Figure 3.8 the influence of CuO layer formed at 150 deg.C on the voids formation

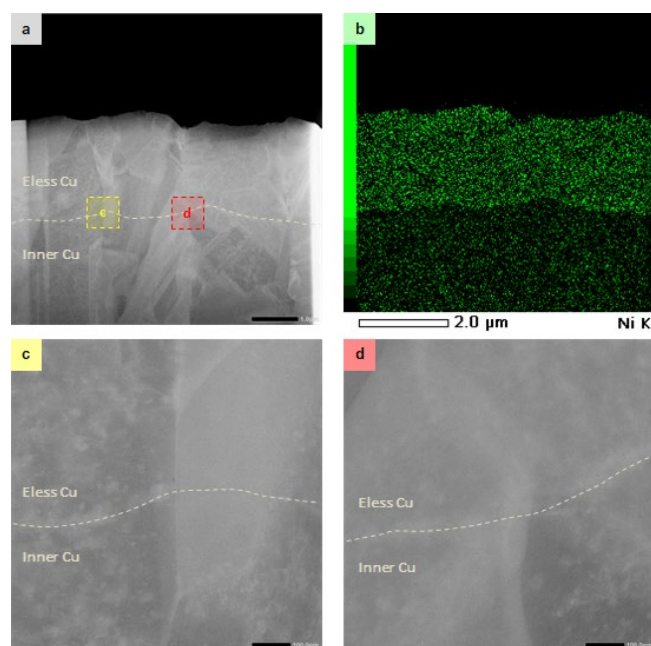


Figure 3.7 the influence of byproducts in a bath on the voids formation
a) Overall, b) Ni mapping, c) and d) magnified view

As shown in this figure, while the voids were rarely observed in the sample which was plated on the surface of CCL annealed under 150 deg. C – 60 min, it was confirmed under 150 deg. C – 180 min. We thought that this result suggested there is the influence of copper oxide and its thickness on void formation in electroless copper plating. Additionally, the conditions to anneal CCL were changed to 180 deg. C – 60min and 180 deg. C – 180 min and the cross-section views of the samples which were prepared on CCL annealed by those conditions were obtained with TEM as STEM images. Those were shown in Fig. 3.9. It would be confirmed that the voids occurred in the Cu-Cu interface with small diameter around tens of nm from the figure. It could also suggest that there is the tendency to form voids more as stronger annealing conditions from these results. We presumed that the reason why more voids were formed with longer annealing time and higher temperature is the changing of

copper surface morphology by each annealing condition.

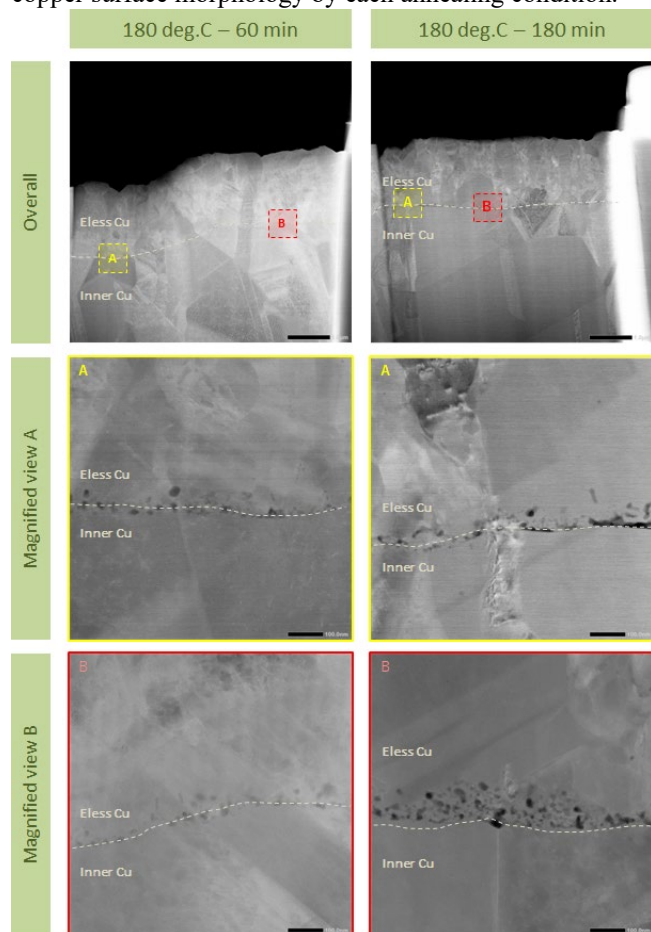


Figure3.9 the influence of CuO layer formed at 180 deg.C on the voids formation

The surface of CCL substrates after annealing was analyzed with AES to estimate the depth of copper oxide layer which was formed by annealing under each condition including 150deg. C - 60min, 150 deg. C -180min, 180 deg. C - 60min and 180 deg. C - 180min. Fig. 3.10 showed this result obtained by AES and could estimate 20nm to 90nm thick of the copper oxide formed as a result of annealing. If this figure was confirmed in more detail, it would be clear that the oxide layer on each sample got thicker at 20nm, 30nm, 60nm, 90nm with by changing annealing conditions, 150 deg. C - 60 min, 150 deg. C -180 min, 180 deg. C -60 min, 180 deg. C -180 min, respectively.

And the substrate annealed under 180 deg. C - 180min was also observed with TEM as STEM images and shown in Fig.3.11. Comparing Fig. 3.10 and Fig. 3.11, thickness of results obtained by both ways were similar to each other. Therefore, AES results seemed to be correct. It could be observed from Fig. 3.11 that the oxide area was formed with stratification after annealing. Meanwhile, that layer was not confirmed anywhere at all conditions after plating, but instead, contrasts with dots were only observed around the Cu-Cu interface. Additionally, the area where dot contrasts occurred is consistent with the area where the oxide layer was formed after annealing by comparison between Fig. 3.9 and 3.11.

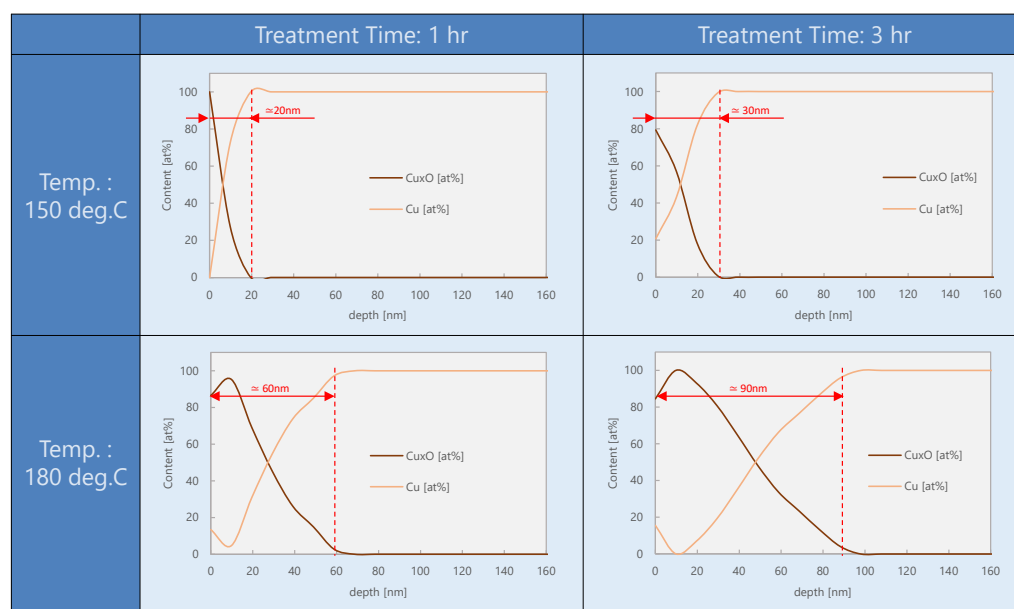


Figure3.10 the influence of annealing condition on the Cu oxide layer in thickness.

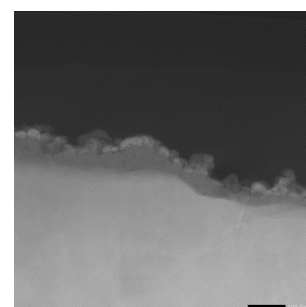


Figure3.11 Cross section view of CuO in STEM

These results would suggest that if the reaction of electroless copper plating occurred on copper oxide, this oxide compound was reduced to metal state by reduction with any reducibility substances relating to plating reaction, such as hydrogen and formaldehyde. If the electroless copper plating reaction set off on copper occurred from a part of the oxide layer, copper oxide would be incorporated under the electroless copper deposit. We have supposed that this copper oxide captured in electroless copper layer could contribute to form voids. Compared to a report that had investigated reactivity among hydrogen and copper oxide being between metal copper layers [14] and the present report, the formation of voids could be contributed that hydrogen arising during plating reaction would react with incorporated copper oxide and H_2O was changed from itself at the Cu-Cu interface. But the more investigations should be needed to reach this conclusion.

IV. Conclusion

The factors that have the probability to cause void formation and would be included in the SAP were investigated to evaluate whether or not they affect voids. If the samples to investigate the formation of voids were prepared by the general plating process, we expected that the results from the general process were affected by numerous factors, mutually. The special plating method devised that is called “a connected plating method,” and was adapted to evaluate just one factor or targeted factors for investigation. Based on the results obtained with STEM observation, EDX analysis and AES, we investigated the influence of the plating reaction itself, treatment process, Ni^{2+} and byproducts being in a bath, and copper oxide layer at the beginning of the reaction on voids formation. As a result, it became clear that existence of copper oxide on the reaction initiation surface affects the voids formation significantly. We have mentioned that there is the probability that copper oxide incorporated in the deposit is related to the void formation based on the sample observation and the other results as far but more investigations is needed to identify the root cause of the void formation. Future work will reveal the mechanism of voids formation.

References

- [1] S. Ghosh: Thin Solid Films, Vol. 669, 641-658, (2019).
- [2] T. Bernhard, L. Gregoriades, S. Branagan, L. Stamp, E. Steinhäuser, R. Schulz, F. Brüning, “Nanovoid Formation at Cu/Cu/Cu Interconnections of Blind Microvias: A Field Study”, International Symposium on Microelectronics (2019).
- [3] T. Bernhard; S. Zarwell; E. Steinhäuser; S. Kempa; F. Brüning, “The Effect of Cu Target Pad Roughness on the Growth Mode and Void Formation in Electroless Cu Films”, IWLPC (2019).
- [4] Z. Zhang, Ming-Chun Hsieh, R. Liu, J. Yeom, A. Suetake, H. Yoshida, C. Chen, J. Kang, H. Honma, Y. Kitahara, T. Matsunami, K. Otsuka, K. Suganuma, Microelectronics Reliability, Vol.138 (2022) 114707.

- [5] N. Fukumuro, K. Tohda, and S. Yae: J. Electrochem. Soc. vol.169 122505 (2022).
- [6] Y. Okinaka and S. Nakahara: J. Electrochem. Soc. vol. 123 475 (1976).
- [7] S. Nakahara: Acta Metallurgica, vol. 36, 7, 1669-1681 (1988).
- [8] S. Nakahara and Y. Okinaka: J. Electrochem. Soc., vol. 136 7 (1989).
- [9] S. Nakahara, C. Y. Mak, and Y. Okinaka: J. Electrochem. Soc., vol. 138 5 (1991).
- [10] T. Sharma, A. E. Landry, A. Leger, D. A. Brown, T. Bernhard, S. Zarwell, F. Brüning, R. Brüning: Thin Solid Films, vol. 666, 76-84 (2018).
- [11] T. Bernhard, E. Steinhäuser, S. Kempa, G. Krilles, R. Massey, F. Brüning, “Nickel dependence of hydrogen co-deposition and nanoporosity in electrolessly deposited Cu-films”, ECTC (2020).
- [12] Z. Zhang, M. Hsieh, R. Liu, J. Yeom, A. Suetake, H. Yoshida, C. Chen, J. Kang, H. Honma, Y. Kitahara, T. Matsunami, K. Otsuka, K. Suganuma; Microelectronics Reliability, Vol. 138, 114707 (2022).
- [13] T. Bernhard, S. Manuela Bremmert, S. Dieter, L. J. Gregoriades, E. Steinhäuser, “Hydrogen Embrittlement Suppressors for Nickel-Free Electroless Copper Baths”; IMPACT (2022).
- [14] S. Konishi, M. Moriyama, M. Murakami; Materials Transactions, vol.43, 7, 1624-1628 (2002).