Panel-level Fan-out: Relationship Between Panel Size and Cost Reduction

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Abstract

Panel-level fan-out packaging is a growing segment of the packaging industry. Some analysts expect that 7% of fan-out packages will be built with panel-level fan-out technology by 2025. The key reason for designers to consider a change from wafer-level to panel-level fan-out is cost reduction. Most activities for fan-out packaging are batch activities performed on the entire wafer or panel at one time. The more die processed during batch activities, the greater opportunity for cost reduction.

Although this economic concept is simple, the reality of implementation is complicated. Handling wafer warpage and die shift can be a challenge even at the wafer level; these must be considered at the panel level as well. There are a few panel sizes available, and using the largest panel size for economic advantage may involve a trade-off with yield. New equipment or materials may be required, so capital expenditure should be considered as well.

It is one thing to recognize the potential cost advantage of producing more chips at once, but designers and fabricators must understand whether to expect a 5% or 50% cost reduction. This paper will analyze the cost of multiple designs built using wafer-level fan-out with a 300mm wafer, and panel-level fan-out using a 515x510mm panel and a 600x600mm panel. Key assumptions, such as package size and yield, will be tested to evaluate their impact on cost reduction. The goal of this paper is to analyze the cost reduction that can be reasonably expected when moving from wafer-level to panel-level fan-out..

Key words

Cost analysis, Cost reduction, Fan-out wafer-level packaging, FOWLP, Panel-level fan-out, Yield analysis

I. Introduction

Panel-level fan-out is a growing segment of the packaging industry [1]. The main drive behind using panels instead of wafers is the ability to process more packages at one time to generate cost reduction. However, determining how much cost reduction can be achieved is not a simple equation. There are multiple panel sizes to consider, which may have different handling and warpage challenges. Some processes must be changed; for example, instead of spinning on materials for photolithographic purposes, dry film lamination or slot coating must be explored, which means a different material and equipment set.

In this analysis, cost modeling is used to determine the cost of the same design built on a 300mm wafer, a 515x510mm panel, and a 600x600mm panel. Standard fan-out process flows are the focus of this analysis (versus advanced fan-out).

II. Activity Based Cost Modeling

Activity based cost modeling was used to construct the fan-out wafer level packaging and panel-level fan-out models used in this analysis. With activity-based cost modeling, a process flow is divided into a series of activities, and the total cost of each activity is calculated. The cost of each activity is determined by analyzing the following attributes: time required, amount of labor required, cost of material required (consumable and permanent), tooling cost, all capital costs, and yield loss associated with the activity.

All of the activities that are performed for wafer-level packaging are performed in the same order for panel-level fan-out. Even so, there are a few differences between activities at the wafer versus panel level. The key differences are:

- All dielectric and photoresist exposures take longer per panel than they do per wafer; a stepper is assumed for all scenarios, but since a panel is larger and exceeds the standard

reticle size, the exposure throughput is affected

• Photoimagable dielectrics and photoresists are spun-on for wafer-level packaging, but they are assumed to be laminated as dry films for panel-level packaging (this impacts material cost as well as equipment costs, considering the price of dry films versus liquid materials and the waste factor of spin-on)

• Etching and plating equipment is assumed to be more expensive for handling panels (but throughput is unchanged)

III. Cost Comparison

A. Cost per Package

The design used for analysis in this section is a 6x6mm package for a 4x4mm die from a $2,000 wafer; the fan-out package has a single RDL. To begin with, it is assumed that the same yield can be achieved for all three scenarios. The first table shows the number of die per wafer or die per panel in each scenario. The second table shows the cost per package savings associated with panel processing, as well as the percentage increase in packages per wafer/panel.

Table I. Die per Wafer/Panel – 6x6mm Package

	300mm	515x510mm	600x600mm
Die per wafer/panel	1473	5929	8100

Table II. Change in Cost per Package

	515x510mm	600x600mm
Cost Savings	42%	50%
Increase in Packages per Panel	302%	450%

Table II reveals two facts. First, if the same package can be built with the same yield achieved in a panel format, it would cost 40% to 50% less than it costs to produce the same package on a 300mm panel. One key caveat associated with this value (and the ones that follow) is that it is assumed the same factory parameters can be used in all scenarios. In reality, after a company invests in a panel-level packaging line, it is extremely likely that there will be higher indirect and overhead costs associated with the panel-level packages to offset the costs involved in setting up the line [2]. Real world pricing is expected to show a less favorable cost reduction than this purely technical comparison.

The second takeaway is that there is not a linear relationship between cost reduction and the increase in the number of packages that can be built on a panel. When considering cost reduction gained by moving from wafers to panels, some might assume that increasing the packages processed by 300% would result in a package that is one-third of the cost. Instead, it is a 40% reduction. That is because not every activity in the fan-out processing flow benefits from processing more packages at one time. This will be explored in more detail later in this section.

B. Cost per Panel

The next table changes the focus to cost per panel instead of cost per package. In other words, what this table shows is that if the activities that make up RDL processing were to cost $100 per 300mm wafer, those same activities would cost $179 per 515x510mm panel, and $219 per 600x600mm panel.

Table III. Change in Cost per Panel

	515x510mm	600x600mm
RDL	79%	119%
UBM	73%	111%
Ball Attach	233%	333%
Fan-out Processing	161%	236%

This table reinforces the claim earlier that cost does not scale in the same way across every activity. Each group of activities is discussed below.

• RDL – Almost all of the steps associated with creating a redistribution layer are per wafer/per panel activities. These types of activities are the ones that receive the greatest benefit from processing a greater number of packages at once. That is why there is only a 79% increase in cost but a 300% increase in packages per panel. If the cost increase scaled perfectly with the increase in packages, we would see a 300% increase in cost. If the exact same material cost, exposure time, and equipment could be used in both wafer and panel scenarios, we would see a 0% increase in cost per panel.

• UBM – This category is very similar to the explanation for RDL above.

• Ball Attach – This category is the opposite of the RDL and UBM activities. The cost of ball attach is primarily associated with the number of balls per package, which has nothing to do with packages per wafer or packages per panel.

• Fan-out Processing – This category includes things like the cost of the initial carrier, mold application, backgrinding, and die placement. Some of these activities are wafer-level/panel-level, such as mold and backgrind, while others are not wafer-level/panel-level, such as die placement. The cost to place the die is dependent on the number of die being placed, regardless of whether it is placed on a wafer or a panel. That is why the cost increase in this category is higher than the increase in the fully wafer-level/panel-level categories like RDL, but less than the increase for ball attach.

C. Impact of Package Size and Utilization

The next chart focuses on how savings change based on package size. This chart shows that package size does have an impact on how much the shift from a 300mm wafer to a 600x600mm panel might save, but it is not a major cost driver. For the package sizes tested, cost savings ranged from

45% to 55%. The spikes that show up in the chart are based on how panelization works at different package sizes; some package sizes are more favorable than others in terms of having less area lost to edge scrap and package-to-package spacing.

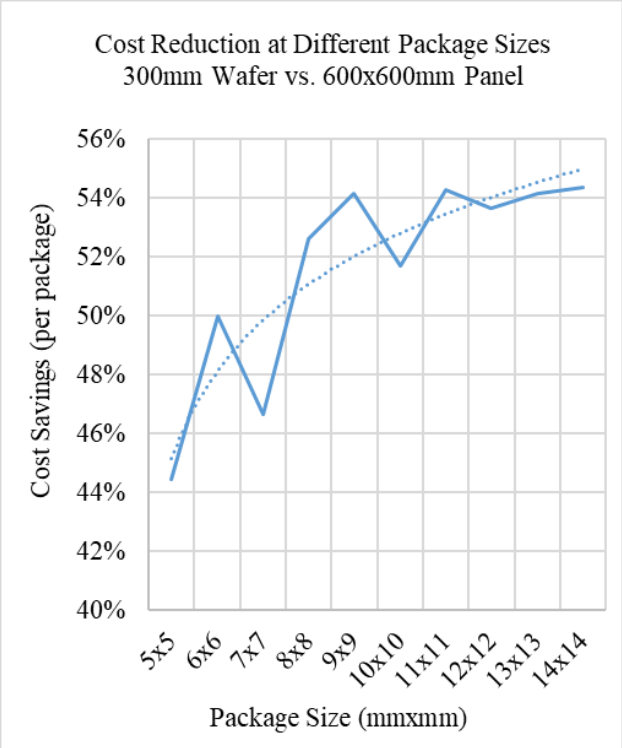

Figure 1. Cost Reduction at Different Package Sizes

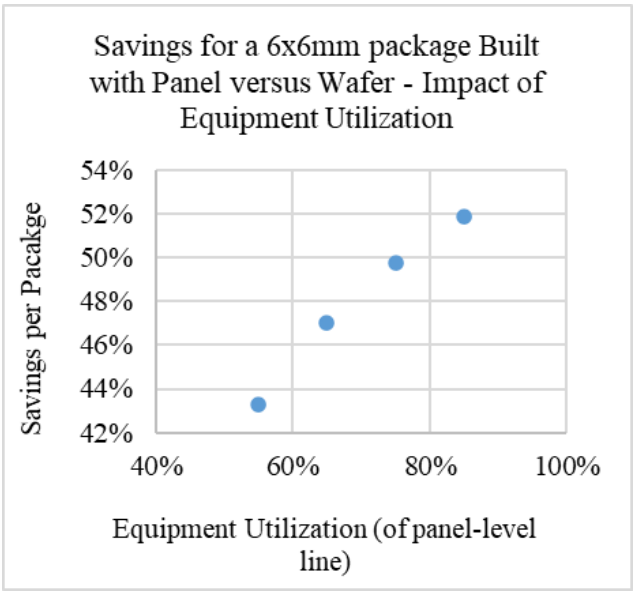

Figure 2. Impact of Equipment Utilization

The last tradeoff in this section focuses on a more indirect aspect of cost. The previous comparisons all assume that the packages being built on the wafers and panels are in well-balanced, highly-utilized factories. However, if a large panel means a factory can build many more packages at once, the question of utilization is raised. A panel line might only have to run at 60% utilization to meet the volume demands of the product, rather than a wafer line which might run at 85%. The following chart shows how the cost savings of the panel process may be eroded by a lack of factory utilization. In the chart in Fig. 2, the savings of building a 6x6mm package on a 600x600mm panel shift from over 50% to almost 40% with a drop in utilization.

IV. RDL Cost Breakdown

The creation of a redistribution layer can represent half of the steps in a fan-out wafer level packaging process flow. The previous section touched on how the cost of the group of RDL steps may be impacted by the shift to panel, but this section will focus on deeper details.

Depending on which part of the RDL creation process is considered, the move to panel can represent a major change or a minor change. The charts in Fig. 3 show how the cost breakdown between capital, material, and labor changes between creating an RDL on a 300mm wafer versus creating one on a 600x600mm panel.

The RDL built up on a 600x600mm panel has cost split more evenly between capital and material, whereas capital dominates the cost in the 300mm wafer-level RDL. This may seem like a surprising takeaway because less material is wasted in the photoresist and dielectric application processes on a panel due to the lack of a spin-on process, and the panel-level equipment is assumed to be more expensive. The following section breaks down how a handful of key steps drive this change in the type of cost.

- Dielectric and Photoresist Application Steps: The capital cost for these steps is similar on a per wafer/per panel basis in both scenarios. However, although the wafer spin-on process wastes a lot of material, there is much more surface area to cover on a panel, so the material cost per panel is higher than the material cost per wafer. But the cost of material per wafer does not scale with area; for example, to use the dielectric application step as an example, about $4 of material is “used” per wafer. This means that the equivalent of $4 of dielectric is dispensed, but only about 10% remains on the wafer. This is in contrast to about $6 dollars of dielectric material cost allocated to this step for the panel. The material cost is only two dollars higher because so much less is wasted.
- Exposure Steps: The exposure of the photoimagable dielectrics and photoresist represents a much higher capital cost in the case of panels versus wafers. This is because of throughput. A stepper is expensive, and it takes longer to expose a large panel than it takes to

expose a 300mm wafer. Slower throughput on expensive equipment means higher capital costs for the panel scenario.

- Metallization: The seed sputter and plating steps are the third group of steps that show different types of cost between the wafer and panel scenarios. The capital contributions are fairly close because the metallization rates do not depend on wafer and panel size. However, more material is required to metallize a 600x600mm panel than a 300mm wafer, so the material costs are higher per panel than per wafer.

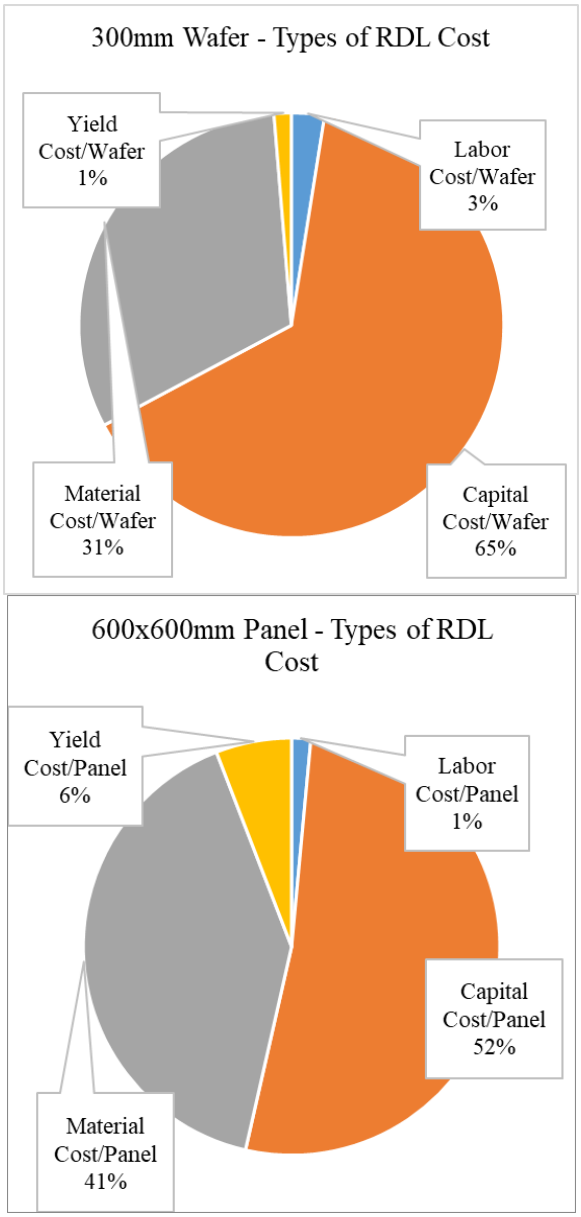

Figure 3. Types of Cost

Although these steps have different allocations of material and capital, it's important to keep in mind how it all breaks down per package. The following two examples show the relationship between the per package cost and the types of cost.

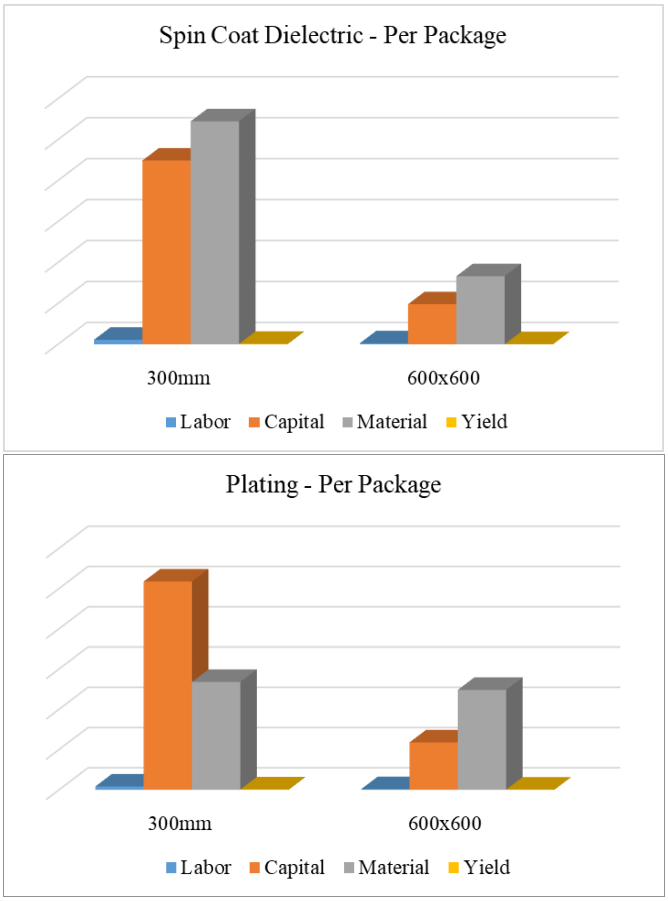

Figure 4. Cost per Package

V. Yield Comparison

Panel level fan-out cannot be discussed without also addressing yield. The benefit of processing so many packages per panel vanishes if high enough yields aren't achieved [3]. The yield impact of major panel warpage or die and RDL misalignment may cancel out any processing cost savings.

The design used for the first set of yield trade-offs is an 8x8mm die in a 10x10mm package with one fine l/s RDL. For comparison, it is assumed that the package built on a 300mm wafer achieves a 99% yield (though it should be noted that fan-out packages can certainly achieve higher yields than that). The yield assumption is adjusted for the 600x600mm panel example while holding the wafer-level packaging assumption steady.

When building this package around a die that comes from a $6,000 wafer, it can be seen that a loss of 3% yield in the panel process brings the per-package cost almost in line for both types of packaging.

The second chart shows that the cross-over point occurs more quickly when considering the scrap impact of a more expensive die. If the yield of the process for this package is 99% on a 300mm wafer, and 97% when using a large 600x600mm panel, the cost benefit is already erased.

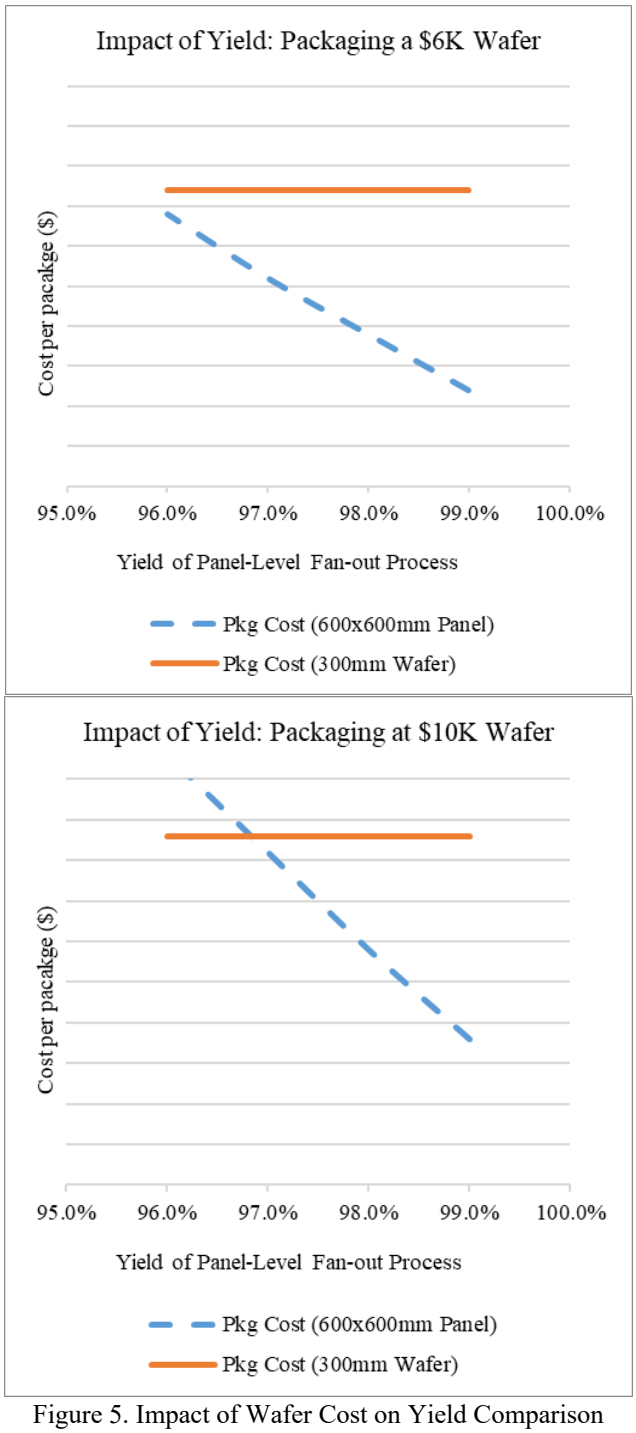

Figure 5. Impact of Wafer Cost on Yield Comparison

The next comparison examines how the level at which yield drives a crossover point between a wafer-level package and a panel-level package changes depending on panel size. The design used for this comparison is a 3x3mm die from a $7,500 wafer in a 5x5mm package. The cost of this package from a 300mm wafer is held steady at 99% yield and included in the chart as reference. The two panel sizes are tested across multiple yield assumptions.

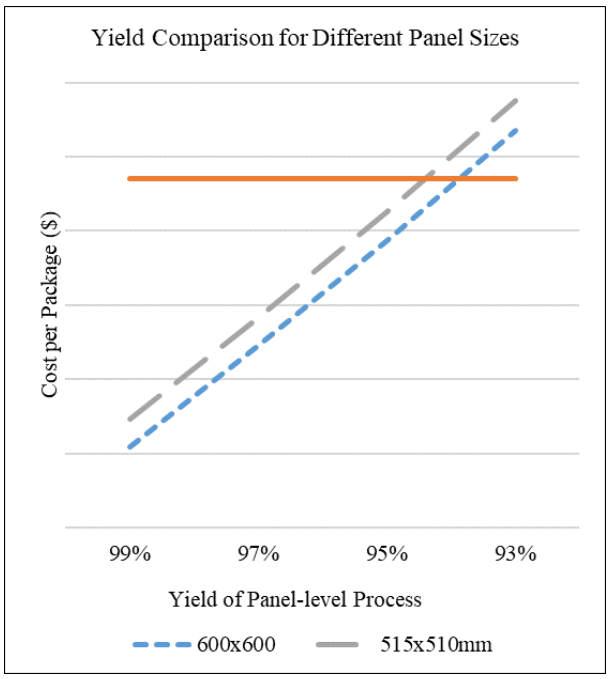

Figure 6. Impact of Panel Size on Yield Comparison

The chart in Fig. 6 shows how the cost of the same package built with panel-level packaging and fan-out wafer-level packaging increases as the yield decreases. For the package built with the 515x510mm panel, the crossover point occurs just past 95%. However, the crossover point is closer to 94% for the package from the 600x600mm panel. In other words, a little more yield loss can be sustained by the package from the larger panel before it no longer competes with a higher yielding package from the wafer.

VI. Conclusion

Activity based cost modeling was used to compare the cost of packages built using fan-out wafer level packaging with 300mm wafers to panel-level packaging using panels at two different sizes. It was established that savings up to 40% and 50% per package may be achieved by building designs on large panels. It was also shown that cost reduction does not scale linearly with the increase in the number of packages built at once. Some wafer-level and panel-level activities benefit more than others from panel processing.

The breakdown between material, labor, and capital costs changes when considering fan-out wafer-level packaging and panel-level fan-out. Yield also plays a key role in

determining whether panel-level fan-out is the right choice for any given package. Analysis showed that a small yield drop due to using large panels has the potential to erode any process cost savings gained from building more packages at once.

References

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