Advancing Semiconductor Packaging: Intelligent Architectures for Heterogeneous Integration Assembly

Glenn Farris, VP of Global Equipment Sales Operations & Marketing
Universal Instruments
33 Broome Corporate Parkway
Conklin, New York 13748 U.S.A.
Ph: 805 404 3420
Email: glenn.farris@uic.com

Abstract

The semiconductor industry is undergoing a profound transformation driven by the growing demand for enhanced performance, reduced energy consumption, faster time-to-market, and increased functionality. However, this evolution is accompanied by significant challenges, notably escalating costs over the past decade. Advanced packaging technologies leveraging Heterogeneous Integration (HI) have emerged as indispensable solutions to address these challenges and meet the dynamic demands of the market. This paper emphasizes the critical need for innovative and intelligent system architectures to overcome the hurdles in semiconductor packaging, particularly in achieving efficient Heterogeneous Integration assembly with the highest yield and optimal economics.

Keywords

Heterogeneous Integration, Advanced Packaging Semiconductor, Smart Assembly Solutions, Semiconductor Industry

I. Introduction

The semiconductor industry is experiencing a paradigm shift fueled by the rapid advancement of technology and the increasing demands of various market sectors. As the industry strives to meet the requirements for lower energy consumption, higher compute power, and faster time-to-market, the traditional approaches to semiconductor packaging are proving inadequate. Advanced packaging technologies, particularly those centered around Heterogeneous Integration, offer promising solutions to these challenges. However, realizing the full potential of HI assembly requires the development of innovative and intelligent system architectures that can optimize utilization, maximize yield, and ensure the industry's long-term sustainability.

II. Market Drivers

The demand for lower energy usage, increased compute power, faster time-to-market, and enhanced functionality across various sectors, such as server/network infrastructure, automotive, smart manufacturing, and consumer mobile devices, continues to drive the need for innovative semiconductor packaging solutions. These market drivers underscore the importance of advance packaging technologies to meet evolving industry requirements and customer expectations.

III. Challenges

Escalating costs, particularly in nodes below 22nm, pose significant challenges to the semiconductor industry. (Figure 1; Figure 2) Traditional semiconductor placement systems struggle to maintain high utilization for HI assembly applications, highlighting the need for smarter assembly solutions. Addressing these challenges necessitates the development of compact, comprehensive, and intelligent system architectures that can optimize economics while delivering the highest utilization and yield.

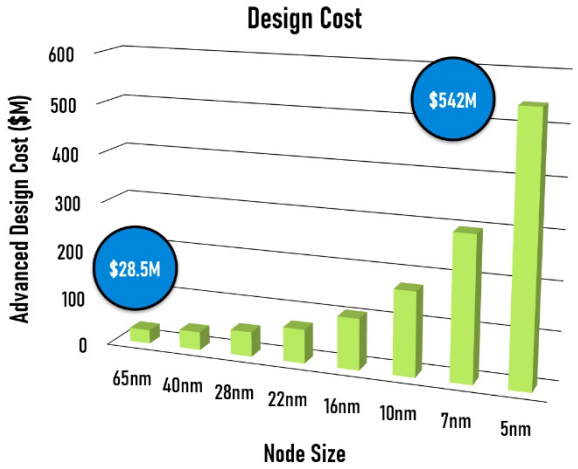

Figure 1: Design Cost - In recent years, advanced design costs have risen significantly, up by a factor of 7.75 over the last ten years for nodes below 22nm. (1)

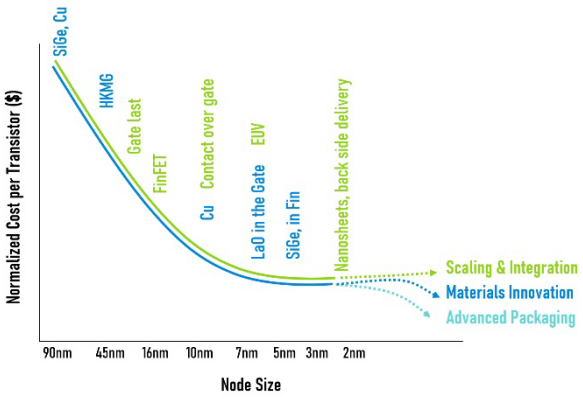

Figure 2: Normalized Cost Per Transistor -Transistor cost scaling stalled at 28 nm and remains relatively flat. (2)

IV. Implications for the Industry

Efficient Heterogeneous Integration assembly demands the ability to process die from various presentation sources, including wafers, tape & reel, waffle pack, JEDEC tray, and specialized trays. (Figure 3, Figure 4, Figure 5) Meeting these demands requires comprehensive solutions seamlessly integrating different die types and presentation formats, maximizing utilization, and optimizing manufacturing processes in several key ways:

Increased Flexibility**:** Accommodating multiple die formats enables sourcing from a broader range of suppliers and technologies, which is essential for efficiently integrating diverse materials and devices in heterogeneous integration.

Streamlined Workflow**:** Processing various formats seamlessly integrates different dies, reducing reformatting, bottlenecks, and downtime, leading to faster transitions and improved throughput.

Maximized Equipment Use**:** Versatile equipment reduces idle time and maximizes utilization, keeping manufacturing tools productive across different die formats.

Cost Efficiency**:** Supporting multiple formats lowers investment in specialized equipment, reduces handling errors, and minimizes rework, cutting overall costs.

Optimized Inventory**:** Flexibility in processing various dies allows for diverse inventory management, enabling quicker responses to demand changes and reducing shortages or overstock.

Improved Yield & Quality**:** Efficient integration minimizes damage and contamination, enhancing yield and quality, which is critical for the precision of heterogeneous integration.

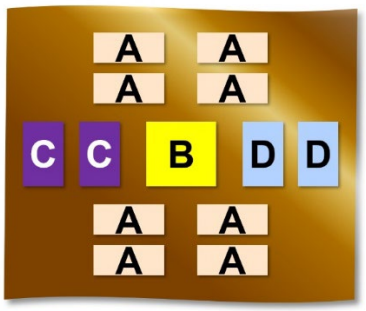

Figure 3: Typical HI Device- Typical HI devices integrate multiple different die into a higher-level assembly, providing enhanced functionality and performance.

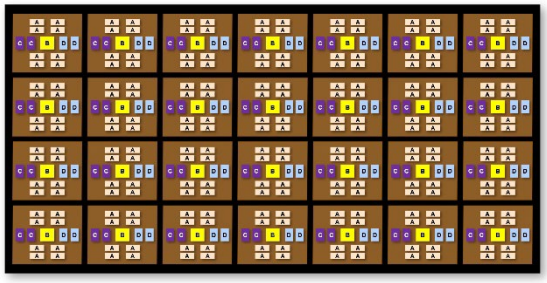

Figure 4: Typical HI Device in JEDEC Tray

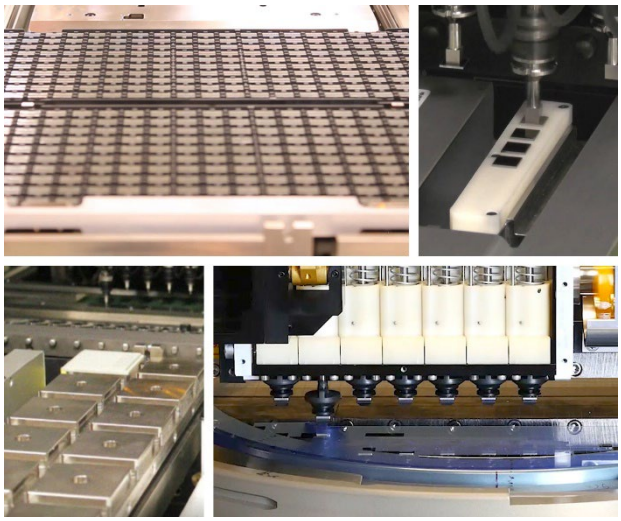

Figure 5: Die Feeding Types - Due to the complexity of H I assembly requirements, it is essential to have the capability to process dies from various presentation formats, including wafers, tape & reel, waffle packs, JEDEC trays, and specialized trays, to meet these specific needs.

V. Smart Assembly Solution Requirements

To address the needs of the semiconductor industry, smart assembly solutions must prioritize the lowest line depreciation and highest utilization. This necessitates the development of compact, integrated systems capable of rapid die exchange, high-speed operation, and adaptive sequencing to optimize economics. (Figure 6). The ultimate multi-die solution for heterogeneous integration should offer ample wafer capacity, support for multiple die types, accommodation for large substrates, and the ability to handle thin die to maximize yields and minimize scrap costs.

Figure 6: Smart Assembly Solution- The ideal smart assembly solution has the required system design elements to support HI.

VI. Smart System Software Architecture Elements

The software architecture of smart assembly solutions plays a critical role in achieving the highest utilization and yield. Elements such as full multi-die circuit offline programming for New Product Introduction (NPI) (Figure 7) program optimization and intelligent error recovery via adaptive sequencing are essential for maximizing productivity and minimizing scrap costs. Smart multi-die capabilities further reduce operator intervention, especially in complex HI assembly processes. (Figure 8)

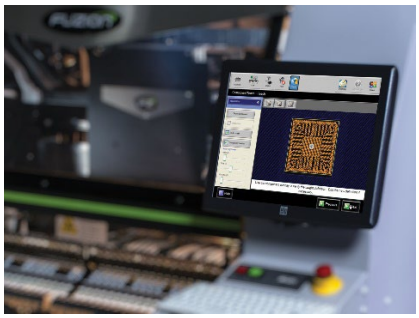

Figure 7: Offline Programming for NPI- Comprehensive offline programming tools facilitate efficient processes.

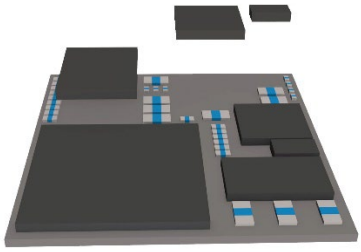

Figure 8: Multi-Die Package- Multi-die program optimization and error recovery help to maximize utilization and yield.

VII. Smart System Software Value

Achieving the highest utilization and yield requires intelligent software solutions that optimize assembly processes and adapt to changing production requirements. By implementing adaptive sequencing algorithms, semiconductor manufacturers can minimize operator intervention (Figure 9), reduce downtime, and mitigate scrap costs (Figure 10), maximizing revenue and improving overall economics. (3) The impact of adaptive sequencing can be profound.

Due to a persistent failure rate, the scrap cost can remain high without adaptive sequencing. However, implementing adaptive sequencing techniques can significantly reduce the failure rate by dynamically adjusting the manufacturing process based on real-time feedback and historical data. This adjustment reduces the number of defective circuits, thereby lowering scrap costs.

Potential savings from reducing the failure rate can be substantial. For example, if adaptive sequencing reduces the failure rate by 50%, the annual scrap costs could be halved, resulting in savings of $350,000, based on the example cited in (Figure 10).

The broader economic impact of adaptive sequencing extends beyond cost savings. Lower scrap rates mean more efficient use of raw materials and resources, contributing to better resource utilization. Additionally, reducing scrap aligns with sustainability goals and potentially improves the company's environmental footprint by producing less waste. Furthermore, improved processes and fewer defective units can enhance operational efficiency and productivity, boosting profitability.

Strategic recommendations include prioritizing implementing adaptive sequencing technologies to adjust and optimize the manufacturing process dynamically. Establishing robust monitoring systems and feedback loops is essential for continuously gathering data and improving the process. Training employees on the importance and use of adaptive sequencing ensures effective adoption and utilization. Investing in research and development is crucial to exploring advanced adaptive sequencing algorithms and technologies that can further reduce failure rates.

Due to a high failure rate in the 10-die circuit manufacturing process, the current scrap costs referred to in (Figure 10) highlight the significant financial impact of defects. By implementing adaptive sequencing, a company can reduce the number of defective circuits, thereby lowering scrap costs and enhancing overall efficiency and sustainability. This strategic investment can improve the bottom line and contribute to long-term operational success and environmental responsibility.

Figure 9: Operator Intervention - At 100ppm, a system requires operator intervention every 1.1 hours for a circuit with 10 total die. This results in an 8% uptime reduction and more than $50 million in foregone revenue.

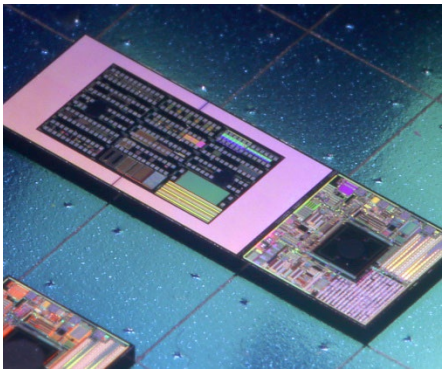

Figure 10: Bad Circuit - For the same 10-die circuit, there is one bad circuit out of every 1000 built. This results in $700K in annual scrap costs without adaptive sequencing.

VIII. Conclusion

In conclusion, the semiconductor industry stands at the cusp of a transformative era, driven by the need for innovative packaging solutions to keep pace with evolving market demands. Advanced packaging technologies, particularly Heterogeneous Integration, offer immense potential to address these challenges and unlock new opportunities for semiconductor manufacturers. However, realizing this potential requires the development of intelligent system architectures and smart assembly solutions capable of maximizing utilization, optimizing yield, and ensuring the industry's long-term sustainability. By embracing innovation and collaboration, the semiconductor industry can pave the way for a future of efficiency, agility, and technological advancement in semiconductor packaging.

References

[1] IBS, "3nm Process Node," *ExtremeTech*, 2019. Online]. Available: https://www.extremetech.com/computing/272096-3nm-process-node.

[2] Semi Analysis, "A Century of Moore's Law," *Semi Analysis*, 2023. [Online]. Available: https://www.semianalysis.com/p/a-century-of-moores-law.

[3] G. Farris, "Intelligent Architectures for Heterogeneous Integration Assembly," presented at *Semicon*, Taiwan, 2023.